Surface contamination (α,n)

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Potential sources of surface (a,n)

Surface contamination before arrival to our hands (α,n)

Affects everything that we buy off-the-shelf. **Important with chips: 0.04 events in 10 y**

Our techniques for small components don't disentangle bulk/surface.

Mitigation: Cleaning (only large surfaces, not electronics), conformal coating?

Surface contamination on our side, (α,n)

Affects everything we store for long periods. **Important for PDU: 0.05 events in 10 y**

This contribution builds up after measurement.

We can monitor but it's irreversible (in most cases).

Mitigation: Cleaning (only large surfaces, not electronics), conformal coating? Rn-free storage

SaG4n specifically developed to study these effects

Surface contamination before arrival (small electronic components)

Affects everything that we buy off the shelf.

Our techniques for small components don't disentangle bulk/surface.

Quantification:

We routinely screen via ICPMS (LNGS, Mendeleev, CIEMAT)+ HPGe (LSC, LNGS, SNOLAB, Boulby)

+ Po extraction (Krakow).

Here assuming all the Po contamination is actually on surface).

- **50 Bq/kg in 210Po**
- **# Chips /PDM: 120**
- **# PDMs: 8400**
- **resulting total 96 Bq**
- **# decays 3×10^{10}**

After CUTS	
nSource	Elec
itself	0.016
Argon	0.024
Sum	0.040

After CUTS	
nSource	Elec
itself	0.016
Coating	0.013
Sum	0.029

>25% reduction with coating

Surface contamination during storage (on our side)

Affects everything we store for long periods.

This contribution builds up after measurement.

We can monitor but (currently) it's irreversible for small components.

Quantification in PCBs:

Assuming:

15 Bq/m3 for 3 y exposure

nSource	PCB Cu	PCB subs	TOTAL
itself	3.20E-3	8.87E-3	**1.21E-2**
Argon	2.20E-2	1.30E-2	**3.50E-2**
Sum	2.52E-2	2.19E-2	**4.71E-2**

Plate out rate as in SNOLAB's measurement: 249 atoms/ d / cm^2 in PE (423 in Cu).

Same +

coating happening after mentioned

3 y exposure.

nSource	PCB Cu	PCB subs	TOTAL
itself	3.20E-3	8.87E-3	**1.21E-2**
Coating	1.20E-2	7.10E-3	**1.91E-2**
Sum	1.52E-2	1.60E-2	**3.12E-2**

Reduction of 35% of this contribution

Reduction of 16% of the goal budget (reference, ~ all the RPUF insulation in the cryostat)

Strategies

Mitigation

Surface cleaning: Cu OK.

Not feasible currently for the critical elements (finished PCBs).

Conformal coating? Under evaluation. Seems feasible but requires R&D.

Clean Storage.

A) Clean room concept: No secret, but needs money.

B) 3-Bags filled with N_2: Identified by Legnaro, permeability studied in Marseille.

Quantification of surface "adherence":

Measuring half of the batch + exposing the other half to a known (high) activity for a known time. The ratio gives you an **indication of the importance of the surface to bulk**.

Summary

Current backgrounds accounted for:

	bg ev in 10 y	comment
Random S1-S2	**0.05**	Decision driven
measured Po in chips	**0.04**	All the Po measured assumed in surface
storing Po in PCBs	**0.05**	15 Bq/m3 for 3y. 10 x top TPC surface
Total	**0.14**	On top of bulk (between 0.1-0.2 itself)

The preliminary "worst case scenario" for (α,n) from electronics (all measured Po on surfaces, storage for 3 years in normal air) gives ~0.1 (potentially ~0.06 with coating).

Quantification of the storage time of each material (specially large surfaces) necessary to quantify this effect for other materials.

The procedure for estimating surface backgrounds is much more tricky than the evaluation of bulk-induced backgrounds.

Copper Protocol Results and future DS implementation

Tumbling (~1 um) + electropolishing (~ 100 um) + chemical etching (~5 um)

1. We have green light, from recent measurement the 210Po is removed from the surface. Reduction to ~mBq/m2 [x7 or x74 depending on initial level].
2. The transport of components under vacuum inside 3 bags (each one of 3 layers = PE-PA-PE) prevent the Radon plate out (Jose Busto measurement= Radon transparency of 0.25% with 3 bags)
3. Tracking the components from the production until the installation is mandatory for an effective contamination protocol and quality control (bar code or qwerty code for each component)
4. The Protocol to avoid recontamination should be also valid for SS and electronics (to verify)