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Business Analysis and Trade-Offs for Chiplet-Based System Design

Marek Hempel, Anu Ramamurthy, Kash Johal, Trent Uehling, James Wong, Irina Sellhusen, Rajesh Pendurkar, Boon Chong Ang, Allan Cantle, Bapi Vinnakota

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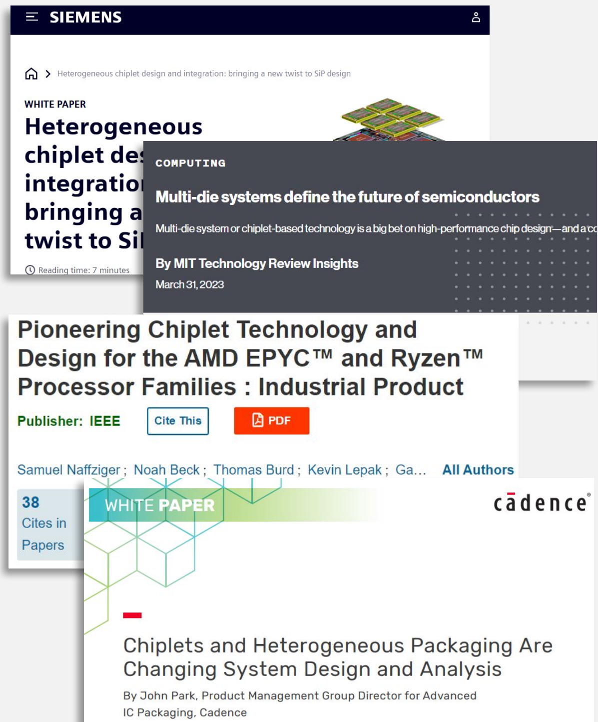
Why another Whitepaper on Chiplets?

Chiplet Whitepapers

- Most whitepaper only focus on benefits/challenges



Cost Calculators

- Full factory cost alone does not capture all details

		Monolithic Baseline	Chiplet
Inputs	Die/Chiplet Eff Area (mm2)	500	175
	Wafer Size (mm)	300	300
	Quantity	1	3
	Wafer Price	$ 10,000	$ 10,000
	Process Maturity	Very Mature	Mature
	Defect Density	0.05	0.08
	Wafer sort time (s)	20	15
	Wafer Sort Cost	$ 1.39	$ 1.04
	Package & Interposer Cost	$ 30	$ 35
	Final Package Test Time (s)	20	20
	Final Package Test Cost	$ 1.39	$ 1.39
Chiplet Outputs	GDPW	109	346
	NDPW	85	301
	Yield (Murphy Model)	78.3%	87.1%
	Silicon Cost	$ 117.65	$ 99.67
	Packaging and Test	$ 32.78	$ 37.43
System Costs	Aggregate Silicon Cost	$ 117.65	$ 99.67
	Relative Silicon Area		105%
	Relative Packaging & Test		114%
	Relative Total Cost		91%
	Total Unit Cost	$ 150.42	$ 137.10

Business Challenges

- ODSA Business Challenge Talks by 9 companies 2023

Company	Presenters	Date
Ventena	Travis Lanier	02/03/2023
Achronix	Nick Ilyadis	02/03/2023
eTopus	Kash	02/10/2023
JCET	Michael Lui	02/10/2023
NXP	Trent Uehling	02/17/2023
ADI	Marek Hempel	02/17/2023
Microchip	Timothy Pezarro	03/03/2023
Marvell	Mark Kuemerle	03/10/2023
AMD	H. Dhavaleswarapu	03/10/2023

White Paper - Chiplet Business Considerations

- **Goal:**
  - Holistic chiplet business case analysis comparison
  - Highlight technical interdependencies

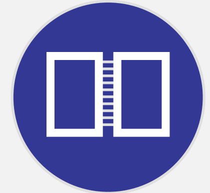
- **Audience:**
  - Businesspeople
  - Product managers
  - System architects

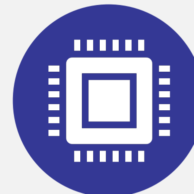
http://tiny.cc/ODSA-Biz-WP-Draft

Whitepaper Chapters

1.Introduction

2. Architecture


3. Interfaces


4. Packaging

5. Testability

6. Cost Structure

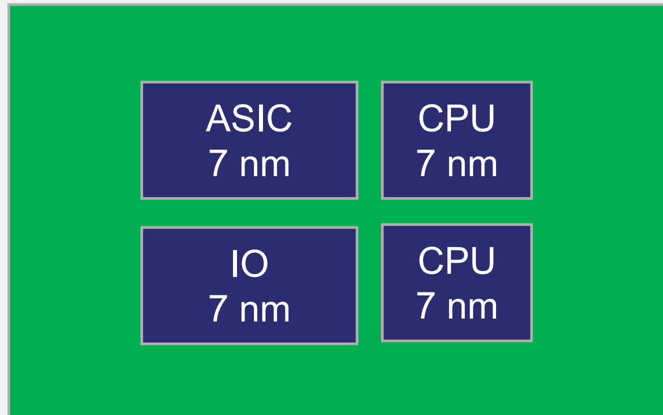
7. Marketplace

8. Standardization

9. Conclusion

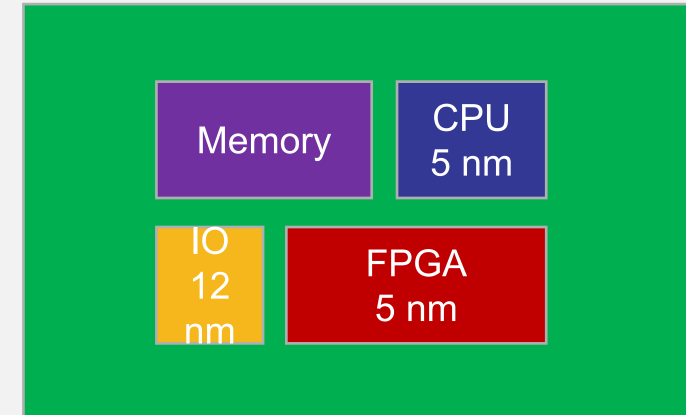
Chiplet Architecture

Homogeneous Design



- **Benefits**
  - Smaller die □ **better yield**
  - No reticle limit □ **build large systems**
- **Often used for**
  - Scalable architectures
  - Very large compute systems

Heterogeneous Design



- **Benefits**
  - Use mature process node □ **lower cost**
  - Use specialized process □ **higher performance**
- **Often used for**
  - Disaggregation by function
  - Splitting analog / digital

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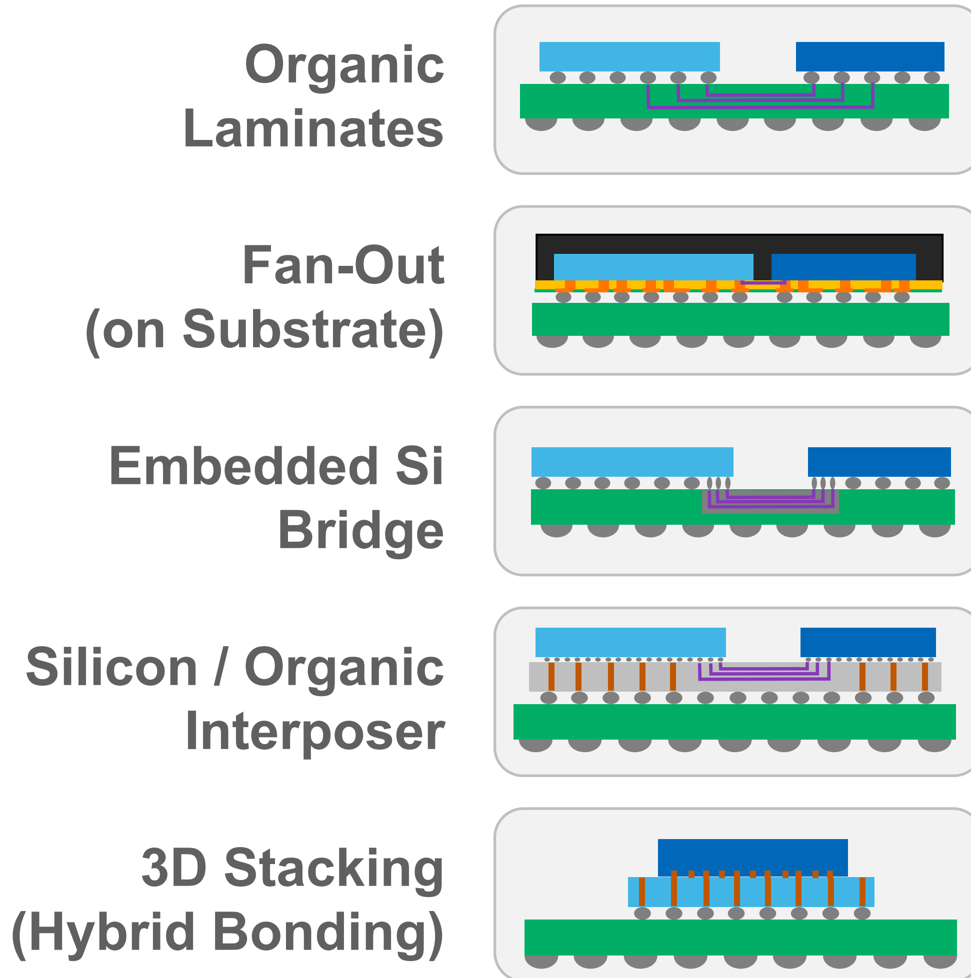
Die-to-Die Interfaces

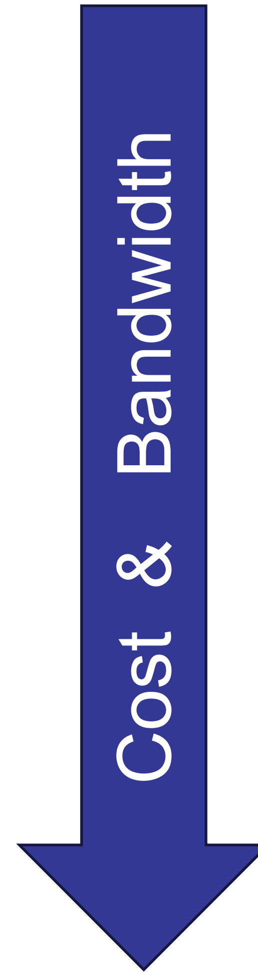
Die-to-Die Interface	Ultra Short Reach SerDes (XSR/USR)	Bunch of Wires (BoW)	Advanced Interface Bus (AIB)	Universal Chiplet Interface (UCIe)
Adoption	Industry standard / in production	~ 10 companies designing with BoW	~ 10x 3rd party chiplets, Intel's chiplets	~120 member companies
Package	Laminate	Laminate, Fan-Out, Interposer	Fan-Out, EMIB, Interposer	Laminate, Fan-Out, EMIB Interposer
Bump Pitch	130-170 µm	45-170 µm	25 - 55 µm	10-130 µm
Lane Rate	112 G / 224 G	2 - 32 Gbps		4 - 32 Gbps
Latency	~10 ns	< 2 ns		< 2 ns
Reach	< 50 mm	< 25 mm	< 25 mm	< 10 mm
Energy	1-4 pJ/bit	0.3-0.5 pJ/bit	0.5-0.8 pJ/bit	0.25-0.5 pJ/bit
Edge Density	< 3 Tbps/mm	< 4 Tbps/mm	< 1.6 Tbps/mm	< 10 Tbps/mm
Link Layer	Not Defined	BoW link layer, supporting AXI, CHI	AXI	Raw, Streaming, PCIe, CXL
Target Applications	Optical Networking	Disaggregation, e.g AI accelerators, automotive	Aerospace & defense ecosystem	Scale & split, system aggregation

- **Performance Metrics**
  - Bandwidth range (Gbps)
  - Beach front (Gbps/mm)
  - PHY footprint (mm^2)
  - Energy (pJ/bit)
  - Latency (ns)
  - Reach (mm)

- **Other Metrics**
  - Package type
  - Associated cost
  - IP availability
  - Adoption
  - Maturity

Chiplet Packaging Options

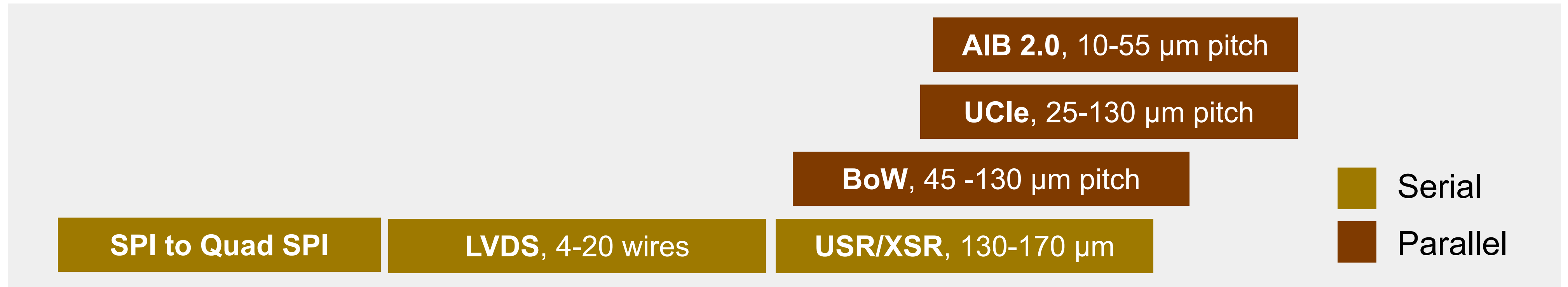


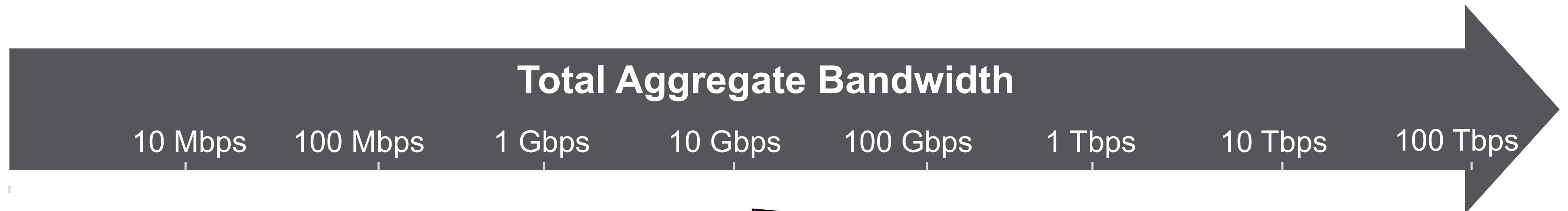


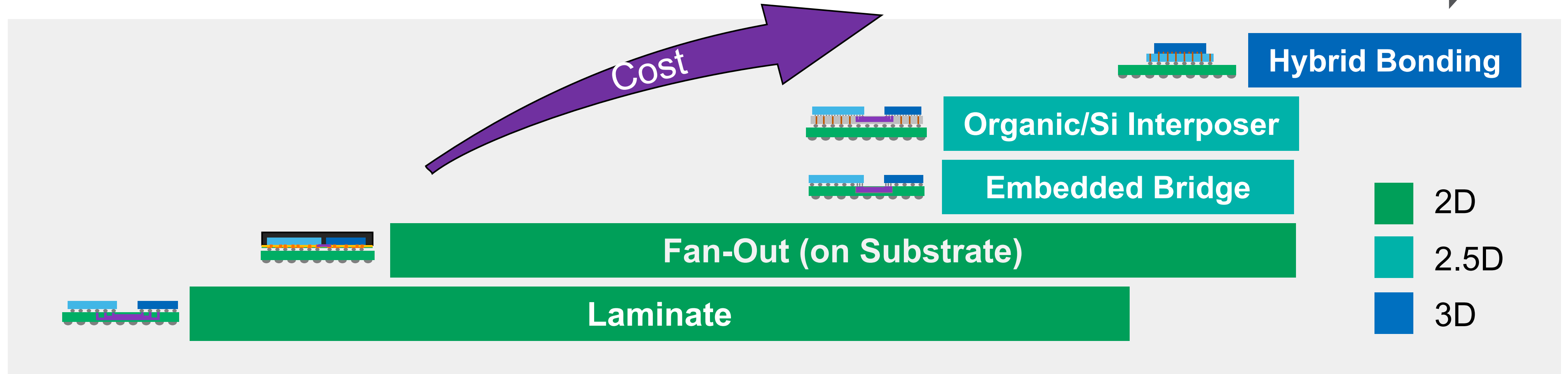
Packages need to match their D2D interfaces

- Bump and escape pitch → via pad, L/S
- Depths of signal bumps → # of layers
- Needed insertion loss → dielectric choice

Packaging and D2D Interface Mapping

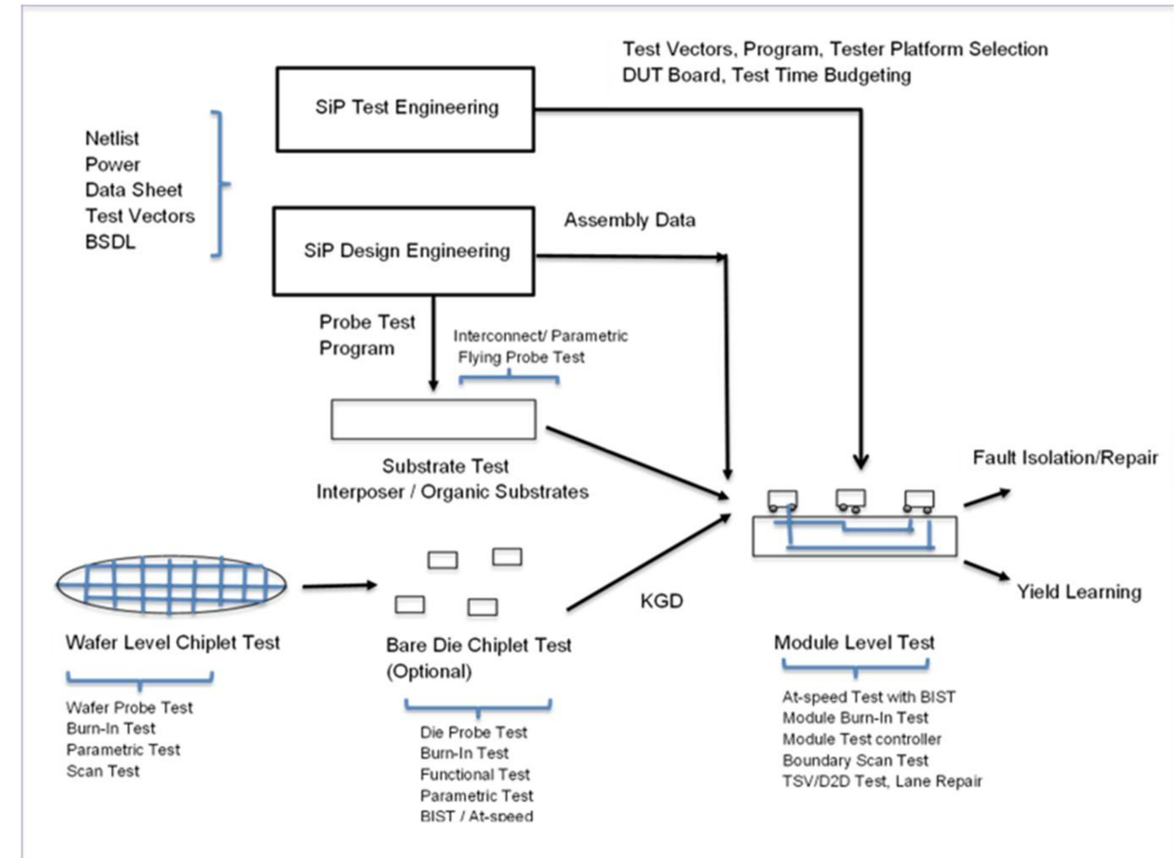






Chiplet Testability

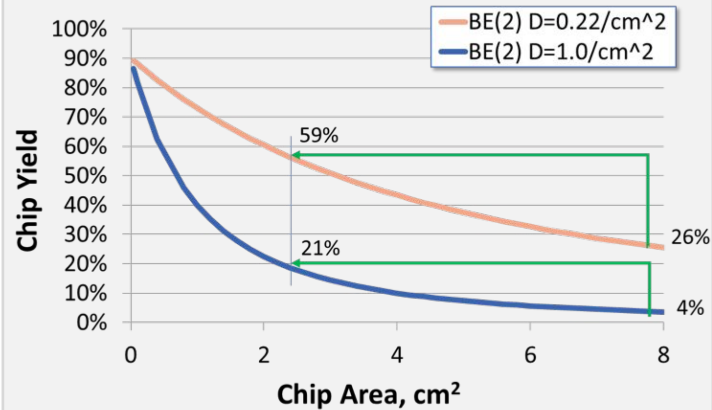
- **Why test?**
  - Lower scrap cost from failing parts
- **Design for Test (DFT)** techniques
  - ATGP, Memory/Logic BIST, Boundary Scan, etc.
  - IEEE 1838 3D test architecture
- **Test points** inserted at various steps, e.g.
  - Wafer probe KGD
  - Substrate test
  - Final test / System Level Test
- **Test Cost** ~ test time * hourly rate / units
  - Rule of thumb: test cost < 20% of die cost
  - Don't spend more than scrap cost savings



Three Financial Benefits of Chiplets

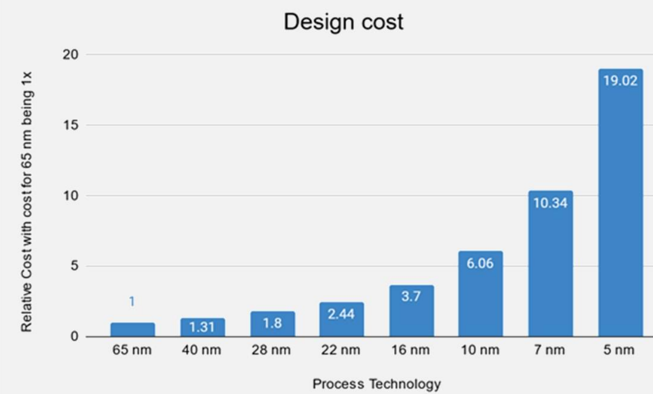
Yield Advantage

- Smaller die have higher yield
- Can off-set higher package, test cost for large systems
- See ODSA cost model



Design Cost Advantage

- Newer processes are more expensive to design on
- Shifting some functions to older nodes reduces cost

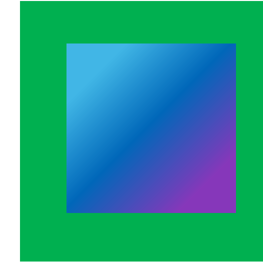


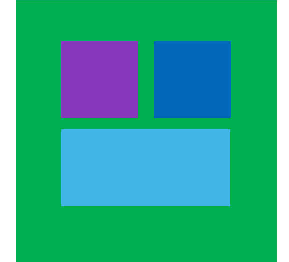
Early Entry Advantage

- Chiplet reuse increases TTM
- This can improve returns by:
  - Higher market share
  - Longer product life-cycle
  - Higher profit margin

Monolithic vs. Chiplet Cost Trends

$$\text{ROI} = \frac{(\text{ASP} - \text{FFC}) \times \text{Units}}{\text{NRE}}$$





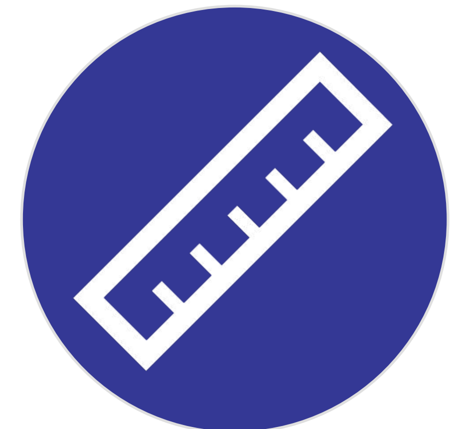
		Monolithic Design	Chiplets Design
Non-Recurring Engineering Cost (NRE)	Chip Design	baseline	less *
	External IP	baseline	similar
	Mask Sets	baseline	depends
Full Factory Cost (FFC)	Silicon Cost	baseline	depends
	Probe	baseline	more
	Package	baseline	more
	Final Test	baseline	similar

* assuming chiplet reuse

Open Chiplet Economy And Standardization

- **Open Chiplet Marketplace is not ready yet**
  - **Interoperability** testing infrastructure not in place for chiplets
  - **Bridge chiplets** could help with interface link-layer incompatibility
  - **Supply chain** like adv. packaging accessibility needs to improve
  - **Getting started** with chiplet requires investment and know-how

- **Standards are key to an Open Chiplet Economy**
  - **Chiplet Design Exchange** group spearheaded several contributions
  - **Standardized chiplet models** to ease system-level integration
  - **Data Exchange format** to describe chiplet properties
  - **Integration workflows** for heterogeneous chiplet systems



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Summary

- Previous work hasn't captured a holistic view of chiplet-based design
- Economically viable chiplet-design depends on technology options
- Chiplet product portfolios have lower NRE through reuse, FFC depends
- 3rd party chiplets market still has its challenges but standards help.

Come Join Us

ODSA Business Group

Fridays, 9-10 am PT

Zoom Link

ODSA Mailing List

Next Projects & Events

Chiplet Business Challenges Workshop
Mar 15th,2024

OCP Chiplet Marketplace

Marek.Hempel@ocproject.org

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Backup

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Chiplet Business Issues by Count

Business

- **6x Cost benefit vs monolithic, cost overhead**
- 3x Product schedule uncertainty, risk
- 2x Up-Front Cost, capability of self-development
- 2x Final Product Responsibility
- 2x Confidential Disclosure

Marketplace

- 3x Third Party Chiplet Availability
- 2x No open marketplace yet

Technical

- **4x D2D Interface Choice**
- 3x Best packaging option std., adv.
- 2x Standardization (Link layer, power, aspect ratio, etc.)