ADAMAS UNIVERSITY

PURSUE EXCELLENCE

KOLKATA

SCHOOL OF ENGINEERING & TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

Bachelor of Computer Application

Course File (Theory)

Course Code: CSE11411

Course Coordinator: Mr. Dipanjan Banerjee

THEORY COURSE FILE CONTENTS

Check list Course Outcomes Attainment

S. No.	Contents	Available (Y/N/NA)	Date of Submission	Signature of HOD
1.	Authenticated Syllabus Copy	Y		
2.	Individual Time Table	Y		
3.	Students' Name List (Approved Copy)	Y		
4.	Course Plan, PO, PSO, COs, CO-PO Mapping, COA Plan, Session Plan and Periodic Monitoring	Y		
5.	Previous Year End Semester Question Papers	Y		
6.	Question Bank (All Units - Part A, Part B & C)	Y		
7.	Dissemination of Syllabus and Course Plan to Students	Y		
8.	Lecture Notes - Unit I, II & III	Y		
9.	**Sample Documents and Evaluation Sheet for Internal Assessment** – Tutorials / Assignments / Class Test / Open Book Test / Quiz / Project / Seminar / Role Play if any (Before Mid Term)	N		
10.	**Mid Term Examination** A. Question Paper / Any Other Assessment Tools Used B. Sample Answer Scripts (Best, Average, Poor) if required C. Evaluation Sheet D. Slow Learners List and Remedial Measures	Y		
11.	Lecture Notes – Unit IV & V	Y		
12.	**Sample Documents and Evaluation Sheet for Internal Assessment** – Tutorials / Assignments / Class Test /Open Book Test / Quiz / Project / Seminar / Role Play if any (After Mid Term)	N		
13.	Course End Survey (Indirect Assessment) & Consolidation	Y		
14.	**End Term Examination** A. Question Paper & Answer Key B. Sample Answer Scripts (Best, Average, Poor) if required C. Evaluation Sheet **D.** Slow Learners List and Remedial Measures.	Y		
15.	Content Beyond the Syllabus (Proof)	NA		
16.	Innovative Teaching Tools Used for TLP	N		
17.	Details of Visiting Faculty Session / Industry Expert / Guest Lecture / Seminar / Field Visit / Webinars /	NA		

	Flipped Class Room / Blended Learning / Online Resources etc.			
18.	Consolidated Mark Statement	Y		
19.	CO Attainment (Mid Term + Internal Assessment + End Term)	Y	09.04.2021	
20.	Gap Analysis & Remedial Measures	Y		
21.	CO - PO Attainment	Y		
22.	Class Record (Faculty Logbook)	Y		

Signature of HOD/ Dean **Signature of Faculty**

Date: **Date:**

1. **Name of the Faculty: Mr. Dipanjan Banerjee**
2. **Course Code : CSE11411**
3. **Course : Computer Organization And Architecture L: 3**
4. **Program : B.C.A T: 0**
5. **Target : 60 %**

P: 0

C: 3

CSE11411	Computer Organization And Architecture	L	T	P	C
Version 1.0	Contact Hour -45	3	0	0	3
Pre-requisites/Exposure	Basic computer Skills				
Co-requisites	--				

Course Objectives:

- To study the basic organization and architecture of digital computers (CPU, memory, I/O, software).
- To Discussions will include digital logic and micro-programming. Such knowledge leads to better understanding and utilization of digital computers, and can be used in the design and application of computer systems or as foundation for more advanced computer-related studies.

Course Outcomes:

On completion of this course, the students will be able to

CO1**. Define** functional block of a computer and relate data representation.
CO2**. Explain** and understand memory hierarchy design, memory access time formula, performance improvement techniques, and trade-offs.
CO3**. Illustrate** pipelined execution, parallel processing and principles of scalable performances.
CO4. **Analyse** the concepts of memory utilization in a computer system.
CO5**. Define** the implementation of parallel processors and Analyse the synchronization techniques

Catalog Description:

The architecture of computer systems and associated software. Topics include addressing modes, interrupt systems, input/output systems, external memory systems, assemblers, loaders, multi-programming, performance evaluation, and data security.

Course Content:

Unit I:

12 lecture hours

Functional blocks of a computer: CPU, memory, input-output subsystems, control unit. Instruction set architecture of a CPU – registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set. Case study – instruction sets of some common CPUs.

Data representation: signed number representation, fixed and floating-point representations, character representation. Computer arithmetic – integer addition and subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift-and-add, Booth multiplier, carry save multiplier, etc. Division restoring and non-restoring techniques, floating point arithmetic.

Unit II: **10 lecture hours**

Introduction to x86 architecture.

CPU control unit design: hardwired and micro-programmed design approaches, Case study – design of a simple hypothetical CPU.

Memory system design: semiconductor memory technologies, memory organization.

Peripheral devices and their characteristics: Input-output subsystems, I/O device interface, I/O transfers – program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes – role of interrupts in process state transitions, I/O device interfaces – SCII, USB

Unit III: **8 lecture hours**

Pipelining: Basic concepts of pipelining, throughput and speedup, pipeline hazards.

Unit IV: **8 lecture hour**

Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies.

Unit V: **7 lecture hours**

Parallel Processors: Introduction to parallel processors, parallel computer models, principles of scalable performances, multiprocessors and multicomputer, message passing mechanism, scalable & Multithreaded dataflow architecture, Concurrent access to memory and cache coherency and synchronization techniques, GPU Processors.

Text Books:

1 "Computer Organization and Design: The Hardware/Software Interface", 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.
2 "Computer Organization and Embedded Systems", 6th Edition by Carl Hamacher, McGraw Hill Higher Education.

Reference Books:

1 "Computer Architecture and Organization", 3rd Edition by John P. Hayes, WCB/McGraw-Hill
2 "Computer Organization and Architecture: Designing for Performance", 10th Edition by William Stallings, Pearson Education.
3 "Computer System Design and Architecture", 2nd Edition by Vincent P. Heuring and Harry F. Jordan, Pearson Education

Modes of Evaluation: Quiz/Assignment/ presentation/ extempore/ Written Examination

Examination Scheme:

Components	Internal Assessment	MTE	ETE
Weightage (%)	30	20	50

Relationship between the Course Outcomes (COs) and Program Outcomes (POs)

Mapping between COs and POs		
	Course Outcomes (COs)	**Mapped Program Outcomes**
CO1	**Define** functional block of a computer and relate data representation.	**PO1,PO3,PO6,PO12,PSO1,PSO3**
CO2	**Explain** and understand memory hierarchy design, memory access time formula, performance improvement techniques, and trade-offs.	**PO1,PO2,PO3,PO6,PO12,PSO1,PSO3**
CO3	**Illustrate** pipelined execution, parallel processing and principles of scalable performances.	**PO1,PO3,PO6,PO11,PO12,PSO1,PSO3,PSO2**
CO4	**Analyse** the concepts of memory utilization in a computer system	**PO1,PO3,PO5,PO6,PO12,PO11,PSO3**
CO5	**Define** the implementation of parallel processors and Analyze the synchronization techniques	**PO1,PO3,PO11,PO6,PO12,PSO1,PSO3**

		Computational Knowledge	Problem analysis	Design/ development of solutions	Conduct investigations of complex problems	Modern tool usage	The engineer and society	Environment and sustainability	Ethics	Individual or team work	Communication	Project management and finance	Life-long Learning	To engage in professional development and to pursue post graduate education in the fields of Information Technology and Computer Applications.	To provide the students about computing principles and business practices in software solutions, outsourcing services, public and private sectors.	Analyze and synthesis computing systems through quantitative and qualitative techniques.
Course Code	Course Title	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CSE 11411	Computer Organization & Architecture	3	2	3	-	2	3	-	-	-	-	-	3	3	2	3

1=weakly mapped
2= moderately mapped
3=strongly mapped

Faculty Individual Time Table

ADAMAS UNIVERSITY, KOLKATA
SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
Programme: B.C.A
Course Code CSE11411 , Course Name: Computer Organization & Architecture Faculty Coordinator: Mr. Dipanjan Banerjee

Day & Time	09.30 - 10.25	10.30 – 11.25	11.30-12.25	12.30-1.30	1.30-2.25	2.30-3.25	3.30-4.25	4.30-5.25
Monday	CoA			LUNCH		CoA(T)		
Tuesday		CoA						
Wednesday								
Thursday		CoA						
Friday								

Signature of HOD **Signature of Class Coordinator**

Date: **Date:**

Students Name List

Full Name	Registration Number	Roll Number
DEBOJYOTI SAHA	AU/2020/0004253	UG/02/BCA/2020/001
AZMAT ALI	AU/2020/0004290	UG/02/BCA/2020/002
SATYAJIT GHOSH	AU/2020/0004448	UG/02/BCA/2020/003
DEBDYUTI DAS	AU/2020/0004449	UG/02/BCA/2020/004

SAYANTAN JANA	AU/2020/0004453	UG/02/BCA/2020/005
SANJUKTA JANA	AU/2020/0004457	UG/02/BCA/2020/006
AYAN RAHAMAN	AU/2020/0004458	UG/02/BCA/2020/007
SUSOVON NANDY	AU/2020/0004461	UG/02/BCA/2020/008
ANWESHA PRAMANIK	AU/2020/0004483	UG/02/BCA/2020/011
Anthony Prakash Rozario	AU/2020/0004498	UG/02/BCA/2020/015
MOUSUMI DUTTA	AU/2020/0004501	UG/02/BCA/2020/016
Dhrubajyoti Dey	AU/2020/0004504	UG/02/BCA/2020/017
Pritam Hore	AU/2020/0004507	UG/02/BCA/2020/018
Aratrika Bose	AU/2020/0004509	UG/02/BCA/2020/019
Tithi Paul	AU/2020/0004510	UG/02/BCA/2020/020
Arpan Mondal	AU/2020/0004513	UG/02/BCA/2020/021
Parichoy nandi	AU/2020/0004514	UG/02/BCA/2020/022
Aditya Jaman	AU/2020/0004515	UG/02/BCA/2020/023
Aparesh Muhuri	AU/2020/0004517	UG/02/BCA/2020/024
Kosturi Mondal	AU/2020/0004520	UG/02/BCA/2020/025
Aritra Das	AU/2020/0004522	UG/02/BCA/2020/026
RISHI BARUA	AU/2020/0004525	UG/02/BCA/2020/027
Neelash Saha	AU/2020/0004526	UG/02/BCA/2020/028
Bittaswer Ghosh	AU/2020/0004533	UG/02/BCA/2020/029

SUNEET CHOUDHARY	AU/2020/0004535	UG/02/BCA/2020/030
Abhishek Tarafdar	AU/2020/0004543	UG/02/BCA/2020/031
Ayon Chakraborty	AU/2020/0004547	UG/02/BCA/2020/032
JYOTISHKA DE	AU/2020/0004552	UG/02/BCA/2020/033
Asmat Sk	AU/2020/0004564	UG/02/BCA/2020/034
Nikhil Kumar Sah	AU/2020/0004575	UG/02/BCA/2020/035
Suprita Nandy	AU/2020/0004582	UG/02/BCA/2020/036
Oliva Dutta	AU/2020/0005526	UG/02/BCA/2020/037
Somnath Gayen	AU/2020/0004505	UG/02/BCABFSI/2020/001
BARUN RAJBHAR	AU/2020/0004598	UG/02/BCABFSI/2020/002
RAKIBUL ISLAM	AU/2020/0004605	UG/02/BCABFSI/2020/003
Swapnil Mitra	AU/2020/0004492	UG/02/BCABFSI/2020/004
SWARNAMOY GHOSH	AU/2020/0004482	UG/02/BCABFSI/2020/005
Susmit Shaw	AU/2020/0004493	UG/02/BCAGA/2020/001
Arka Mitra	AU/2020/0004500	UG/02/BCAGA/2020/002
Sourav Mondal	AU/2020/0004524	UG/02/BCAGA/2020/003
Ranita Bagchi	AU/2020/0004539	UG/02/BCAGA/2020/004
SUBHAJIT SIRCAR	AU/2020/0004568	UG/02/BCAGA/2020/005
Abhishek Mondal	AU/2020/0004497	UG/02/BCAGA/2020/006
Hritankar Das	AU/2020/0004478	UG/02/BCAGA/2020/007

Suman Ghosh	AU/2020/0004496	UG/02/BCAGA/2020/008

Signature of HOD/Dean **Signature of Class Coordinator**

Date: **Date:**

COURSE PLAN

Target	60% (marks)
Level-1	50% (population)
Level-2	60% (population)
Level-3	70% (population)

6. Method of Evaluation

UG	PG
Internal Assessment (30%) (Quizzes/Tests, Assignments & Seminars etc.)	Internal Assessment (30%) (Quizzes/Tests, Assignments & Seminars etc.)
Mid Semester Examination (20%)	Mid Semester Examination (20%)
End Semester Examination (50%)	End Semester Examination (50%)

*Keep as per Program (UG/PG)

7. Passing Criteria

Scale	PG	UG
Out of 10 Point Scale	CGPA – "5.00" Min. Individual Course Grade – "C" Passing Minimum – 40	CGPA – "5.00" Min. Individual Course Grade – "C" Passing Minimum – 35

*Keep as per Program (UG/PG)

8. Pedagogy

- **Direct Instruction**
- Kinesthetic Learning
- **Flipped Classroom**
- Differentiated Instruction
- Expeditionary Learning
- Inquiry Based Learning
- Game Based Learning
- Personalized Learning

9. Topics introduced for the first time in the program through this course

- (New Topics Related to this Course – Syllabus Revision if any/Content Beyond Syllabus)

10. References:

Text Books	Web Resources	Journals	Reference Books
5	4	2	9

Signature of HOD/Dean **Signature of Faculty**

GUIDELINES TO STUDY THE SUBJECT

Instructions to Students:

1. Go through the 'Syllabus' in the LMS in order to find out the Reading List.
2. Get your schedule and try to pace your studies as close to the timeline as possible.
3. Get your on-line lecture notes (Content, videos) at Lecture Notes section. These are our lecture notes. Make sure you use them during this course.
4. check your LMS regularly.
5. go through study material

6. check mails and announcements on blackboard
7. keep updated with the posts, assignments and examinations which shall be conducted on the blackboard
8. Be regular,so that you do not suffer in any way
9. C**ell Phones and other Electronic Communication Devices:** Cell phones and other electronic communication devices (such as Blackberries/Laptops) are not permitted in classes during Tests or the Mid/Final Examination. Such devices MUST be turned off in the class room.
10. **E-Mail and online learning tool:** Each student in the class should have an e-mail id and a pass word to access the LMS system regularly. Regularly, important information – Date of conducting class tests, guest lectures, via online learning tool. The best way to arrange meetings with us or ask specific questions is by email and prior appointment. All the assignments preferably should be uploaded on online learning tool. Various research papers/reference material will be mailed/uploaded on online learning platform time to time.
11. **Attendance:** Students are required to have minimum attendance of 75% in each subject. Students with less than said percentage shall NOT be allowed to appear in the end semester examination.

This much should be enough to get you organized and on your way to having a great semester! If you need us for anything, send your feedback through e-mail dipanjan.banerjee@adamasuniversity.ac.in Please use an appropriate subject line to indicate your message details.

There will no doubt be many more activities in the coming weeks. So, to keep up to date with all the latest developments, please keep visiting this website regularly.

RELATED OUTCOMES

1. The expected outcomes of the Program are:

PO1	**Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering Fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem Analysis:** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/ Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct Investigations of Complex Problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
PO6	**The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and Sustainability:** Understand the impact of professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and Team Work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively in complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and multidisciplinary environments.
PO12	**Life-Long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

2. The expected outcomes of the Specific Program are: (up to 3)

PSO1	Engage in analysis and design of various power system components and their applications in the field of Electrical Engineering.
PSO2	Apply the domain knowledge of Electrical Engineering to solve problems for development of society, and/ or pursue higher education and research.
PSO3	Engage in lifelong learning and adapt to changing professional and societal needs.

3. The expected outcomes of the Course are: (minimum 4 and maximum 6)

CO1	Define functional block of a computer and relate data representation.
CO2	Explain and understand memory hierarchy design, memory access time formula, performance improvement techniques, and trade-offs.
CO3	Illustrate pipelined execution, parallel processing and principles of scalable performances.
CO4	Analyze the concepts of memory utilization in a computer system.
CO5	Define the implementation of parallel processors and Analyse the synchronization techniques

4. Co-Relationship Matrix

Indicate the relationships by 1- Slight (Low) 2- Moderate (Medium) 3-Substantial (High)

Program Outcomes / Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	-	3	2	-	-	-	-	-	-	-	-	-	3	-	-
CO3	-	2	-	-	-	3	-	-	-	-	-	-	3	-	-
CO4	2	-	3	-	-	3	-	-	-	-	-	-	-	-	-
CO5	2	-	2	-	-	3	-	-	-	-	-	3	-	-	-
Average	**2**	**2**	**2**	**-**	**-**	**3**	**-**	**-**	**-**	**-**	**-**	**3**	**3**	**-**	**-**

5. Course Outcomes Assessment Plan (CA):

Course Outcomes	Internal Assessment* (30 Marks)		Mid Term Exam (20 Marks)	End Term Exam (50 Marks)	Total (100 Marks)
	Before Mid Term	After Mid Term			
CO1	7	NA	9	16	7
CO2	8	NA	8	16	8
CO3	5	4	7	16	5
CO4	5	5	10	20	5
CO5	NA	7	9	16	NA
Total	14	16	20	50	100

* Internal Assessment – Tools Used: Tutorial, Assignment, Seminar, Class Test etc.

OVERVIEW OF COURSE PLAN OF COURSE COVERAGE

Course Activities:

S. No.	Description	Planned			Actual			Remarks
		From	To	No. of Session	From	TO	No. of Session	
1.	Functional blocks of a computer & Data Representation	01/09/2021	12/10/2021	12	01/09/2021	12/10/2021	12	Completed As per Plan
2.	Instruction Set Architecture	15/10/2021	24/12/2021	17	15/10/2021	24/12/2021	17	Completed As per Plan
3.	Memory Organization	04/01/2022	25/02/2022	12	04/01/2022	25/02/2022	12	Completed As per Plan
4.	Cache Coherence Policies	01/09/2022	12/10/22	12	01/09/22	12/10/22	12	Completed As per Plan
5.	I/O Organization	13/10/2021	24/11/2021	12	13/10/2021	24/11/2021	12	Completed As per Plan
6.	Instruction Pipeline	01/12/2021	04/01/2022	8	01/12/2021	04/01/2022	8	Completed As per Plan
7.	Revision & Doubt Clearing Classes	19/01/2022	01/03/2022	8	19/01/2022	01/03/2022	8	Completed As per Plan

Total No. of Instructional periods available for the course: 81 Sessions

Signature of HOD/Dean **Signature of Faculty**

Date: **Date:**

SESSION PLAN
UNIT-I

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	03.09.2021	Basic Concept of Computer Organization & Architecture	CO1	1	03.09.2020	Basic Concept of Computer Organization & Architecture	CO1
2	07.09.2021	Basic Concept of CPU	CO1	2	07.09.2020	Basic Concept of CPU	CO1
3	10.09.2021	Basic Concept of Memory	CO1	3	10.09.2020	Basic Concept of Memory	CO1
4	14.09.2021	Input-Output Subsystems, Control Unit	CO1	4	14.09.2020	Input-Output Subsystems, Control Unit	CO1
5	17.09.2021	Instruction Set Architecture Of A CPU	CO1	5	17.09.2020	Instruction Set Architecture Of A CPU	CO1
6	21.09.2021	Addressing Modes	CO1	6	21.09.2020	Addressing Modes	CO1
7	24.09.2021	Instruction Set	CO1	7	24.09.2020	Instruction Set	CO1
8	28.09.2021	Data Representation	CO1	8	28.09.2020	Data Representation	CO1
9	01.10.2021	Floating Point And Character Representation	CO1	9	01.10.2020	Floating Point And Character Representation	CO1
10	05.10.2021	Computer Arithmetic	CO1	10	05.10.2020	Computer Arithmetic	CO1
11	08.10.2021	Booth Multiplier, Carry Save Multiplier, Division Algorithm	CO1	11	08.10.2020	Booth Multiplier, Carry Save Multiplier, Division Algorithm	CO1

12	12.10.2021	Floating Point Arithmetic.	CO1	12	12.10.2020	Floating Point Arithmetic.	CO1

Remarks:

Signature of Faculty

Date:

SESSION PLAN
UNIT-II

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	15.10.2021	Introduction to x86 Architecture	CO 2	1	15.10.2020	Introduction to x86 Architecture	CO 2
2	19.10.2021	CPU Control Unit Design	CO 2	2	19.10.2020	CPU Control Unit Design	CO 2
3	29.10.2021	Hardwired And Micro-Programmed Design Approaches	CO 2	3	29.10.2020	Hardwired And Micro-Programmed Design Approaches	CO 2
4	02.11.2021	Simple Hypothetical CPU Design	CO 2	4	02.11.2020	Simple Hypothetical CPU Design	CO 2
5	05.11.2021	Memory System Design	CO 2	5	05.11.2020	Memory System Design	CO 2
6	09.11.2021	Semiconductor Technologies in Memory Design	CO 2	6	09.11.2020	Semiconductor Technologies in Memory Design	CO 2
7		Peripheral Devices And Their Characteristics	CO 2	7		Peripheral Devices And Their Characteristics	CO 2
8		Input-Output Subsystems	CO 2	8		Input-Output Subsystems	CO 2
9		I/O Device Interface	CO 2	9		I/O Device Interface	CO 2
10		I/O Transfers	CO 2	10		I/O Transfers	CO 2
11		Program Controlled, Interrupt Driven And DMA	CO 2	11		Program Controlled, Interrupt Driven And DMA	CO 2
12		Privileged And Non-Privileged Instruction	CO 2	12		Privileged And Non-Privileged Instruction	CO 2

13		Software Interrupts And Exceptions	CO 2	13		Software Interrupts And Exceptions	CO 2
14		Role Of Interrupts In Process State Transitions	CO 2	14		Role Of Interrupts In Process State Transitions	CO 2
15		I/O Device Interfaces	CO 2	15		I/O Device Interfaces	CO 2
16		SCII	CO 2	16		SCII	CO 2
17		USB	CO 2	17		USB	CO 2

Remarks:

Signature of Faculty

Date:

SESSION PLAN
UNIT-III

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics to be Covered	CO Achieved
1		Basic concept of Pipelining	CO3	1		Basic concept of Pipelining	CO3
2		Basic Functional Units	CO3	2		Basic Functional Units	CO3
3		Asynchronous Pipeline	CO3	3		Asynchronous Pipeline	CO3
4		Synchronous Pipeline	CO3	4		Synchronous Pipeline	CO3
5		Hazards	CO3	5		Hazards	CO3
6		Data Hazards	CO3	6		Data Hazards	CO3
7		Control Hazards	CO3	7		Control Hazards	CO3
8		Structural Hazards	CO3	8		Structural Hazards	CO3
9		Hazard Avoidance	CO3	9		Hazard Avoidance	CO3
10		Branch Prediction	CO3	10		Branch Prediction	CO3
11		Conditional Branch	CO3	11		Conditional Branch	CO3
12		Cache Memory Involvements & Problems.	CO3	12		Cache Memory Involvements & Problems.	CO3

Remarks: **Signature of Faculty**

Date:

SESSION PLAN
UNIT-IV

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics to be Covered	CO Achieved
1		Key Characteristics of a memory	CO4	1		Key Characteristics of a memory	CO4
2		Memory Hierarchy	CO4	2		Memory Hierarchy	CO4
3		Instruction & Data Storage	CO4	3		Instruction & Data Storage	CO4
4		Static & Dynamic RAM Technologies	CO4	4		Static & Dynamic RAM Technologies	CO4
5		Understand the Read & Write Performances	CO4	5		Understand the Read & Write Performances	CO4
6		Virtual Memory Technology	CO4	6		Virtual Memory Technology	CO4
7		TLB, Paging & Segmentation	CO4	7		TLB, Paging & Segmentation	CO4
8		Cache Memory Organization	CO4	8		Cache Memory Organization	CO4
9		Direct & Associative Mapping	CO4	9		Direct & Associative Mapping	CO4
10		Set Associative Mapping	CO4	10		Set Associative Mapping	CO4
11		Page Replacement Policies	CO4	11		Page Replacement Policies	CO4
12		Cache Performance Issues	CO4	12		Cache Performance Issues	CO4

13		Cache Coherence	CO4	13		Cache Coherence	CO4
14		Instruction & Data Cache	CO4	14		Instruction & Data Cache	CO4
15		Consequences for the Programmers	CO4	15		Consequences for the Programmers	CO4
16		Shared Memory Organization	CO4	16		Shared Memory Organization	CO4
17		Demand Paging	CO4	17		Demand Paging	CO4
18		Address Translation Scheme	CO4	18		Address Translation Scheme	CO4
19		Page Table storage & Paging Efficiency	CO4	19		Page Table storage & Paging Efficiency	CO4
20		Segmentation & Base of Virtual memory protection	CO4	20		Segmentation & Base of Virtual memory protection	CO4

Remarks:

Signature of Faculty
Date:

SESSION PLAN
UNIT-V

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1		Introduction to parallel processors	CO5	1		Introduction to parallel processors	CO5
2		Parallel computer models	CO5	2		Parallel computer models	CO5
3		Principles of salable performances,	CO5	3		Principles of scalable performances,	CO5
4		Multiprocessors	CO5	4		Multiprocessors	CO5
5		Multi computer	CO5	5		Multicomputer	CO5
6		Message passing mechanism	CO5	6		Message passing mechanism	CO5
7		Scalable & Multithreaded dataflow architecture	CO5	7		Scalable & Multithreaded dataflow architecture	CO5
8		Concurrent access to memory	CO5	8		Concurrent access to memory	CO5
9		Cache coherency	CO5	9		Cache coherency	CO5
10		Synchronization techniques & , GPU Processors	CO5	10		Synchronization techniques & , GPU Processors	CO5

Remarks:

Signature of Faculty
Date:

PERIODIC MONITORING

Actual date of completion and remarks, if any

Components		From	To	From	To
Duration (Mention from and to Dates)		01.09.2020	23.11.2020	24.11.2020	28.02.2021
Percentage of Syllabus covered		55 %		45 %	
Lectures	Planned	1	45	46	81
	Taken	1	45	46	81
Tutorials	Planned	NA			
	Taken				
Test/Quizzes/ Mid Semester/ End Semester	Planned	01.09.2020	28.11.2020	24.11.2020	22.02.2021
	Taken	01.09.2020	28.11.2020	24.11.2020	22.02.2021
	CO's Addressed	CO1, CO2, CO3	CO1, CO2, CO3	CO4, CO5	CO4, CO5
	CO's Achieved	CO1, CO2, CO3	CO1, CO2, CO3	CO4, CO5	CO4, CO5
Assignments	Planned	2	2	2	2
	Taken	2	2	2	2
	CO's Addressed	CO1, CO2, CO3	CO1, CO2, CO3	CO4, CO5	CO4, CO5
	CO's Achieved	CO1, CO2, CO3	CO1, CO2, CO3	CO4, CO5	CO4, CO5
Signature of Faculty					
Head of the Department					
OBE Coordinator					

Signature of HOD/ Dean

Date

Signature of Faculty

Date

PERIODIC MONITORING

Attainment of the Course (Learning) Outcomes:

Components	Attainment level	Action Plan	Remarks
Assignment	CO1:	Submission Target	
	CO2:		
	CO3:		
	CO4:		
	CO5:		
	CO6:		
Quiz/Test etc.	CO1:	Conducted on	
	CO2:		
	CO3:	Conducted on	
	CO4:	Conducted on	
	CO5:		
	CO6:	Conducted on	
Mid Semester	CO1:	Scheduled on	
	CO2:		
	CO3:	--	
	CO4:	Scheduled on	
	CO5:	--	
	CO6:	--	
End Semester	CO1:	Scheduled on	
	CO2:		
	CO3:		
	CO4:		
	CO5:		
	CO6:		
Any Other	CO1:	NA	
	CO2:		
	CO3:		
	CO4:		
	CO5:		
	CO6:		

Signature of HOD/ Dean
Date

Signature of Faculty
Date

Previous Year Question Papers – Set 1

	ADAMAS UNIVERSITY **END SEMESTER EXAMINATION** (Academic Session: 2020 – 21)		
Name of the Program:	MCA	**Semester:**	I
Paper Title:	Computer Organization & Architecture	**Paper Code:**	ECS51143
Maximum Marks:	50	**Time Duration:**	3 Hrs
Total No. of Questions:	**17**	**Total No of Pages:**	3
(Any other information for the student may be mentioned here)	**1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

	Group A **Answer All the Questions (5 x 1 = 5)**		
1	A source program is usually in _____ a) Assembly language b) Machine level language c) High-level language d) Natural language	**R**	**CO1**
2	Which memory device is generally made of semiconductors? a) RAM b) Hard-disk c) Floppy disk d) Cd disk	**R**	**CO2**
3	The small extremely fast, RAM's are called as _____	**R**	**CO3**
4	The ALU makes use of _____ to store the intermediate results. a) Accumulators b) Registers c) Heap d) Stack	**R**	**CO4**
5	The control unit controls other units by generating ____ a) Control signals b) Timing signals c) Transfer signals d) Command Signals	**R**	**CO5**
	Group B **Answer Allthe Questions (5 x 2 = 10)**		
6 a)	Let us assume that a complete execution of a program requires the execution of 100 machine language instruction. Some instructions may be executed more than once when they are inside loop, So we can assume that the average	**AP**	**CO1**

	no of basic steps needed to execute one basic instruction is 7, such that each and every basic step completes in 1 clock cycle. If a 10 Hz – processor is used then calculate time required by the processor to execute the program.		
	(OR)		
6 b)	What is Processor clock.	**R**	**CO1**
7 a)	Explain the role of each and every stage of a four stage general pipeline.	**U**	**CO2**
	(OR)		
7 b)	What are the different types of hazards that can occur in a pipeline?	**R**	**CO2**
8 a)	What do you understand by byte addressability.	**R**	**CO3**
	(OR)		
8 b)	Discuss the basic functional units of a computer.	**U**	**CO3**
9 a)	Write the instruction sequences for push mechanism in Stack.		**CO4**
	(OR)		
9 b)	Write the instruction sequences for pop mechanism in Stack.	**R**	**CO4**
10 a)	Explain different formats of instructions with example.	**U**	**CO5**
	(OR)		
10 b)	What do you understand by effective address of an operand and explain how it is calculated.	**R**	**CO5**
	Group C **Answer All the Questions (7 x 5 = 35)**		
11 a)	Design an algorithm for division along with the flowchart.	**An**	**CO1**
	(OR)		
11 b)	Represent each and every step for dividing 4 by 2 using division algorithm.	**An**	**CO1**
12 a)	Generate the3-Address and 1-Address Instruction sequence for the following expression $X = \frac{(a+b)}{4} + \frac{(c+5)\times d}{2}$	**Ap**	**CO2**
	(OR)		
12 b)	Generate the 2-Address and Zero address Instruction sequence for the following expression $X = \frac{\left(\frac{a}{2}+\frac{b}{e}\right)}{4} + \frac{\left(\frac{c}{3}+5\right)\times d}{2}$	**AP**	**CO2**
13 a)	Explain the working principle of a synchronous bus for input operation with timing diagram.	**U**	**CO3**
	(OR)		
13 b)	What is an interupt and how it is processed	**R**	**CO3**
14 a)	Discuss with with diagram the working principle of a peripheral device	**U**	**CO4**
	(OR)		
14 b)	Discuss the process by which input is taken from a keyboard.	**U**	**CO4**
15 a)	What is Instruction Pipeline. What are the reasons for data hazard? Give a solution for data hazard. A Pipelined processor has 4 stages, Fetch, Decode, Execute, Write Back. Fetch, Decode and Write Back stage takes 1 clock cycle for each and every instructions and for Execution stage it depends on the Instruction. Addition and Subtraction instruction takes 1 clock cycle and Multiplication Instruction takes 3 clock cycles. The Instructions are $I_1 : ADD R_2 R_1 R_0$ I_2 : MUL $R_4 R_3 R_2$	**E**	**CO4**

<table>
<tr><td></td><td>I_3 : SUB R_5 R_4 R_2
Calculate the total number of clock cycles required to complete the execution of above Instruction sequence in-
<u>Case1</u>: Without data forwarding and <u>Case2</u>: With data forwarding.</td><td></td><td></td></tr>
<tr><td colspan="4">(OR)</td></tr>
<tr><td>15 b)</td><td>A 4-Stage asynchronous pipelined processor with Fetch, Decode, Execute & Write Back Stages with an instruction sequence with respective clock cycles for every stages is displayed below:
<table><tr><th></th><th>IF</th><th>ID</th><th>EX</th><th>WB</th></tr><tr><td>I_1</td><td>2</td><td>1</td><td>1</td><td>1</td></tr><tr><td>I_2</td><td>1</td><td>3</td><td>2</td><td>2</td></tr><tr><td>I_3</td><td>1</td><td>1</td><td>1</td><td>3</td></tr><tr><td>I_4</td><td>1</td><td>2</td><td>2</td><td>2</td></tr></table>Calculate the number of clock cycles needed to execute the loop [for(i=0;i<=2;i++){I_1;I_2;I_3;I_4;}]. State briefly the mechanism of processing Instructions in every stages.</td><td>E</td><td>CO4</td></tr>
<tr><td>16 a)</td><td>Discuss the Internal Organization of the bit cells in a memory chip with diagram.</td><td>An</td><td>CO5</td></tr>
<tr><td colspan="4">(OR)</td></tr>
<tr><td>16 b)</td><td>State the working principle of a CMOS Static RAM cell</td><td>C</td><td>CO5</td></tr>
<tr><td>17 a)</td><td>The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, what will be the length (in number of bits) of the tag field.</td><td>E</td><td>CO5</td></tr>
<tr><td colspan="4">(OR)</td></tr>
<tr><td>17 b)</td><td>A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. What do you mean by 4-way set associative cache(with diagram)? Calculate the number of bits in every required field in an address to access the cache memory and the size of the cache tag directory.</td><td>E</td><td>CO5</td></tr>
</table>

Previous Year Question Papers – Set 2

ADAMAS UNIVERSITY

END SEMESTER EXAMINATION

(Academic Session: 2020 – 21)

Name of the Program:	MCA	**Semester:**	I
Paper Title:	Computer Organization & Architecture	**Paper Code:**	ECS51143
Maximum Marks:	50	**Time Duration:**	3 Hrs
Total No. of Questions:	**17**	**Total No of Pages:**	3
(Any other information for the student may be mentioned here)	**1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

Group A
Answer All the Questions (5 x 1 = 5)

1	What does RTN stands for _____ a) Register Transfer Notation b) Register Transmission Notation c) Regular Transmission Notation d) Regular Transfer Notation	**R**	**CO1**
2	Name the two phases of executing an instruction are _____ a) Instruction decoding and storage b) Instruction fetch and instruction execution c) Instruction execution and storage d) Instruction fetch and Instruction processing	**R**	**CO2**
3	Show the RTN of the instruction, Add R1,R2,R3 a) $R3 = R1 + R2 + R3$ b) $R3 \leftarrow [R1] + [R2] + [R3]$. c) $R3 = [R1] + [R2]$. d) $R3 \leftarrow [R1] + [R2]$.	**R**	**CO3**
4	Which is the smallest entity of memory is called _____ a) Cell b) Block c) Instance d) Unit	**R**	**CO4**
5	The instruction, Add #45,R1 does _____ a) Adds the value of 45 to the address of R1 and stores 45 in that address b) Adds 45 to the value of R1 and stores it in R1	**R**	**CO5**

	c) Finds the memory location 45 and adds that content to that of R1 d) None of the mentioned		
Group B Answer All the Questions (5 x 2 = 10)			
6 a)	What is Programmed I/O and Memory Mapped I/O?	**R**	**CO1**
(OR)			
6 b)	Explain the properties of memory hierarchy.	**U**	**CO1**
7 a)	What do you mean by Bus Cycle?	**R**	**CO2**
(OR)			
7 b)	What is Instruction Pipeline and what is its necessity.	**R**	**CO2**
8 a)	State the main difference between computer organization & architecture.	**U**	**CO3**
(OR)			
8 b)	State the overflow conditions for signed magnitude arithmetic operations	**Analyze**	**CO3**
9 a)	What do you mean by subroutine?	**R**	**CO4**
(OR)			
9 b)	What do you mean by branching?	**R**	**CO4**
10 a)	What is locality of reference	**R**	**CO5**
(OR)			
10 b)	Construct the 2-Address &1-Address m/c instruction sequences for the following expression: $X = \frac{(A+B)(4+7)}{\frac{C+D}{5}}$	**App**	**CO5**
Group C Answer All the Questions (7 x 5 = 35)			
11 a)	Discuss address assignment scheme. State five differences between computer organization and computer architecture	**C**	**CO1**
(OR)			
11 b)	Explain Indirect and Indexed Addressing modes and its necessity with example.	**U**	**CO1**
12 a)	Explain with diagram the working principle of Static-RAM & Dynamic-RAM cells.	**U**	**CO2**
(OR)			
12 b)	The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, what will be the length (in number of bits) of the tag field	**Analyze**	**CO2**
13 a)	State Booth's Algorithm for 2's complement multiplication along with the flowchart.	**C**	**CO3**
(OR)			
13 b)	Recomend each and every step for multiplying 6 and (-6) using booths multiplication algorithm	**E**	**CO3**
14 a)	Calculate the hit ratio and miss ratio of a computer with a direct mapped cache with 8 cache blocks (0-7). If the memory block requests are in the order-	**E**	**CO4**

	3, 5, 2, 8, 0, 6, 3, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24 Which of the following memory blocks will not be in the cache at the end of the sequence? What is conflict miss. State with diagram how a ROM cell stores information		
	(OR)		
14 b)	What do you understand by a fully associative cache explain with diagram. Calculate the hit ratio and miss ratio for LRU and FIFO replacement policy implemented on a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order- 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7 If LRU replacement policy is used, which cache block will have memory block 7?	**E**	**CO4**
15 a)	Discuss briefly the Indirect addressing mode and its importance.	**U**	**CO4**
	(OR)		
15 b)	Discuss briefly the Indexed addressing mode and its importance.	**U**	**CO4**
16 a)	What is an Interrupt. Explain briefly with flowchart how interrupt is processed.	**U**	**CO5**
	(OR)		
16 b)	State the necessity of an I/O module with diagram.	**Ana**	**CO5**
17 a)	Explain how data transfer takes place using Handshaking Protocol for Input and Output operation for asynchronous bus with the help of timing diagram.	**U**	**CO5**
	(OR)		
17 b)	State the working principle of a DMA Controller.	**E**	**CO5**