FPGA Assignment: UP–DOWN Counter + TIMER Circuit

Platform: Altera DE2-70 FPGA board

Project Goal

Design and implement a digital **UP–DOWN counter with a timer function** on the DE2-70 FPGA board, Fig. 1. Use the board's **switches (SW)** and **keys (KEY)** to control the operation according to the following specifications.

Functional Description

1. **Timer Duration Control**
   - **Switch group A (SW A):**
     Sets the **duration** of the timer signal — this represents either:
     - Whole seconds, or
     - Tenths of a second (0.1 s)
   - **Switch B (SW B):**
     Selects the **time unit** for the duration set by SW A:
     - `0` → duration in **seconds**
     - `1` → duration in **seconds / 10**
2. **Counting Direction**
   - **Switch C (SW C):**
     Determines counting direction:
     - `0` → **Up-counting**
     - `1` → **Down-counting**
3. **Counter Enable**
   - **Switch D (SW D):**
     Acts as the **enable (gate)** control for the counter:
     - `1` → Counter active
     - `0` → Counter stopped
4. **Timer Trigger and Reset**
   - **KEY A:**
     One-shot trigger — starts the timer once when pressed.
   - **KEY B:**
     Reset — clears the counter and timer, returning the circuit to its initial state.
5. **Output Display**
   - The **current counted value** (in seconds or tenths of seconds, based on SW B) must be displayed on the **7-segment displays** of the FPGA board.

Implementation Groups

- **Group 1:** Implement the **"blue modules"** (as shown in your project diagram or design document).
- **Group 2:** Implement the **"orange modules."**

Deliverables

Each group must submit:

1. **Project materials**
    - Quartus project files (.qpf, .bdf/.v/.vhd, pin assignments)
    - Timing and block diagrams (if applicable)
2. **Short Description**
    - Explain how each switch and key controls the system.
    - Describe the functionality of the timer and counter modules.
    - Mention how the display output is generated.
3. **Video Demonstration**
    - Show the FPGA in operation:
        - Demonstrate both UP and DOWN counting.
        - Show switching between seconds and seconds/10 mode.
        - Demonstrate timer triggering and reset functions.

Learning outcomes

- Use a **clock divider** to create 1-second and 0.1-second timing signals.
- Implement the **counter** and **timer** as separate modules for clarity.
- Use **state machines** for precise control of timer start/stop.
- Test each part separately before integrating everything.

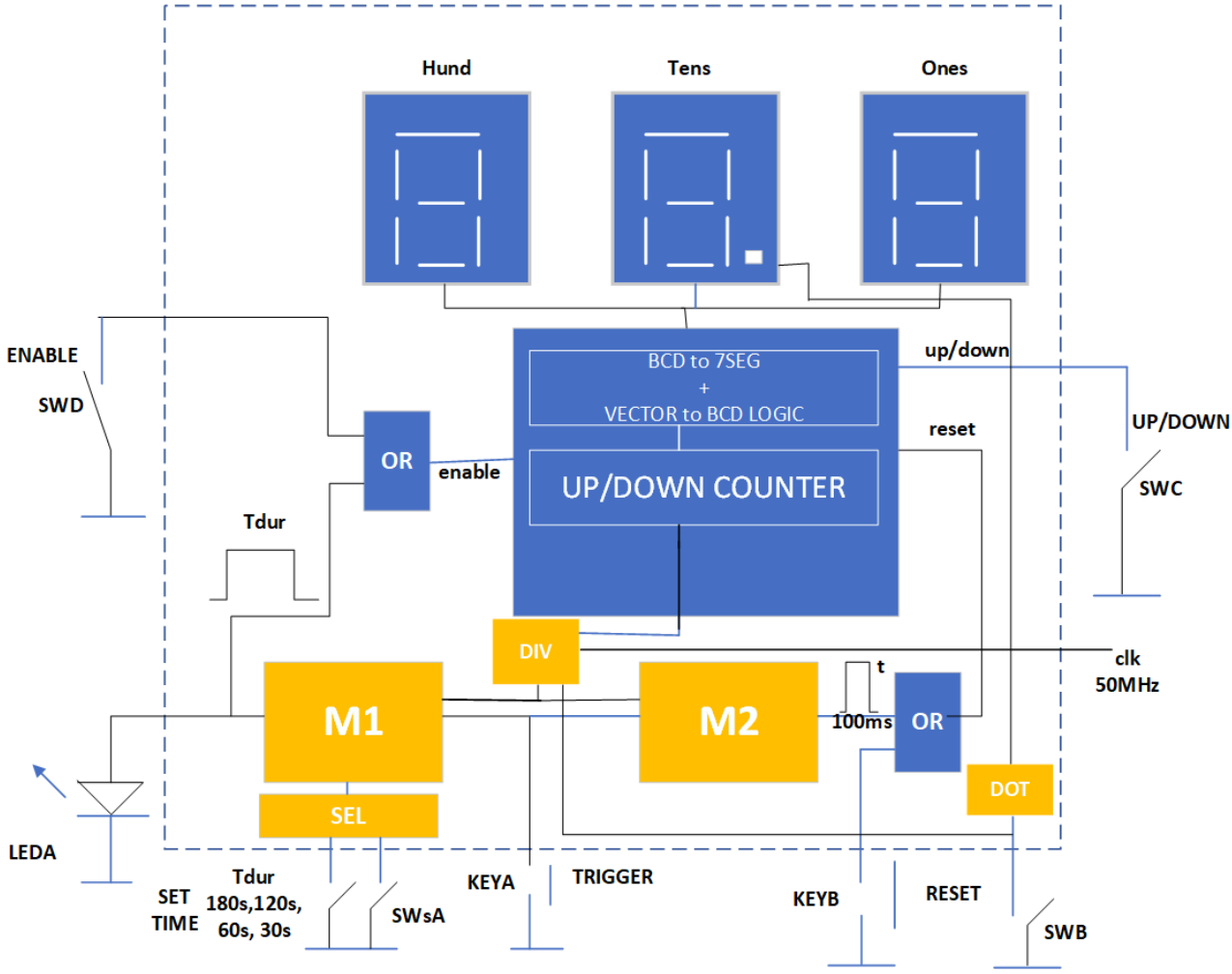

Figure 1: Architecture of FPGA UP/Down counter with Timer logic