Ni-Si baseline testing for n-doped and p-doped chips before and after annealing with silicide formation analysis

Methodology

Following the process in FabuBlox, two Ni-Si chips were fabricated for the baseline testing. One chip was n-doped and the other was p-doped. The chips were fabricated side by side and the Nickel was deposited at the same time.

The chips were probed before and after annealing at 250C for 15 minutes, and at 450C for 15min

Materials

Dopants: Filmtronics P504 SOG and Filmtronics B154 SOG

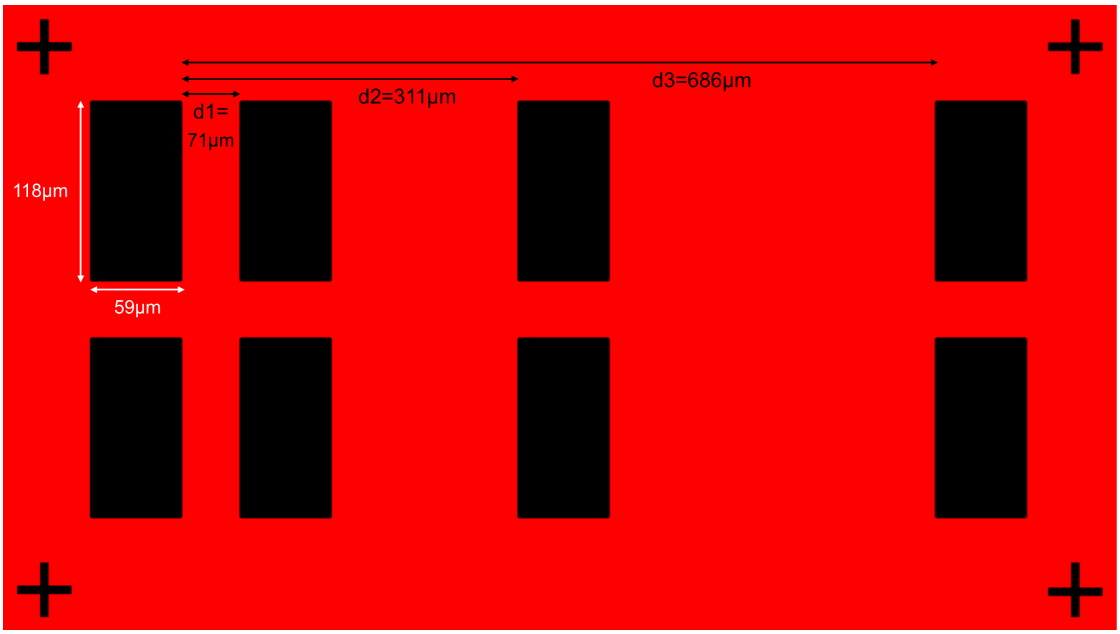
Insulating layer: Filmtronics 700B (SiO2)

Ni deposition source: Nickel electroless plating solution

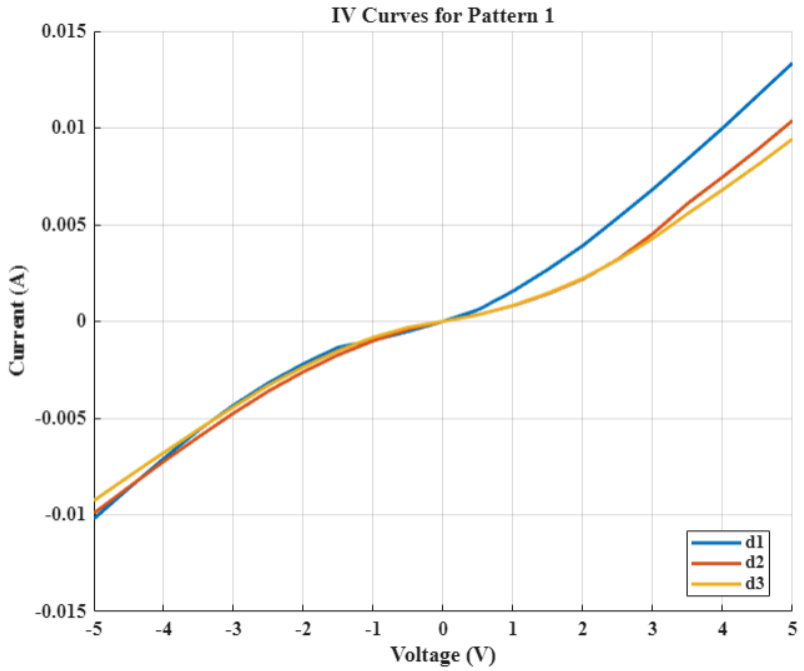
Substrate: University Wafer <100> single crystal p type silicon (5-10 ohm-cm)

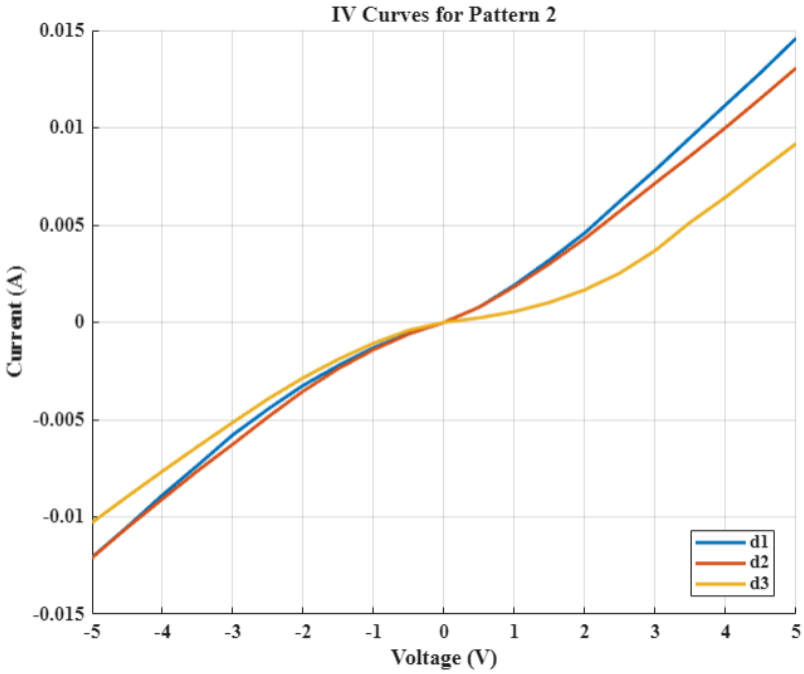
Patterns

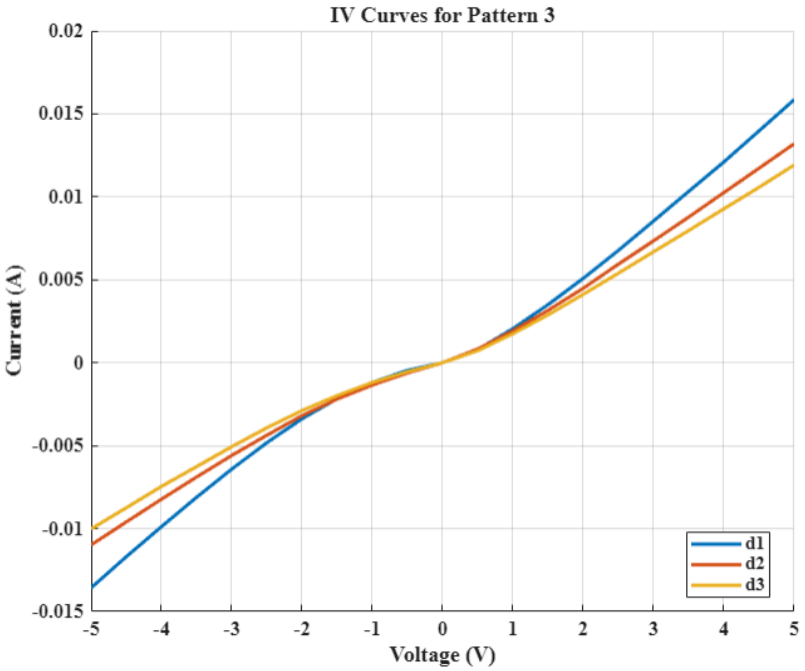
The patterns used are in Masks.pptx - Google Slides and shown in the figure below.

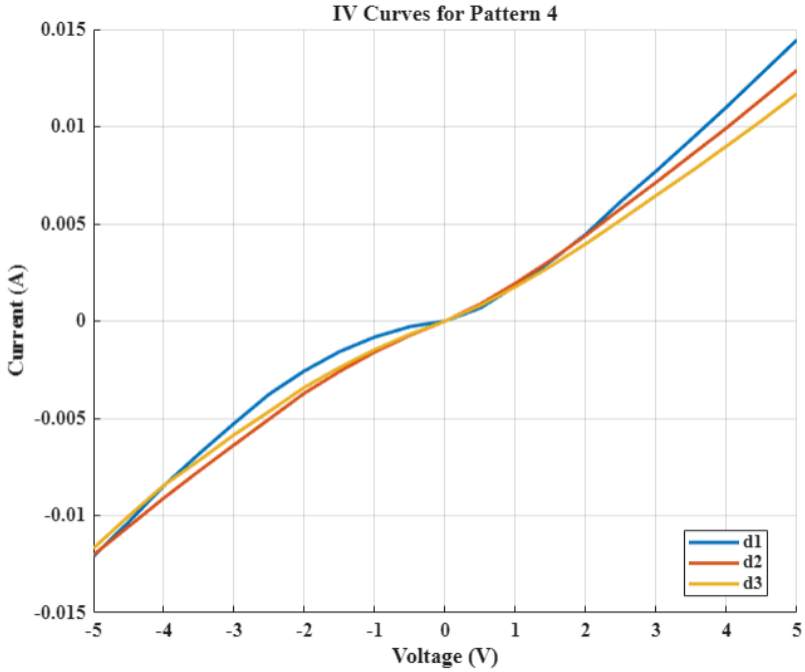


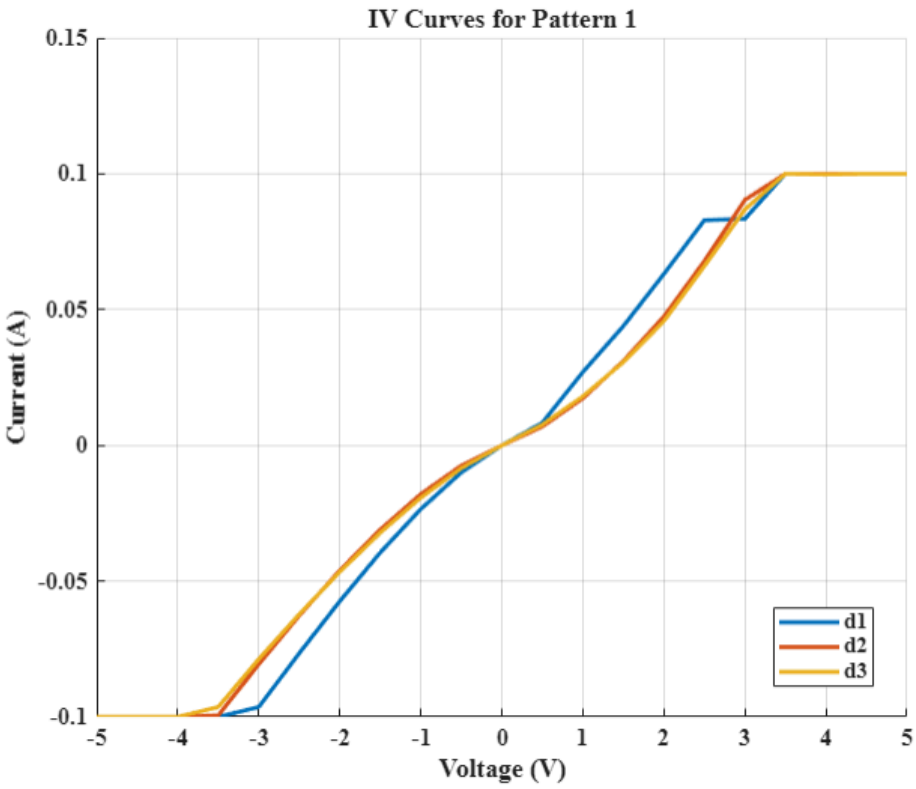
Annealing 250C Results - IV Plots

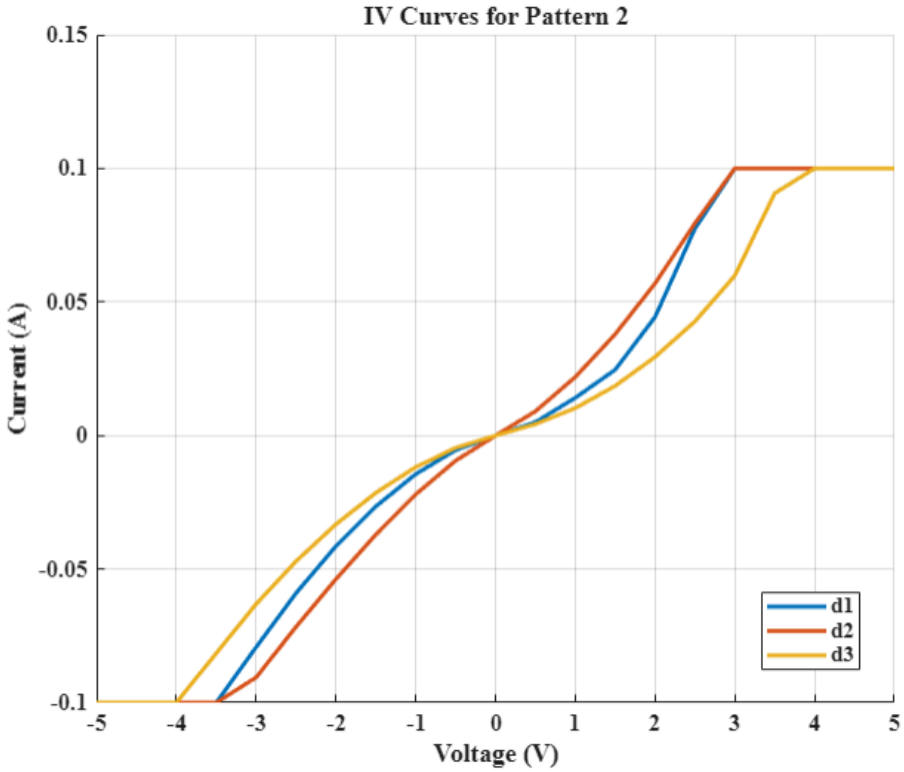


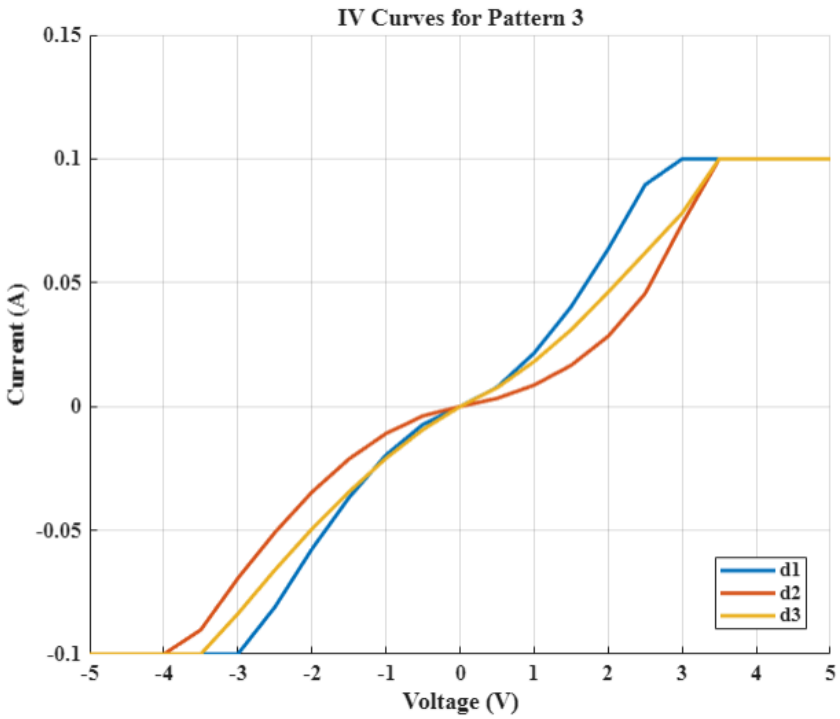


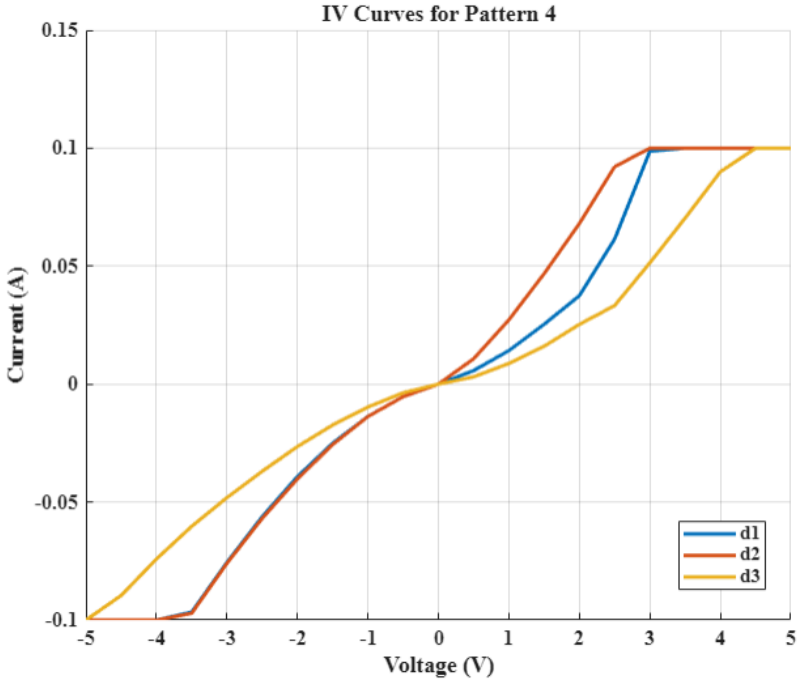

IV Curves for Pattern 3
Current (A)
Voltage (V)
d1
d2
d3

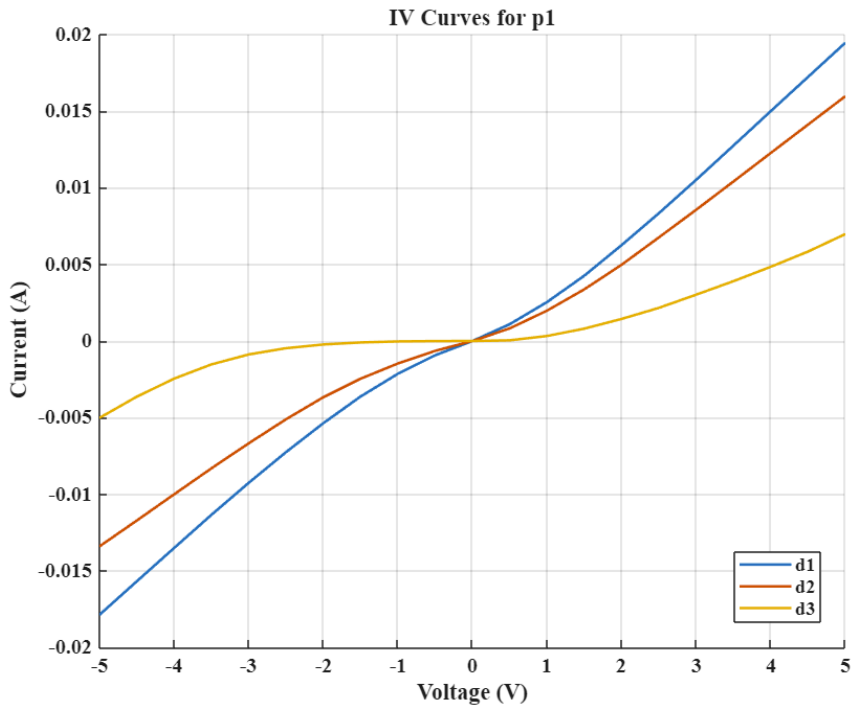

IV Curves for Pattern 4
Current (A)
Voltage (V)
d1
d2
d3

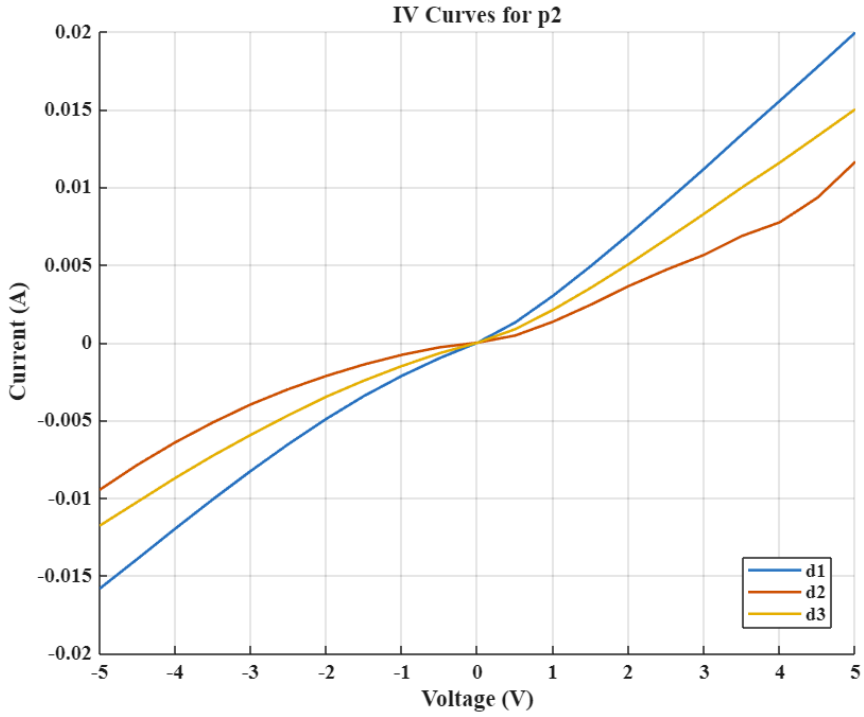

IV Curves for Pattern 1
Current (A)
Voltage (V)
0.15
0.1
0.05
0
-0.05
-0.1
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3

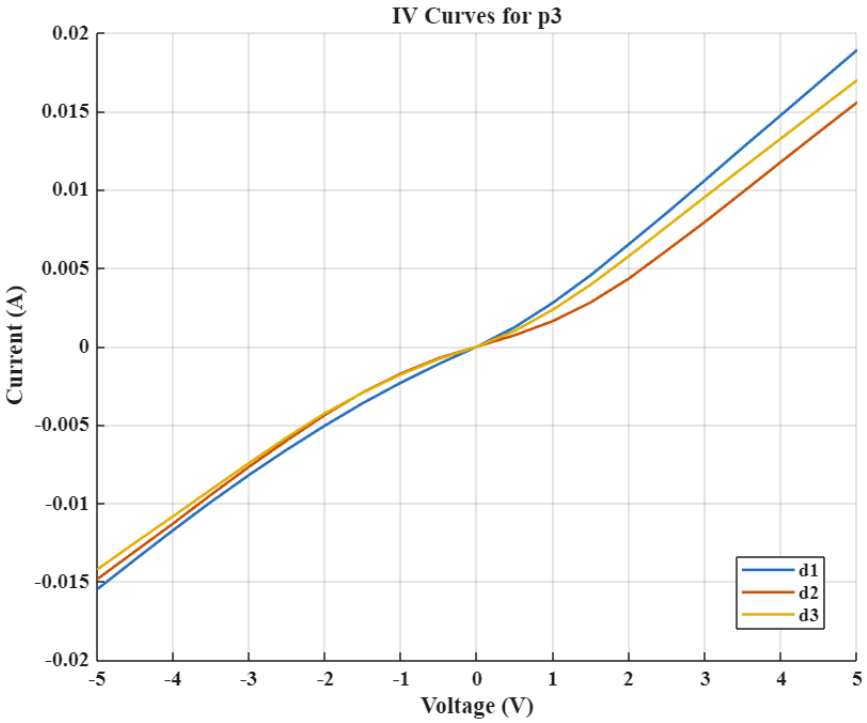

IV Curves for Pattern 2
Current (A)
Voltage (V)
0.15
0.1
0.05
0
-0.05
-0.1
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3

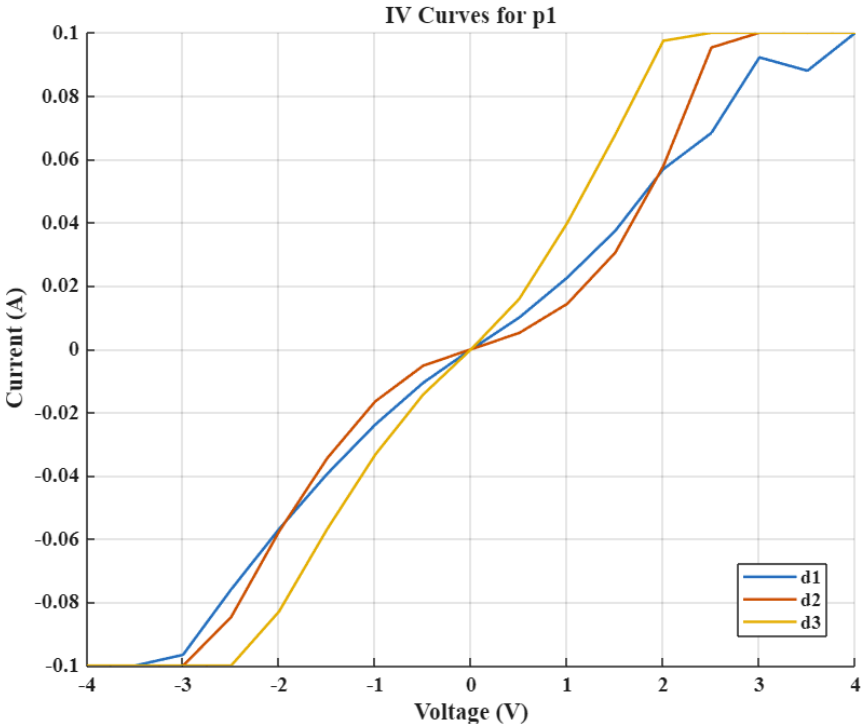

IV Curves for Pattern 3
Current (A)
Voltage (V)
0.15
0.1
0.05
0
-0.05
-0.1
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3

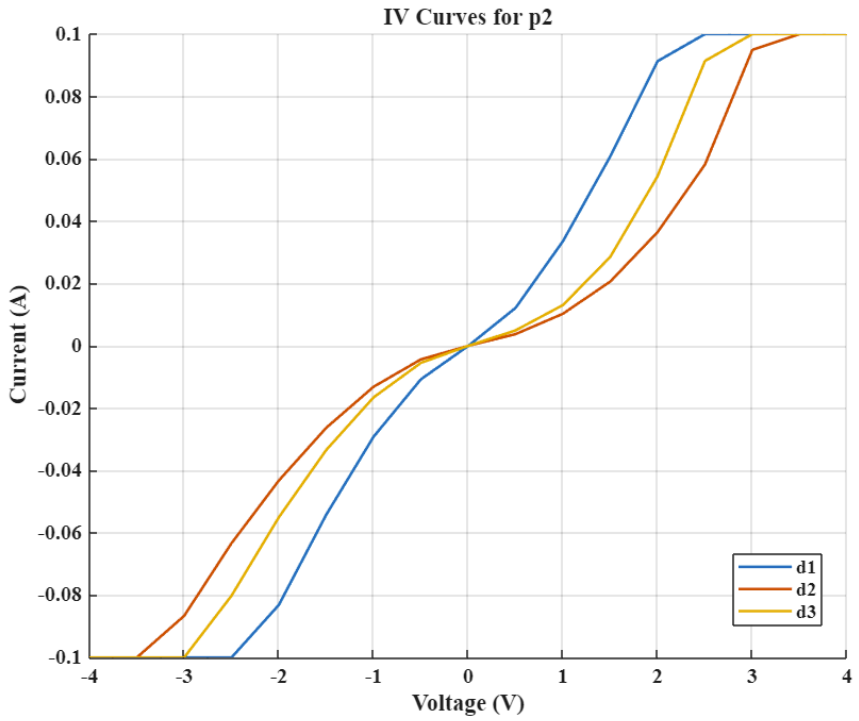

IV Curves for Pattern 4
Current (A)
Voltage (V)
0.15
0.1
0.05
0
-0.05
-0.1
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3

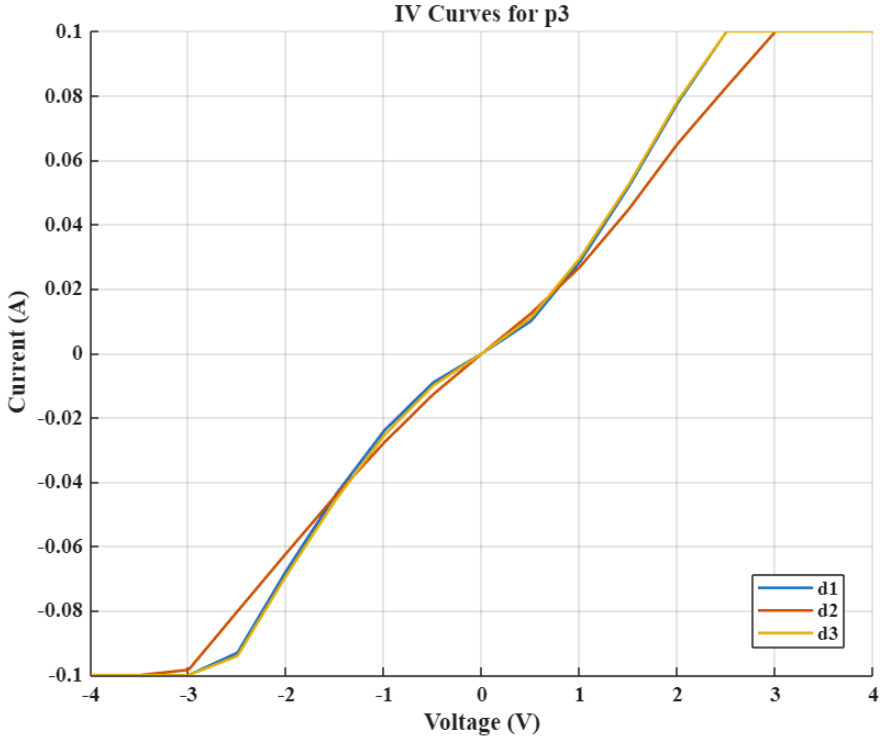

IV Curves for p1
Current (A)
Voltage (V)
0.02
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
-0.02
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3


IV Curves for p2
Current (A)
Voltage (V)
0.02
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
-0.02
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3


IV Curves for p3
Current (A)
Voltage (V)
0.02
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
-0.02
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3


IV Curves for p1
Current (A)
Voltage (V)
0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
-4
-3
-2
-1
0
1
2
3
4
d1
d2
d3

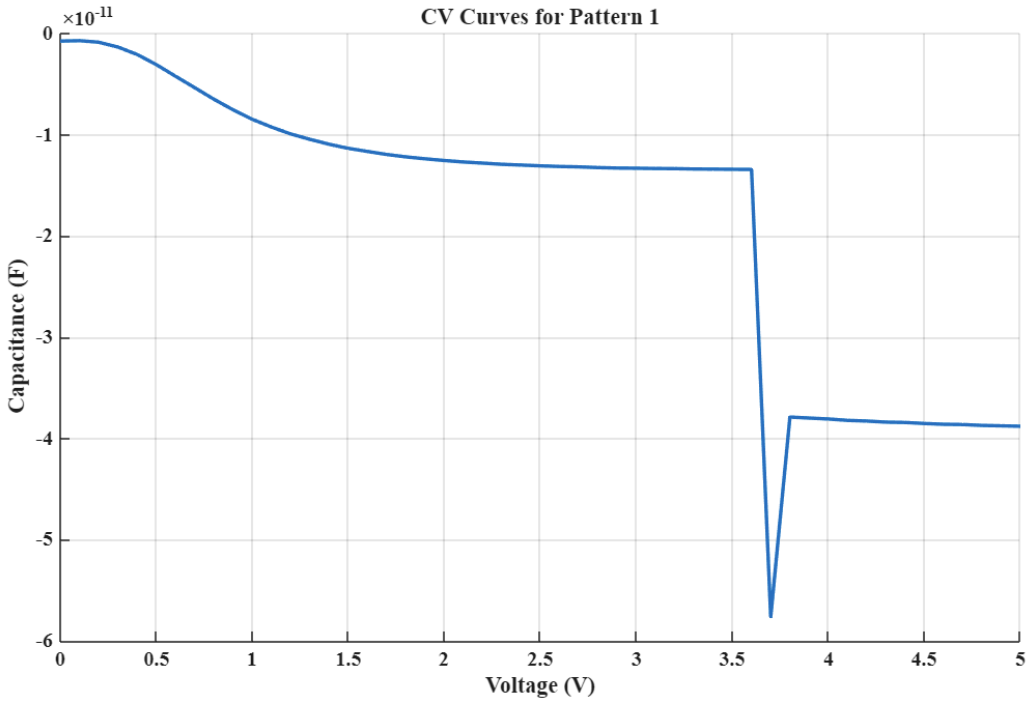

IV Curves for p2
Current (A)
Voltage (V)
d1
d2
d3

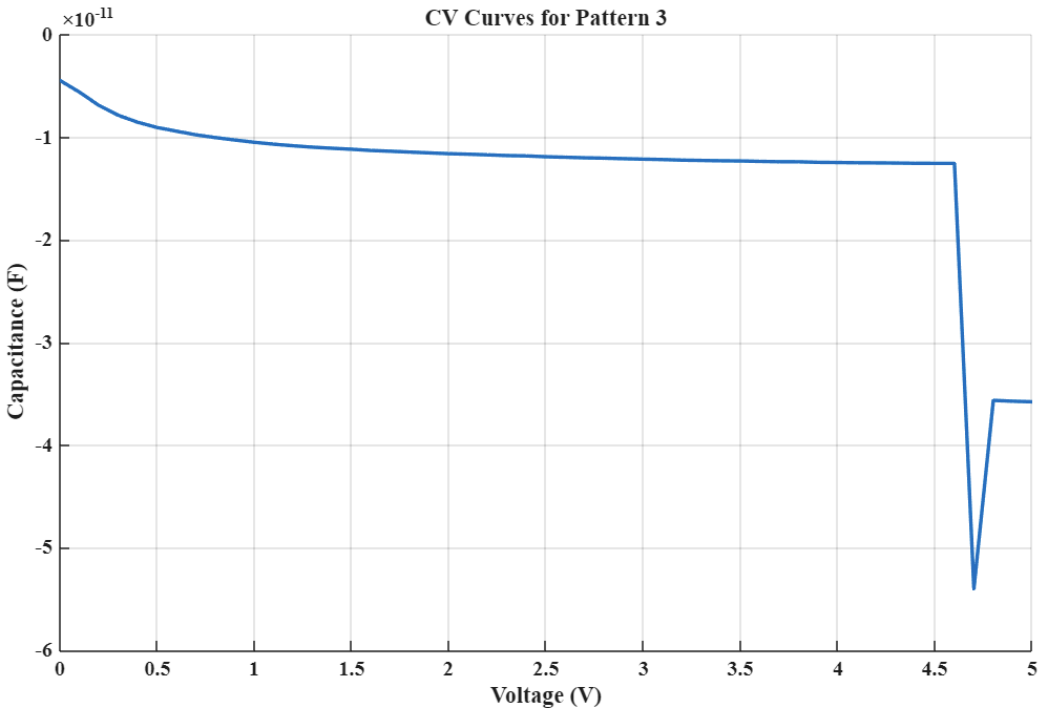

IV Curves for p3
Current (A)
Voltage (V)
d1
d2
d3

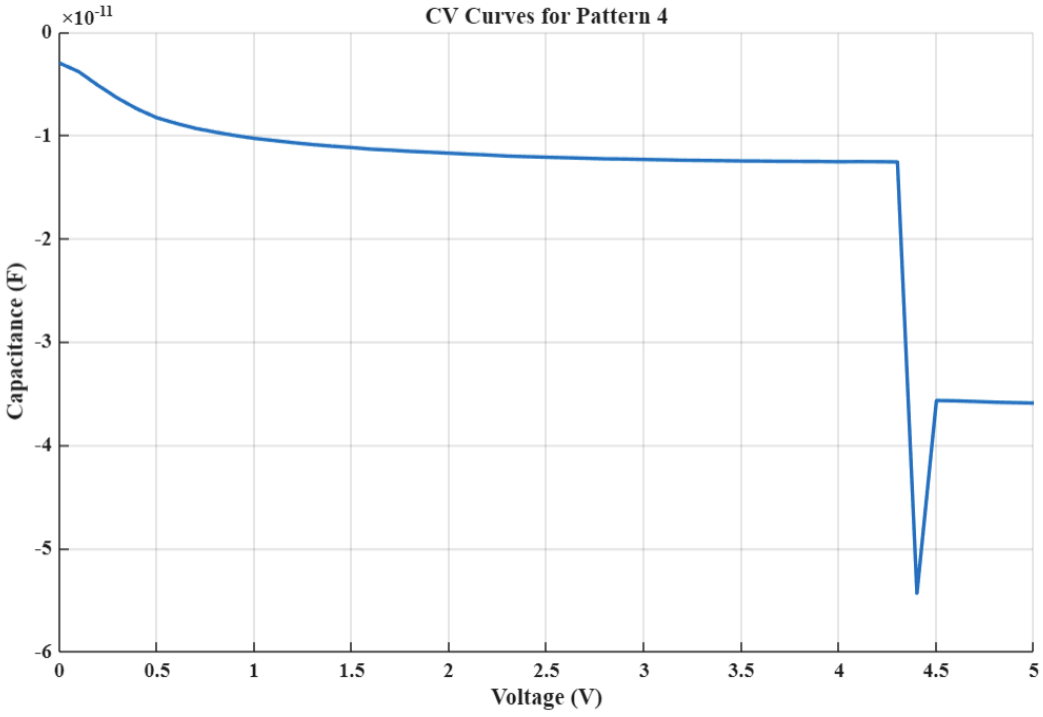
It appears that annealing at 250C was not enough to make the contacts ohmic, as it was for the Aluminum chips. Additionally, the contacts in these chips do not follow the usual trend of increasing resistance with increasing distances. Further annealing at 450C might provide more insights into this behavior.

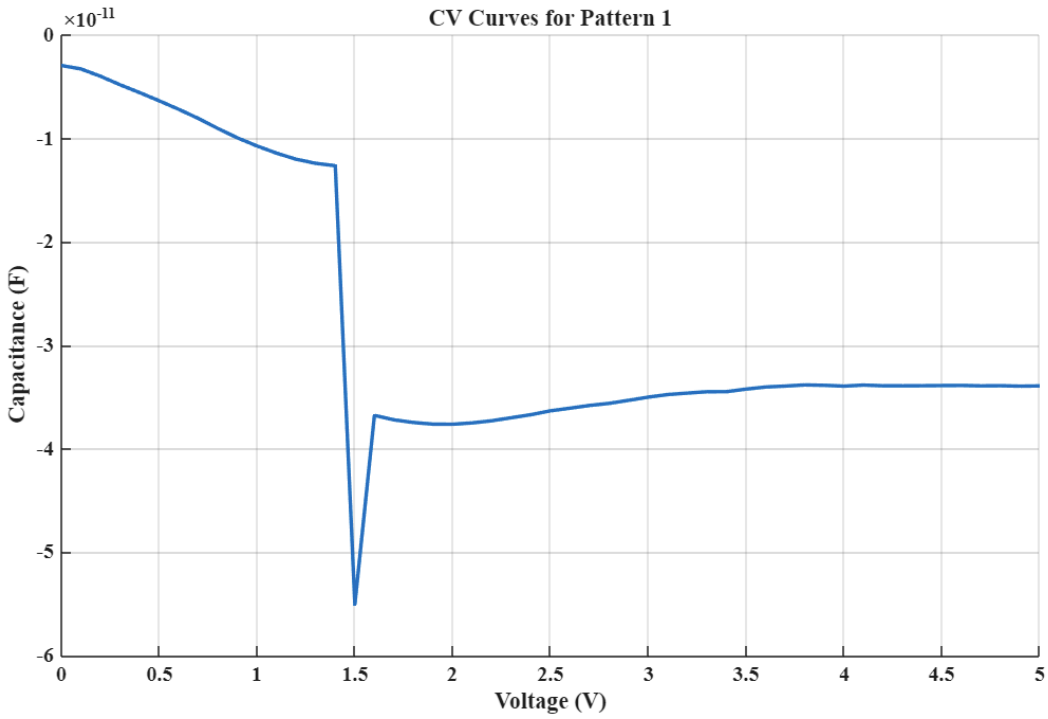
Annealing 250C Results - CV Plots

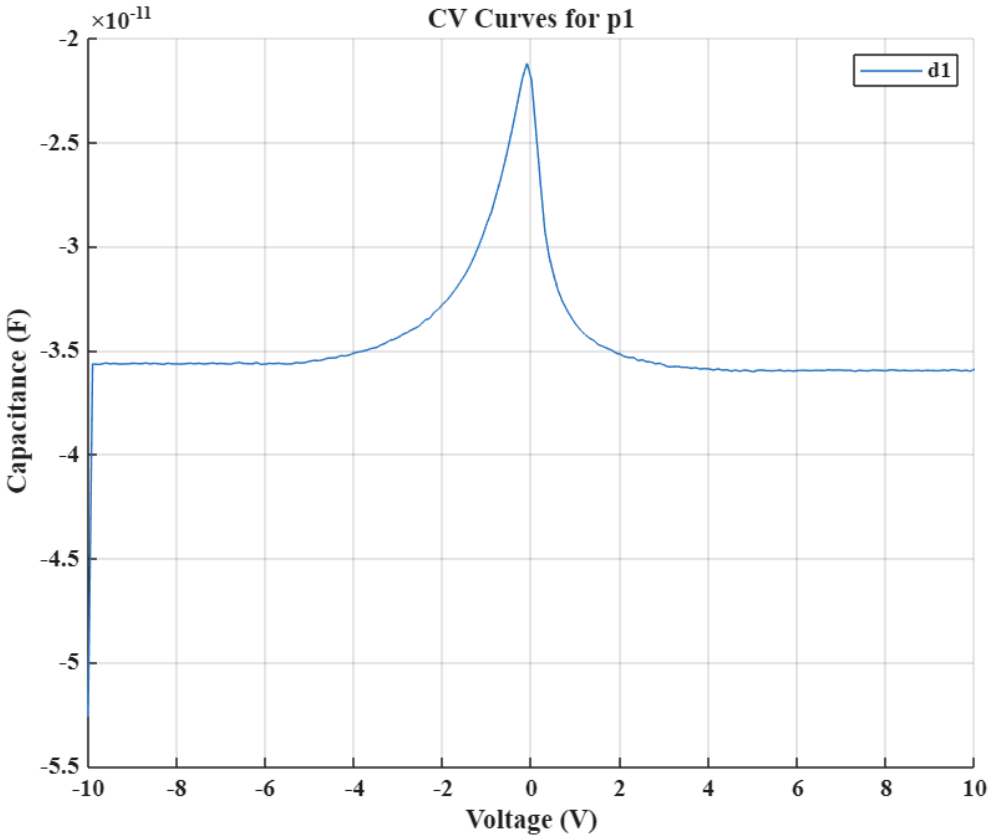
Performed at 10MHz

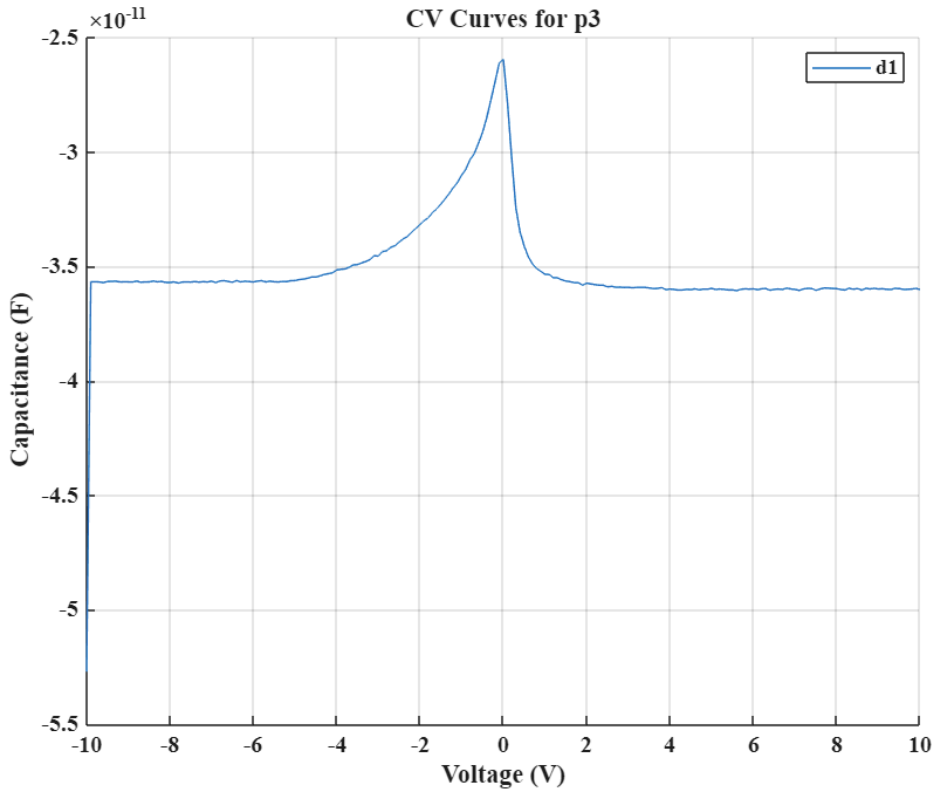


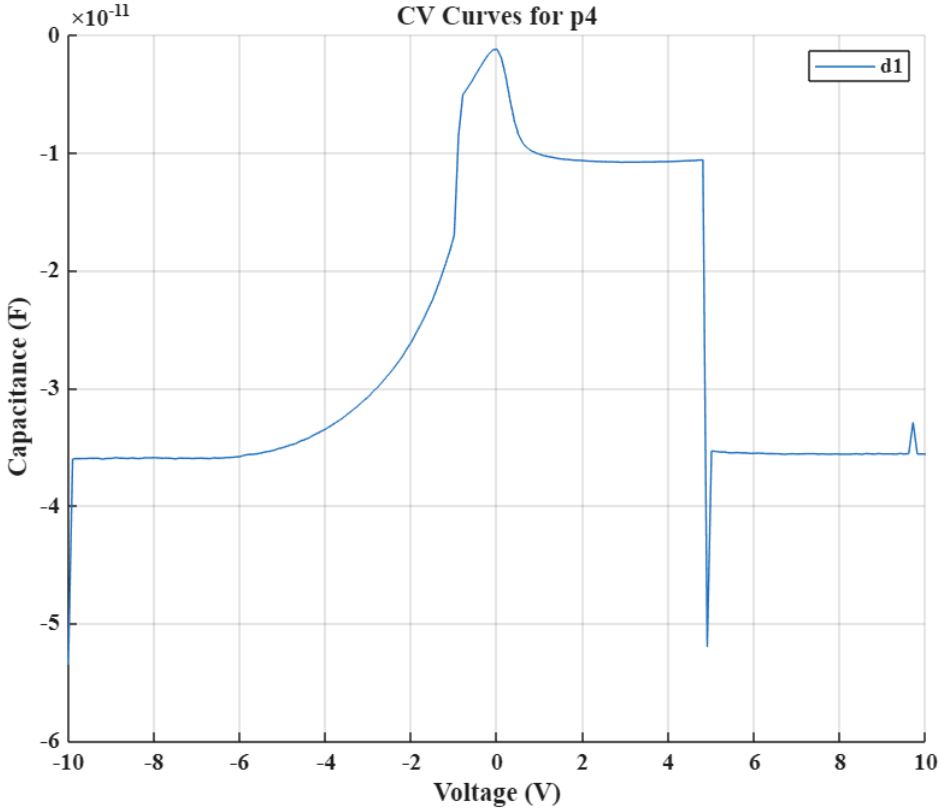

CV Curves for Pattern 3
×10-11
0
-1
-2
-3
-4
-5
-6
Capacitance (F)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Voltage (V)

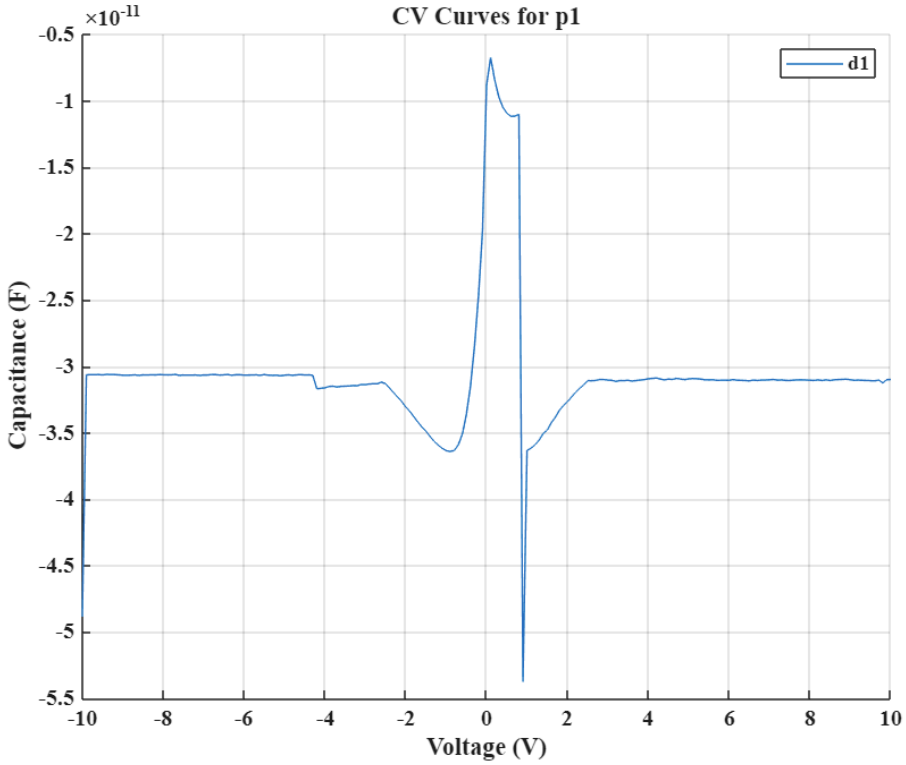

CV Curves for Pattern 4
×10-11
0
-1
-2
-3
-4
-5
-6
Capacitance (F)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Voltage (V)

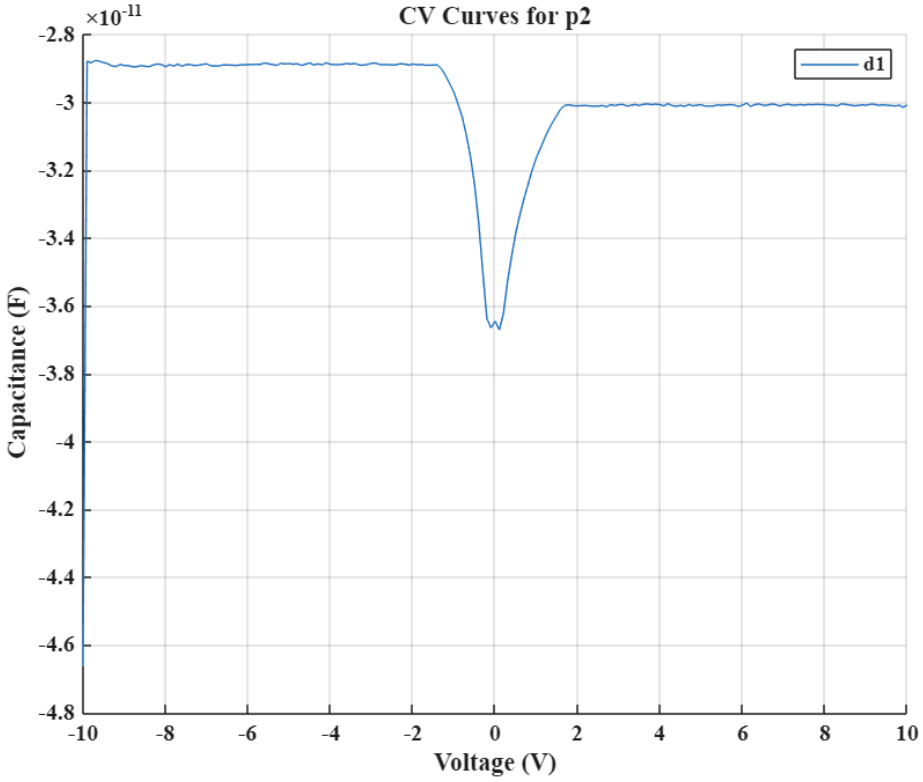

CV Curves for Pattern 1
×10^-11
0
-1
-2
-3
-4
-5
-6
Capacitance (F)
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Voltage (V)

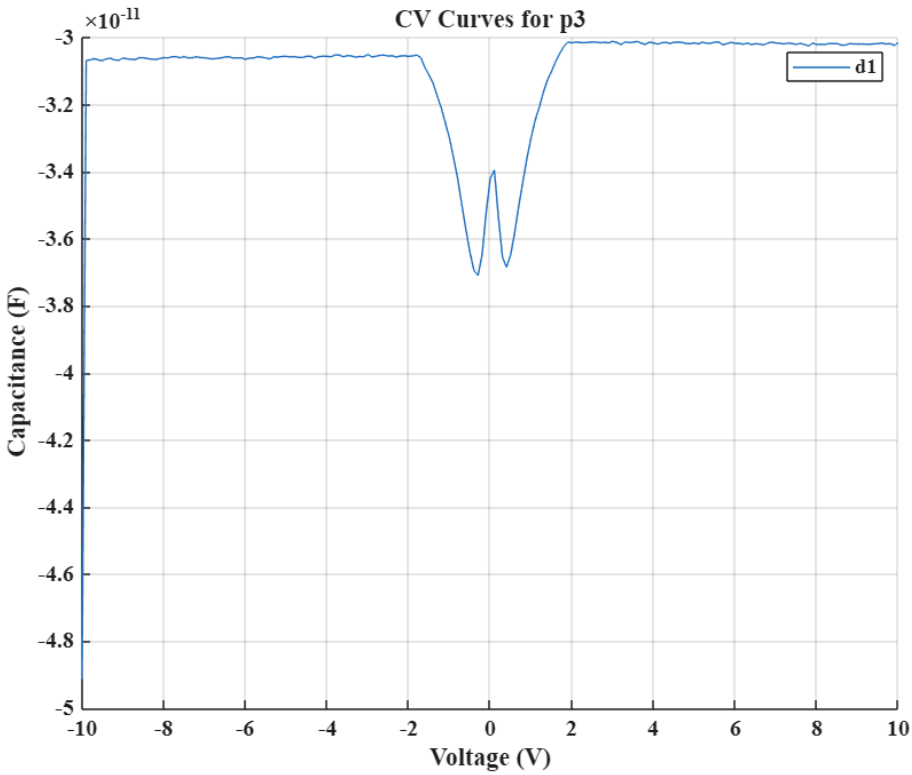

CV Curves for p1
×10^-11
-2
-2.5
-3
-3.5
-4
-4.5
-5
-5.5
Capacitance (F)
d1
-10
-8
-6
-4
-2
0
2
4
6
8
10
Voltage (V)


CV Curves for p3
×10-11
-2.5
-3
-3.5
-4
-4.5
-5
-5.5
Capacitance (F)
-10
-8
-6
-4
-2
0
2
4
6
8
10
Voltage (V)
d1

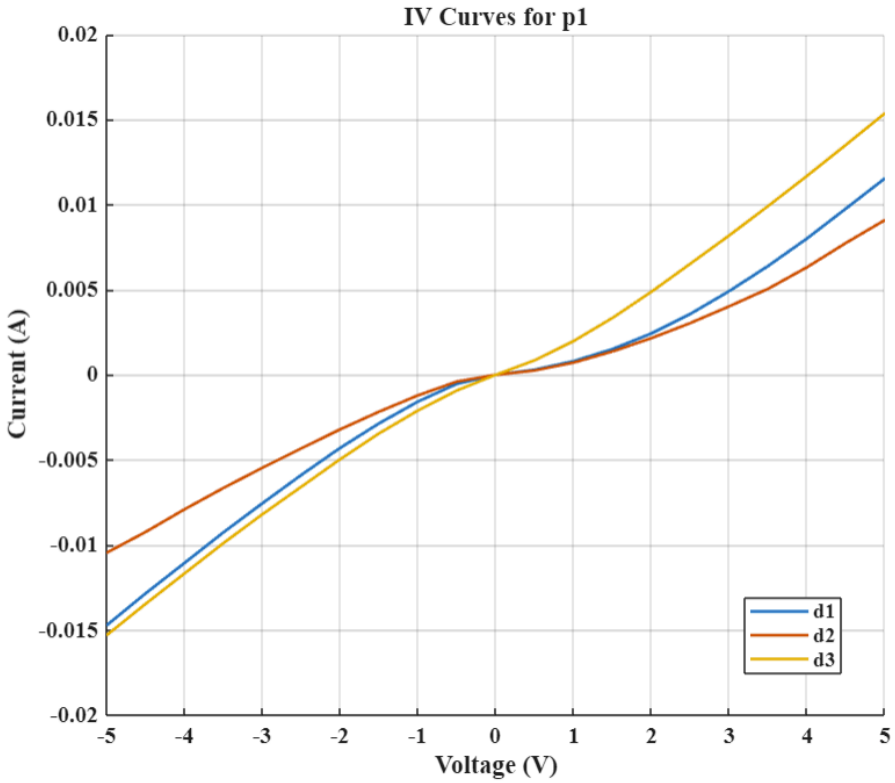

CV Curves for p4
×10-11
0
-1
-2
-3
-4
-5
-6
Capacitance (F)
-10
-8
-6
-4
-2
0
2
4
6
8
10
Voltage (V)
d1

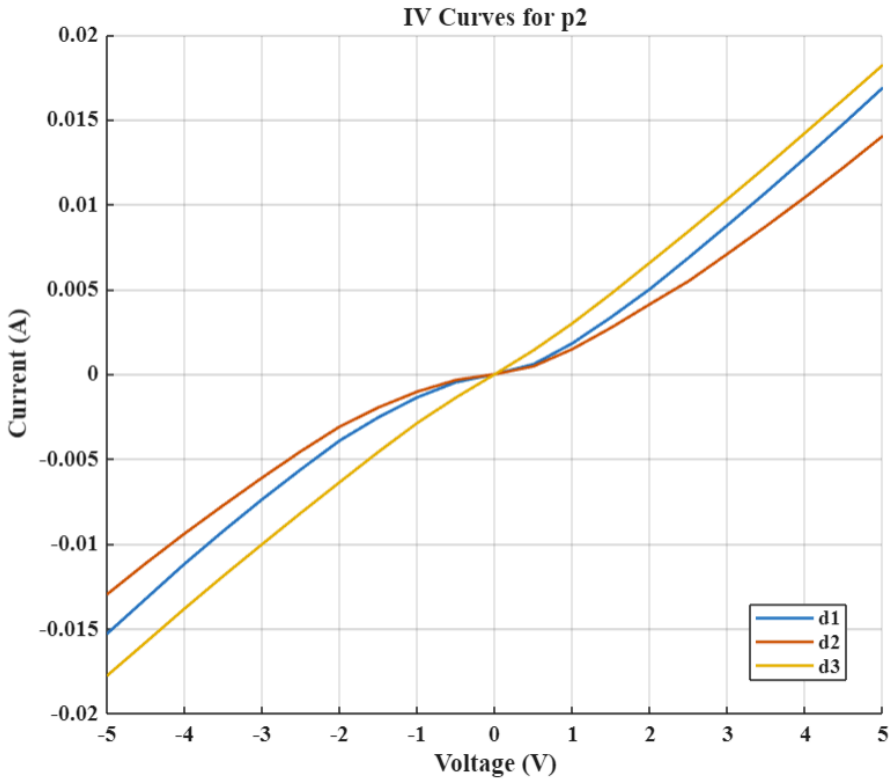

CV Curves for p1
×10-11
d1
Capacitance (F)
Voltage (V)
-0.5
-1
-1.5
-2
-2.5
-3
-3.5
-4
-4.5
-5
-5.5
-10
-8
-6
-4
-2
0
2
4
6
8
10

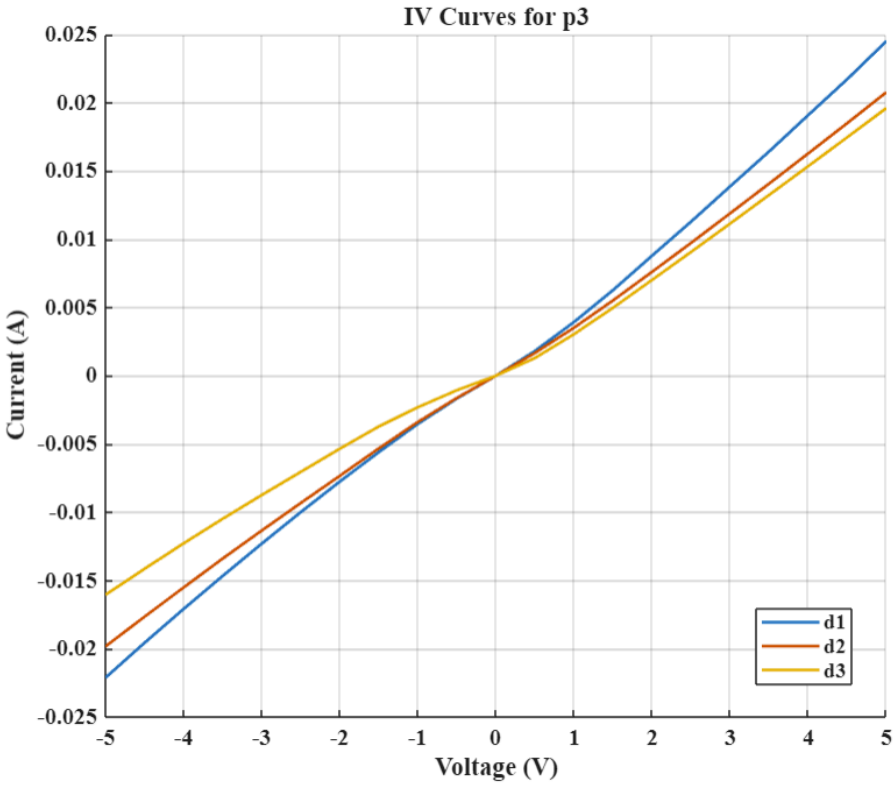

CV Curves for p2
×10-11
d1
Capacitance (F)
Voltage (V)
-2.8
-3
-3.2
-3.4
-3.6
-3.8
-4
-4.2
-4.4
-4.6
-4.8
-10
-8
-6
-4
-2
0
2
4
6
8
10

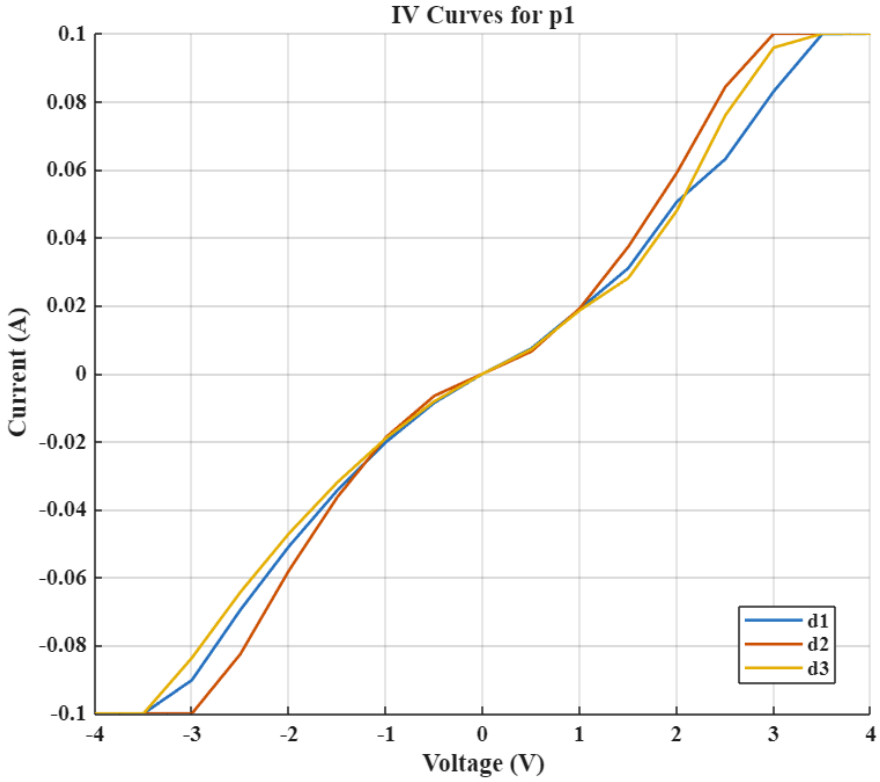

CV Curves for p3
×10-11
-3
-3.2
-3.4
-3.6
-3.8
-4
-4.2
-4.4
-4.6
-4.8
-5
Capacitance (F)
-10
-8
-6
-4
-2
0
2
4
6
8
10
Voltage (V)
d1

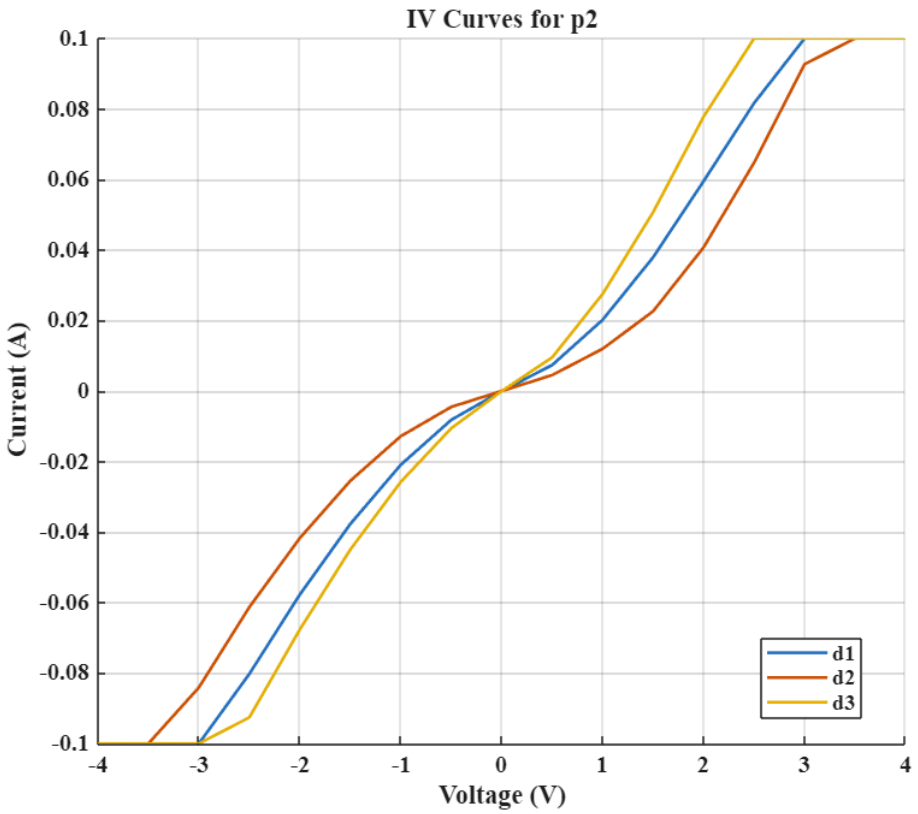
Annealing 450C (Silicide Formation) Results - IV Plots

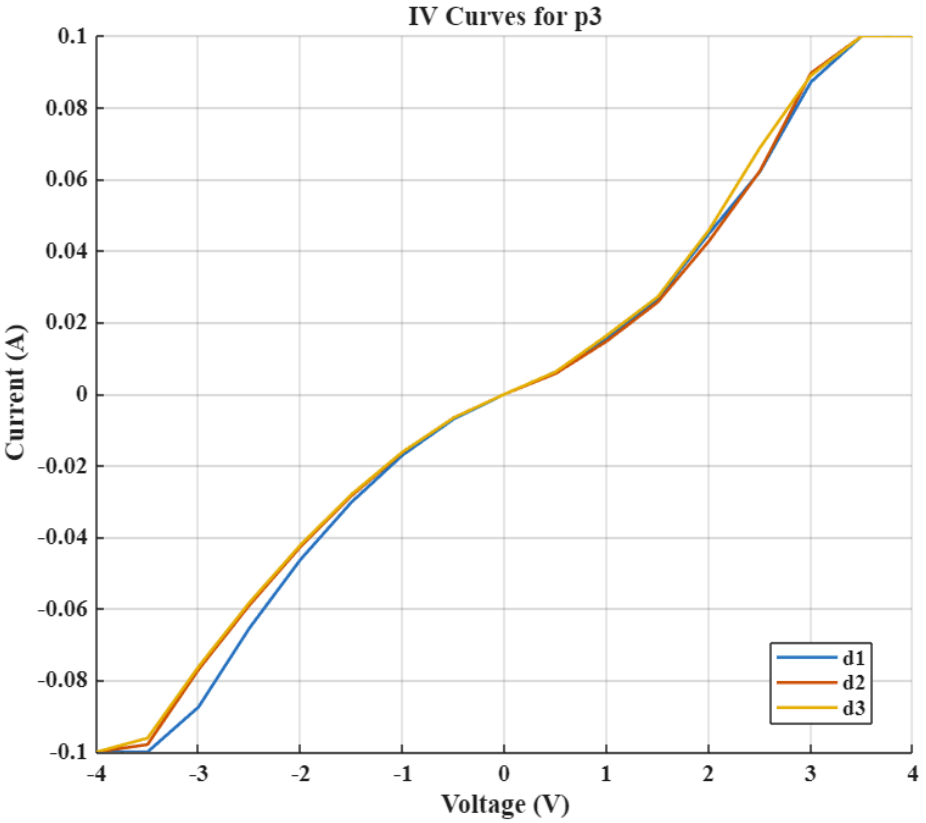





IV Curves for p3
Current (A)
Voltage (V)
0.025
0.02
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
-0.02
-0.025
-5
-4
-3
-2
-1
0
1
2
3
4
5
d1
d2
d3


IV Curves for p1
Current (A)
Voltage (V)
0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
-4
-3
-2
-1
0
1
2
3
4
d1
d2
d3


IV Curves for p2
Current (A)
Voltage (V)
0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
-4
-3
-2
-1
0
1
2
3
4
d1
d2
d3


IV Curves for p3
Current (A)
Voltage (V)
0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
-4
-3
-2
-1
0
1
2
3
4
d1
d2
d3

The resistance of the contacts did not increase with increasing probe distances as expected in the TLM probing method. Instead, the measurements showed no clear trend, suggesting poor contact quality and non-uniform current flow. Even after two annealing steps, which should have facilitated the formation of NiSi and $NiSi_2$ and improved contact behavior, there was no significant improvement in electrical properties. This suggests an incomplete or non-uniform silicide formation, diffusion issues, or barrier inhomogeneities.

Several factors could explain this behavior. Non-uniform silicide formation may have resulted in certain regions forming an ohmic NiSi phase, while others remained rectifying. Variations in the Schottky barrier height across the contact could contribute to the mix of ohmic and rectifying behavior that is possible to observe across several plots. Interfacial contamination or oxidation might have prevented proper contact formation, leading to an inconsistent reaction between Ni and Si. Additionally, the Nickel deposition might not have been completely homogeneous.

Despite undergoing multiple annealing steps, the Ni-Si contacts never exhibited consistent ohmic behavior. The persisting irregularities suggest that the silicidation process was either incomplete, non-uniform, or affected by interfacial contamination. Further investigation into the contact interface, silicide phase composition, and barrier height uniformity may be necessary to understand why these contacts failed to improve.