Bill's notes of Xilinx KV260

Board info:

Executive Summary:

Issues / Questions:

- **Ethernet does not seem to work in u-boot (at least in prebuilt 2021.1 images)**
  - This will be a problem
  - Reproduce with u-boot:
    - **# setenv autoboot off; dhcp**
    - **No ethernet found.**
  - The above is true; ethernet is not available in U-boot and Xilinx has no plans to make it available (publiclly)
  - Note: ZCU102 _does_ have ethernet in U-boot
  - ***Will have to plan a different CI model for this board***
- Schematics & BOM for SOM not available(?)
  - Vision starter carrier schematics are available
  - SOM description PDF does not include part numbers for QSPI and EMMC (TPM?, would others need DDR part #s?)
  - SOM schematics are not planned to be made publicly available
  - DT source has some part#s, good enough for our purposes
    - https://github.com/Xilinx/u-boot-xlnx/blob/master/arch/arm/dts/zynqmp-sm-k26-revA.dts
  - I would think that real SOM customers would want something a bit more official / easy to find but that is a Xilinx concern
- KV260 only supports QSPI boot mode
  - KV26 SOM supports multiple boot modes but vision starter carrier board ties to QSPI only
  - What is wear on QSPI like? How long will board last if we program new boot images 10 times a day (LAVA wore out BB-X15 eMMC in 2 years)
    - Assuming QSPI on SOM is similar to that on ZCU102 (MT25QU512ABB8ESF-0SIT) then it should be fine
    - Rated at 100K erase/write cycles
    - Assume worst case:
      - 4 writes to status block per trial (2 more likely)
      - 10 trials a day (probably peek would be 10/day, averaged over a month would be less)
      - Should still last 6.8 years

    - Is the recovery program scriptable with curl?
        - Nov3: Yes, the http API is pretty simple and can be seen by watching the network activity of the script (chrome devtools) or do:
            - wget http://192.168.0.111/index.js
            - And look at the code
    - Would it be possible to make an A/B/recovery switcher that activated SD boot instead of the recovery image if the FWUEN button is pushed?
    - Are the A/B/Recovery mtd partitions ...
        - permanently locked (OTP bits)
        - locked each boot by switcher
        - Locked via non-volatile r/w setting (can be unlocked with a command)
    - What is the procedure for writing a new A/B/Recovery image?
        - Is it doable w/o expensive Xilinx tools and licenses?
        - This board is supported by the no cost Vivado ML Standard version
        - Ubuntu 20.04 is a supported distro for this tool set
- SOM in KV260 does not seem to have eMMC
    - Not really a problem but the documents seem to be inconsistent in this regard
        - I think the documents are fine. I was reading ug1091 “Kria SOM Carrier Card Design Guide” as a reference for the kv260 carrier card but I see now that it is a guide on how to design YOUR OWN carrier card.
    - eMMC might have been nice to have for future SystemReady testing but won’t affect OpenAMP
        - Could by an official SOM (~$300) and use it with the KV260 carrier card
        - Double check this works before buying
- Is there info on using OpenOCD with this board? ZynqMP in general?
    - Upstream openocd does have zynqmp target
- The docs (where?) show the breakdown of boot.bin but does not show the fpga bit file. Is that bundled into the FSBL image?
    - Board _can_ boot w/o loading any FPGA
        - WAM: I thought all IO multiplexing was done via FPGA image but now understand that there is a more traditional IO pinmux layer for the PS side.
    - The current boot.bin images probably have no FPGA bit file and that FPGA is configured later. Confirm
    - Nov: confirmed that FPGA is loaded from userspace. There is one *.bit file in /lib/firmware/xilinx/*. It has associated dtbo files applied at kernel runtime.
- The SOM fan is really annoying
    - I bought a 140mm Fan to sit over the whole board and blow down.
        - OK to remove the SOM fan?
        - Is it as easy as it looks or are there any gotchas?
        - Is the fan removable w/o removing heatsink?
    - Nov3: I have removed the red cowling by undoing the four small screws. The cowling comes off w/o disturbing the heat sink. I have a large & quiet 140mm fan blowing across the heatsink. The heatsink efficiency may not be as good this

way but there is a lot of airflow and the chip never gets above 27C in the things I was doing.

- Linux shutdown does not work in prebuilt images
    - Shutdown for power off or reboot, neither works
    - Can work around with power switch but may corrupt image after a while

Documentation notes / issues:

Notes on ZynqMP SOC Architecture:

- R5's
    - Can run split mode or lock step
    - Memory
        - TCM memories
            - In split mode each R5 has its own TCMs, no direct map to TCMs of other (could go via global address but slow)
            - In lock set R5_0 has access to all TCMs (TCMs look twice as big)
            - A53 etc can only access TCMs via global address map and via the R5 subsystem (so it must be powered on, R5s could be in reset)
        - Shared direct access to OCM memories
            - Policed by firewall in front of OCM
        - Access to DDR
            - Can go direct to DDR or via IOMMU TBU and CCI based on chip level configuration
            - TBU can do policing and translation based on A53's control
            - CCI would make R5 accesses to DDR IO coherent when viewed from A53
            - Direct path has no TBU and is not coherent with A53s
            - Both paths pass through firewall on way to DDR
        - Global monitors in front of OCM (and DDR?)
            - So ld link / store conditional should work between R5s and A53s
- FPGA
    - Lots of choices for memory path
        - Note: a given IOMMU stream can be in bypass, going through TBU does not necessarily mean policing is enabled
        - Can go via SMMU TBU and CCI, IOMMU and IO coherent
        - Can go via SMMU TBU but bypass CCI, IOMMU but not IO coherent
        - others
            - Can go to APU ACP port (cache warming)
            - ACE to CCI (2 way coherency, cache in PL can stay coherent)
        - All paths seem to be able to get to OCM and go via a TBU
- GPU/PCIe/SATA:

    - Only one path that goes via a TBU and CCI
- USB
    - Path to OCM has not TBU. Does have a firewall
- Full power DMA is NOT IO coherent!
- Low power domain DMA IS IO coherent (or at least optionall)

Running with Xilinx Prebuilt images:

Good diagrams pulled from docs:

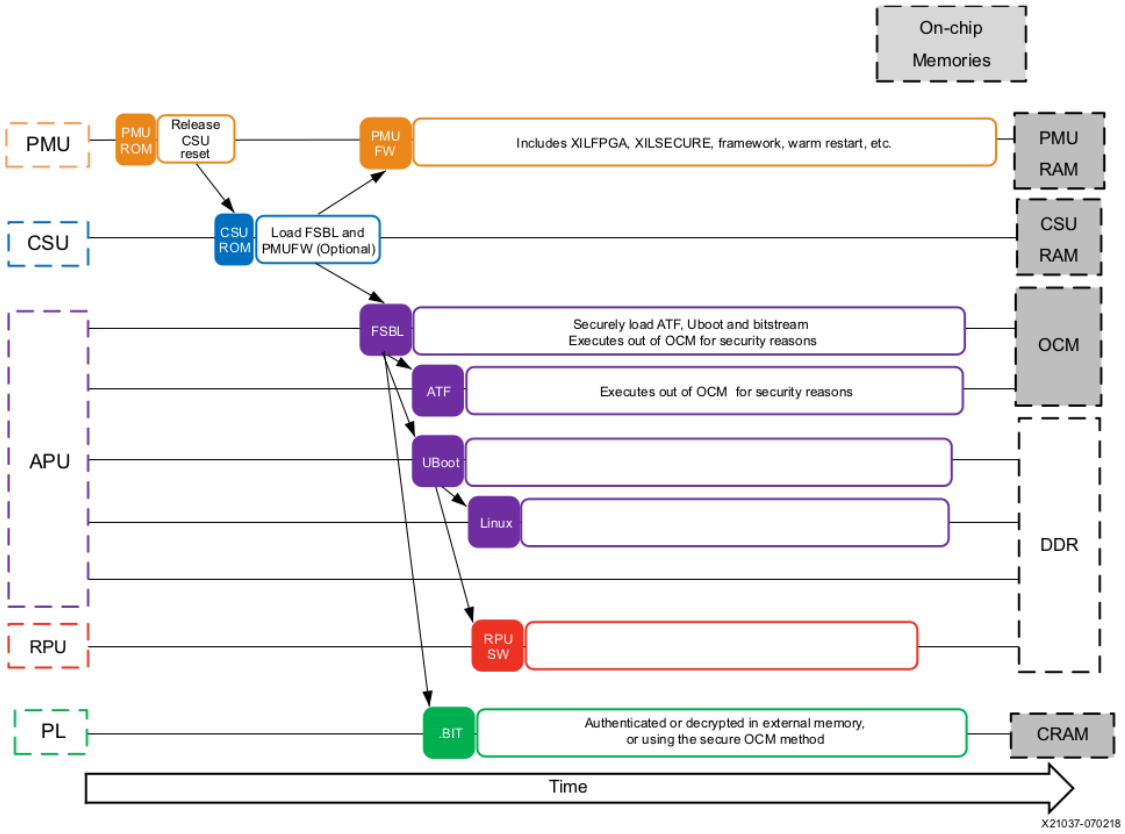

Figure 12-10: **Hardware Root of Trust Secure Boot Example**

Note: FSBL can run on APU (A53 core 0) or RPU (R5_0 in (lockstep or not)?) based on the FSBL header. Regardless of who runs FSBL it gets loaded to OCM. Above shows the default for Xilinx Linux (PetaLinux).

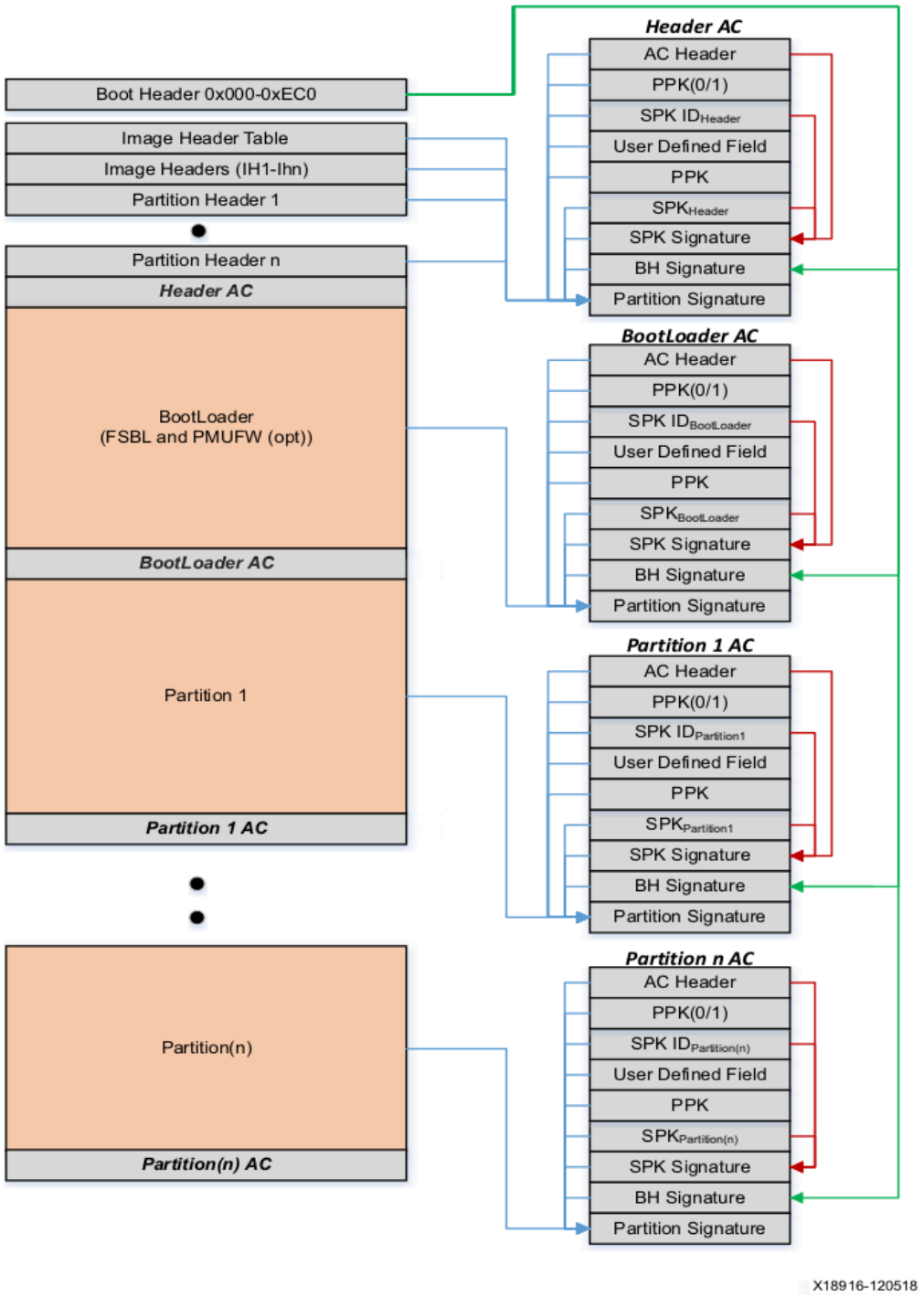

Figure 12-16: **Secure Boot Image**

Note: in the diagram above “partition” just means “section” not a disk (GPT or MBR) partition.

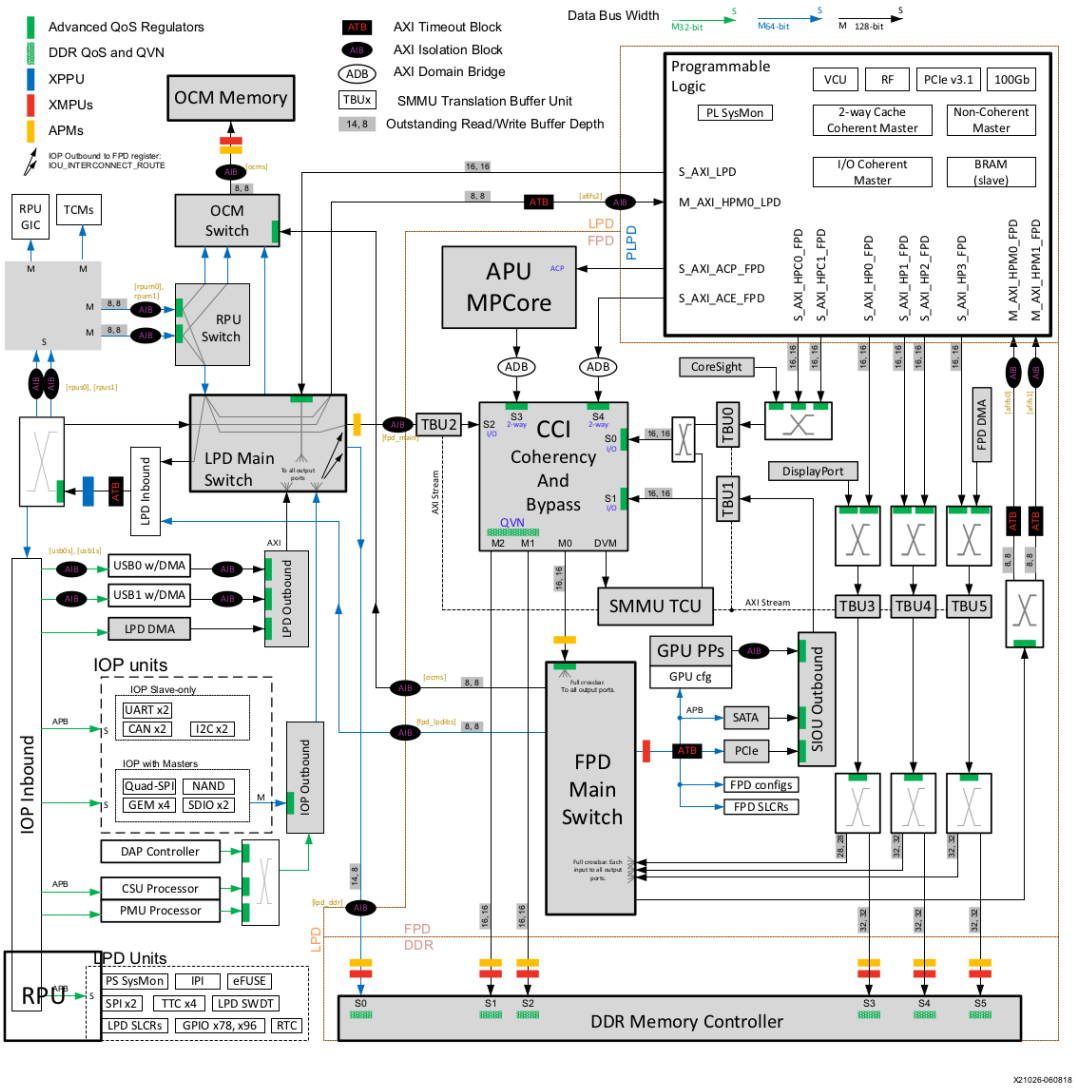

Figure 1-1: **AXI Interconnect**