Subject Code 5EC12

R15

VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

B.Tech. IV Year I Semester Regular/Supplementary Examinations, February 2021

VLSI DESIGN

(ECE)

Time: 3 hours **Max. Marks: 60**

*Answer any **FIVE** questions*

5X12=60

1. Derive an expression for Vin of a CMOS inverter to achieve the condition Vin=Vout. What should be the relation for βn=βp.

2. a) Derive the drain current of MOS device in different operating regions. 8M
   b) An NMOS transistor has the following parameters: gate oxide thickness=10nm, relative permittivity of gate oxide =3.9, electron mobility=520cm^2/v-sec, threshold voltage=0.7V, permittivity of free space=8.85x10^{-14}F/cm and W/L=8. Estimate the drain current when V_{GS}=2V and V_{DS}=1.2V and also compute the gate oxide capacitance per unit area. Note that W and L refer to the width and length of the channel respectively. 4M

3. a) Discuss about stick diagram Encodings for a simple metal nMOS process with neat diagrams.
   b) Draw schematic and layout diagram for 2-input CMOS NOR logic.

4. a) Derive the expressions for Rise time and Fall time for CMOS inverter. 8M
   b) Explain about Choice of Layers in detail. 4M

5. a) Draw the neat diagram of Parity generator - structured design approach, and its Stick diagram.
   b) Differentiate FPGA and CPLD.

6. a) Design 4-bit Carry Select Adder.
   b) Design Binary to Gray code converter using PLA.

7. a) Explain about Design capture tools and Design verification tools.
   b) Explain scan path testing with neat diagram.

8. a) Explain in detail about Built In Self Testing (BIST) techniques.
   b) Compare chip level test techniques and system level techniques.

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