VHDL notebook za studente

```
-- 4 bits up counter with reset
--# DE2-70 pin assignments for 4-bit counter

--PIN_AB26   -to clk      # SW1
--PIN_AA23 -to rst       # SW0
--PIN_W27  -to q[0]      # LEDG0
--PIN_W25 -to q[1]       # LEDG1
--PIN_W23 -to q[2]       # LEDG2
--PIN_Y27 -to q[3]       # LEDG3
--PIN_AC27 to up_down    #SW3 (Za domaci)
-- FAMILY  CYCLONE II
-- DEVICE EP2C70F896C6



library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity counter4_sync_reset is
   port (
      clk   : in  std_logic;
      rst   : in  std_logic; -- aktivni HIGH sinhroni reset
      q     : out std_logic_vector(3 downto 0)
   );
end entity;

architecture rtl of counter4_sync_reset is
```

```
    signal cnt : unsigned(3 downto 0) := (others => '0');
begin
    process(clk)
    begin
        if rising_edge(clk) then
            if rst = '1' then
                cnt <= (others => '0'); -- sinhroni reset
            else
                cnt <= cnt + 1;
            end if;
        end if;
    end process;

    q <= std_logic_vector(cnt);
end architecture;
```