Department of Electronics Engineering (VLSI D & T)

Academic Year	:	2025-26	Course Name	:	Low Power VLSI Design
Semester	:	6th	Course Code	:	BVL613A
Scheme	:	2022	L:P: SDA:C	:	3:0:0:3
Total Contact hours	:	40 hrs	CIE Marks	:	50
Course Plan Author	:	Dr. N.C Patil	SEE Marks	:	50
Date	:	05.01.2026	Total Marks	:	100

Course Prerequisites:

1. Digital Electronics.
2. Synthesis basics
3. Digital VLSI design concepts

Learning Objectives:

This course will enable students to

1. To identify the power dissipation mechanisms in various MOS logic styles
2. To familiarize suitable techniques to reduce power dissipation

Course Outcomes:

CO		*At the end of the course, students should be able to . . .*	**Blooms' Level**
CO1	:	**Understand** the impact of low power on system performance	2
CO2	:	**Identify** the mechanisms of power dissipation in digital IC systems.	3
CO3	:	**Apply** different circuit techniques to manage the low power	3
CO4	:	**Analyze** the functionality of Low- voltage low -power memories	4

Blooms' Taxonomy:

L1	L2	L3	L4	L5	L6
Remembering	**Understanding**	**Applying**	**Analyzing**	**Evaluating**	**Creating**

Program Outcomes:

PO1	**:**	Engineering knowledge	**PO7**	**:**	Environment and sustainability
PO2	**:**	Problem analysis	**PO8**	**:**	Ethics
PO3	**:**	Design/development of solutions	**PO9**	**:**	Individual and team work
PO4	**:**	Conduct investigations of complex problems	**PO10**	**:**	Communication
PO5	**:**	Modern tool usage	**PO11**	**:**	Project management and finance
PO6	**:**	The engineer and society	**PO12**	**:**	Life-long learning

Program Specific Outcomes:

PSO1:	Graduates will possess advanced knowledge and practical skills in VLSI design including the use of state-of-the-art tools and techniques to develop, analyze and optimize analog, digital and mixed mode systems for real-world applications.
PSO2:	Graduates will demonstrate the ability to conduct interdisciplinary research in VLSI technologies contributing to innovative solutions that address global challenges while advancing sustainable and inclusive technology
PSO3:	Graduates will be equipped with the entrepreneurial mindset and leadership qualities necessary to create innovative solutions in VLSI design, promoting new ventures, generating employment and taking on roles that foster industry collaboration and societal impact.

CO-PO-PSO Mapping:Course Content (Syllabus)

CO	Program Outcomes														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	3	2	–	–	–	-	-	-	-	-	-	-	3		
CO2	2	3	3	–	2	-	-	-	-	-	-	-	3		
CO3	3	3	2	2	2	-	-	-	-	-	-	-	2		
CO4	3	2	3	2	3	-	-	-	-	-	-	-	2		

Module 1	CH
Introduction **Introduction, Sources of power dissipation, designing for low power, Physics of Power dissipation in MOSFET devices MIS structure, Need for low power circuit design, Threshold voltage, body effects.**	**08**
Module 2	
Power dissipation in CMOS **Sources of power dissipation in CMOS-Switching power dissipation, Short circuit power dissipation, glitching power dissipation, Leakage power dissipation, Transistor leakage mechanisms of deep submicron transistors, Low power design limits - Principles of low power design.**	**08**
Module 3	
LOW POWER CIRCUIT TECHNIQUES **Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.**	**08**
Module 4	
LOGIC SYNTHESIS FOR LOW POWER ESTIMATION TECHNIQUES **Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers**	**08**
Module 5	
LOW POWER MEMORY DESIGN **Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.**	**08**

Schedule of Instruction:

Class No	Topic	Date	RBT	CO	Mode
Module-1					
Chapter Name					
1.	**Introduction of course website:**	27.01.26			PPT
2.	**Introduction of subject:Importance & MOOC's**	30.01.26	L2	CO1	PPT
3.	**Sources of power dissipation**	02.02.26	L2	CO1	L
4.	**Designing for low power**	03.02.26	L2	CO1	L
5.	**Designing for low power**	06.02.26	L2	CO1	V+L
6.	**Physics of Power dissipation in MOSFET devices**	09.02.26	L2	CO1	L
7.	**MIS structure**	10.02.26	L2	CO1	L
8.	**Need for low power circuit design,**	13.02.26	L3	CO1	PPT
9.	**Threshold voltage**	16.02.26	L2	CO1	L
10.	**Body effect**	17.02.26	L3	CO1	L
Module-2					
Chapter Name					
11.	**Power dissipation in CMOS**	20.02.26	L2	CO2	L
12.	**Sources of power dissipation in CMOS**	23.02.26	L2	CO2	L
13.	**Switching power dissipation,**	24.02.26	L2	CO2	L
14.	**Short circuit power dissipation**	27.02.26	L2	CO2	L
15.	**Glitching power dissipation,**	02.03.26	L3	CO2	L
16.	**Leakage power dissipation**	03.03.26	L3	CO2	L
17.	**Transistor leakage mechanisms of deep submicron transistors,**	06.03.26	L2	CO2	L
18.	**Low power design limits - Principles of low power design**	09.03.26	L2	CO2	L
Module-3					
Chapter Name					
19.	**LOW POWER CIRCUIT TECHNIQUES**	10.03.26	L2	CO3	
20.	**Power consumption in circuits,,**	13.03.26	L2	CO1	L
21.	**Flip-flops & latches,**	20.03.26	L2	CO1	L
22.	**High capacitance nodes,**	30.03.26	L4	CO2	L
23.	**Energy recovery,**	31.03.26	L4	CO2	L
24.	**Reversible pipelines,**	03.04.26	L4	CO2	L
25.	**High performance approaches.**	06.04.26	L2	CO2	L
26.	**High performance approaches.**	07.04.26	L2	CO1	L
Module-4					
Chapter Name					
27.	**LOGIC SYNTHESIS FOR LOW POWER ESTIMATION TECHNIQUES**	13.04.26	L2	CO3	PPT

Class No	Topic	Date	RBT	CO	Mode
28.	**Logic Synthesis for Low Power estimation techniques:**	17.04.26	L3	CO3	L
29.	**Logic Synthesis for Low Power estimation techniques:**	21.04.26	L2	CO3	L
30.	**Power minimization techniques,**	24.04.26	L3	CO3	L
31.	**Power minimization techniques,**	27.04.26	L3	CO3	L
32.	**Low power arithmetic components-**	28.04.26	L2	CO3	L
33.	**Circuit design styles,**	04.05.26	L2	CO3	L
34.	**Adders, multipliers**	08.05.26	L2	CO3	L
Module-5					
Chapter Name					
35.	**LOW POWER MEMORY DESIGN Low-Voltage Low-Power Memories: Basics of ROM,**	09.05.26	L2	CO4	PPT
36.	**Low-Power ROM Technology,**	09.05.26	L3	CO4	L
37.	**Future Trend and Development of ROMs,**	11.05.26	L3	CO4	L
38.	**Basics of SRAM, Memory Cell,**	11.05.26	L2	CO4	L
39.	**Precharge and Equalization Circuit,**	12.05.26	L3	CO4	L
40.	**Low Power SRAM Technologies,**	12.05.26	L2	CO4	L
41.	**Basics of DRAM, Self-Refresh Circuit,**	14.05.26	L2	CO4	L
42.	**Future Trend and Development of DRAM.**	15.05.26	L3	CO4	L

Textbooks:

T1	Gray Yeap, Practical low power digital VLSI design, Springer, 1998
T2	Kaushik Roy, Sharat C Prasad, Low power CMOS VLSI circuit design, Wiley India, 2000
T3	P Rashinkar, Paterson and L. Singh, ―Low Power Design Methodologies‖, Kluwer Academic, 2002

Reference books:

R1	J.B.Kulo and J.H Lou, ―Low voltage CMOS VLSI Circuits‖, Wiley, 1999
R2	A.P.Chandrasekaran and R.W.Broadersen, ―Low power digital CMOS design‖, Kluwer,1995
R3	Abdellatif Bellaouar, Mohamed I Elmasry, Low power digital VLSI design, Kluwer Academic, 95
R4	Anatha P Chandrakasan, Robert W Brodersen, Low power digital CMOS Design, Kluwer 6
R5	Academic, 1995 Christian Piguet, Low power CMOS circuits, Taylor & Francis, 200
R6	Kiat Seng Yeo, Kaushik Roy, Low voltage, low power VLSI sub systems, Tata McGraw Hill, 2004

Web links and Video Lectures (e-Resources):

1.	https://tinyurl.com/low-power-vlsi (Course Website)
2.	https://www.youtube.com/watch?v=oL8SKNxEaHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM (CMOS Digital VLSI Design) NPTEL Course by Sudeb Dsas Guptha IIT Roorke
3	https://www.youtube.com/watch?v=lRpt1fCHd8Y&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk (VLSI Physical Design) NPTEL Course by Indranil Sen Guptha IIT Kharagpur

Assessment Schedule:

S.N.	Assessment Type	Content	CO	Duration	Marks	Date
1.	**IA Test 1**	Module 1 , 2 & 3(Part I)	1,2,3	1.30 min	50	17.03.26
2.	**IA Test 2**	Module 3(Part II) 4 & 5	3,4	1.30 min	50	06.05.26
					25	
3.	**Unit Test**	Module 1 , 2 & 3(Part I)	1,2,3	1 hour	10	14.03.26
4.	**Assignment / Exempted for i)MOOC-Physical Design ii) IISC ISWDP Certified**	Module 3(Part II) 4 & 5	3,4	1 hour	10	30.04.26
					20	
5.	**Quiz**	Module 1,2,3,4,5	1,2,3,4	20Min	05	10.05.26
6.	Semester End Examination	Module 1, 2, 3, 4 & 5	1,2,3,4	03	50	

***RB** – Text Book/**R**eference **B**ook, ***L** – **L**ecture, **V**- Videos or any other mode, ***RBT** – **R**evised **B**looms' **T**axonomy, **L: T: P: C** – Theory/**L**ecture: **T**utorial: **P**ractical/Drawing: **C**redits, **SEE**: **S**emester **E**nd **E**xamination, **CIE**: **C**ontinuous **I**nternal **E**valuation, **Seminar**: Group of 6-8 students, **Module** 1,2,3,4 & 5,*

The sum of total marks of three tests, two assignments, and seminar will be out of 100 marks and will be scaled down to 50 marks. (As per the scheme), **CIE + SEE = 50 + 50 = 100 marks

Faculty In charge **Course Coordinator** **HoD**