Université de Sousse
Institut Supérieure d'informatique
et des techniques de communications

Matière : Systèmes sur puces SoC

Compte rendu de TP1

Travail réalisé par :

Mokhles El Benna

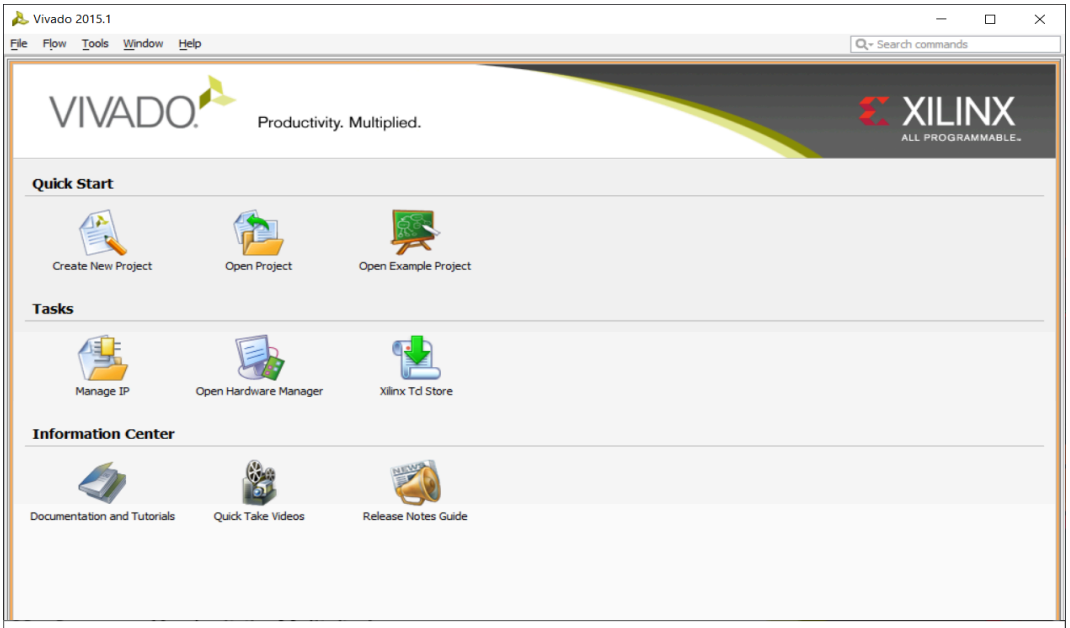
Table des matières

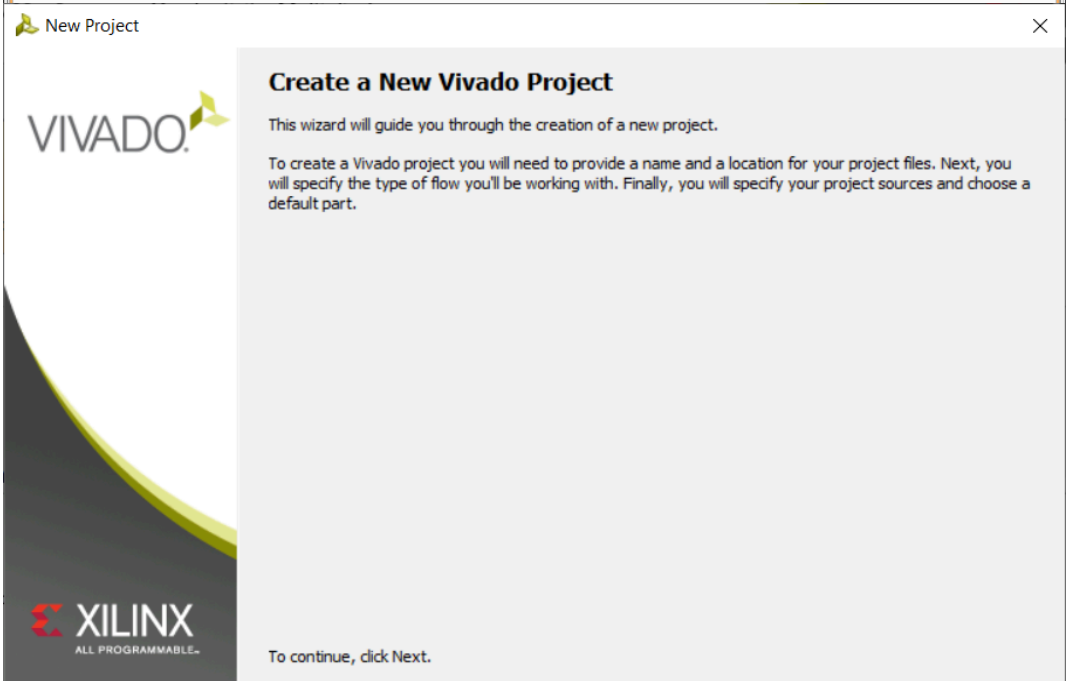
I. Objectif de TP :

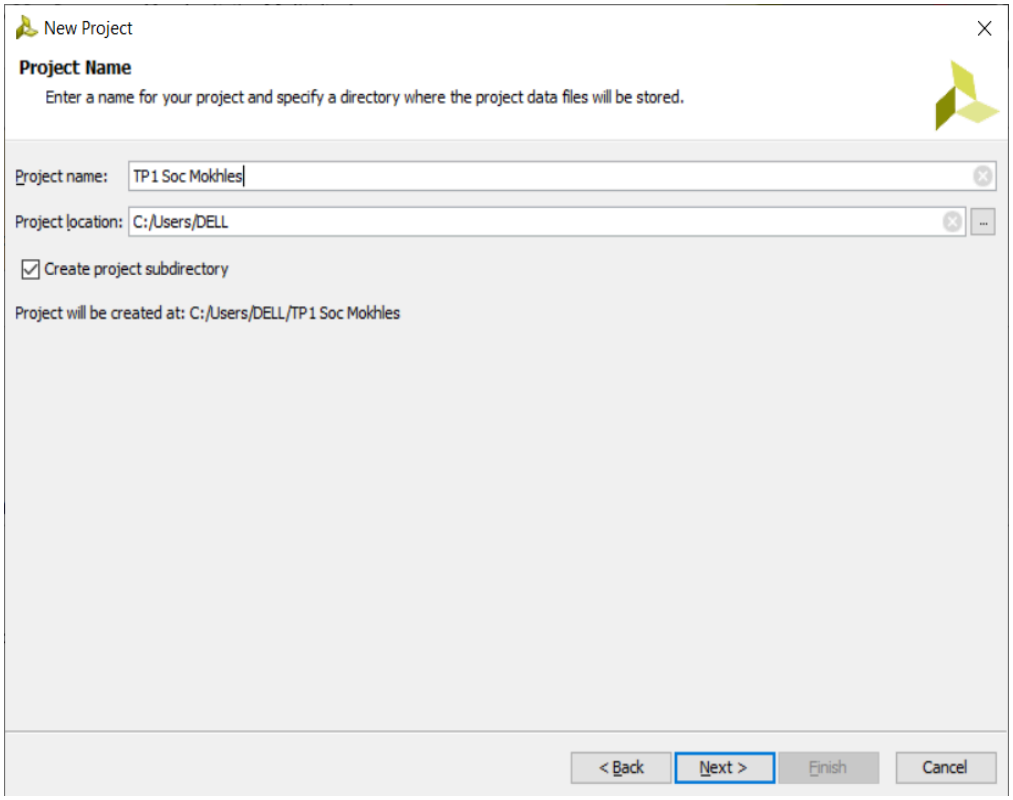
Ce TP est un tutoriel dédié à la familiarisation avec les outils et le flot de conception d'Xilinix en utilisant l'environnement Vivado et SDK.

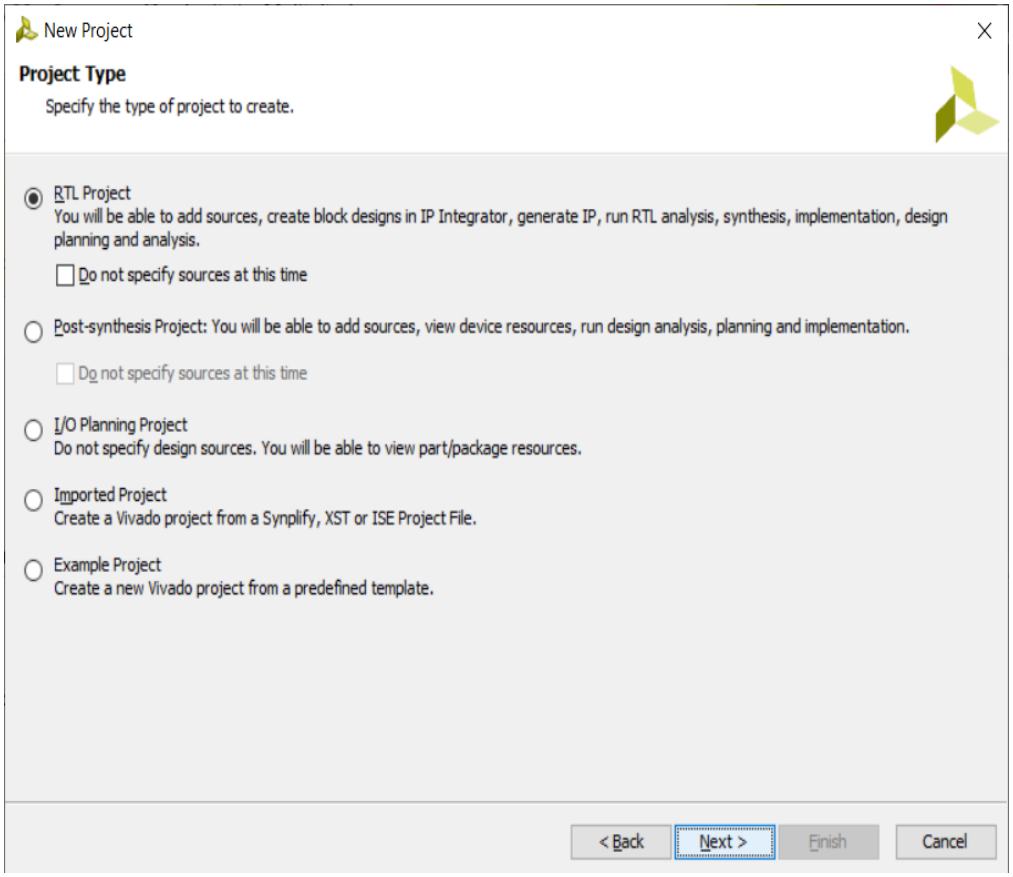
II. Manipulation :

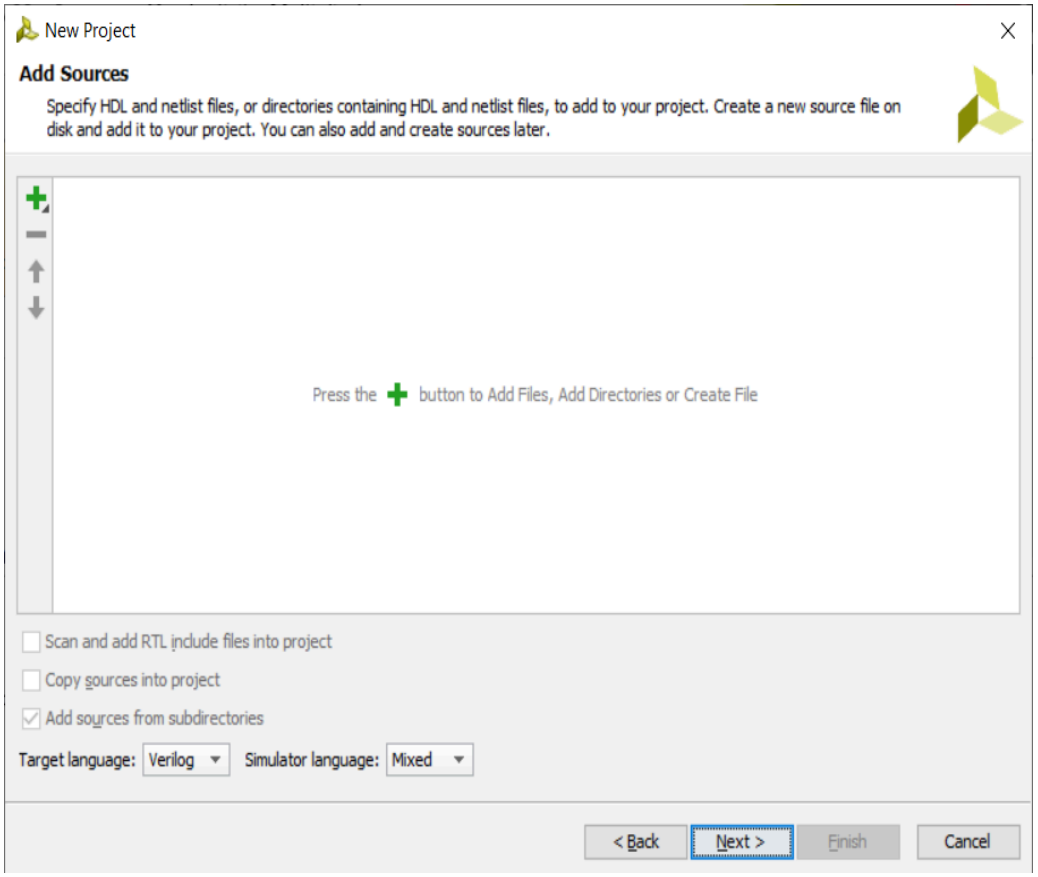
1. Création de projet :

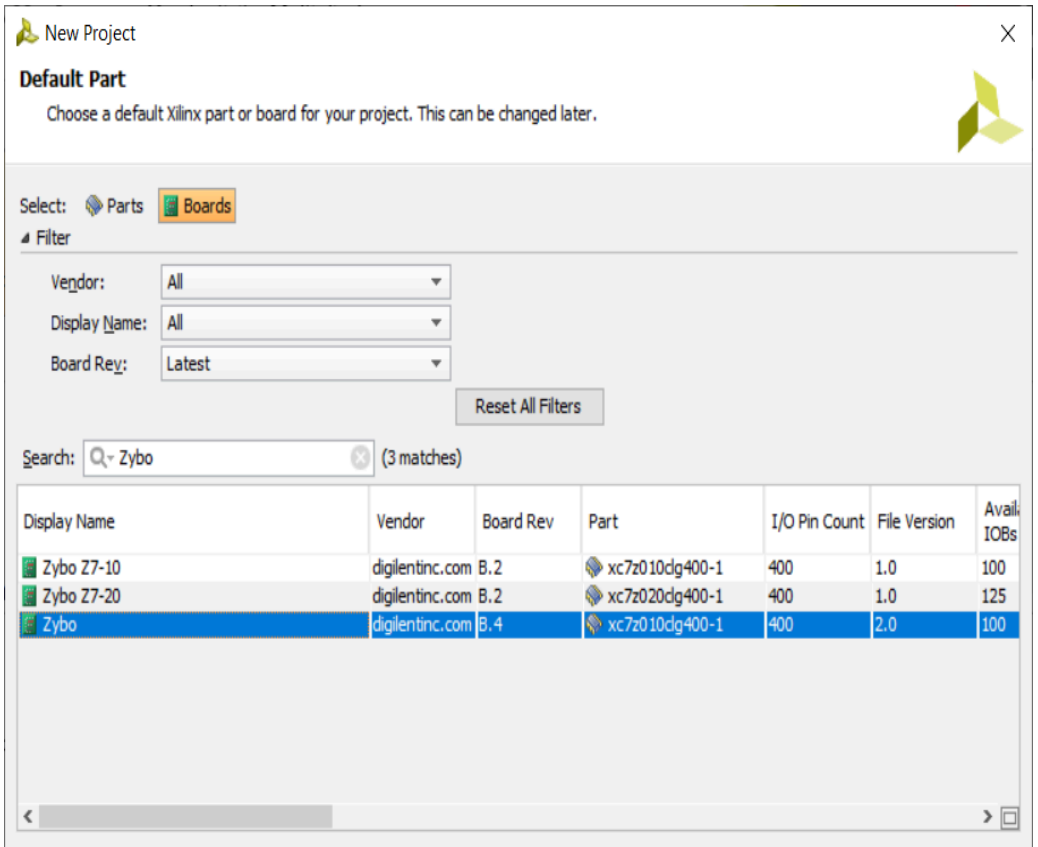




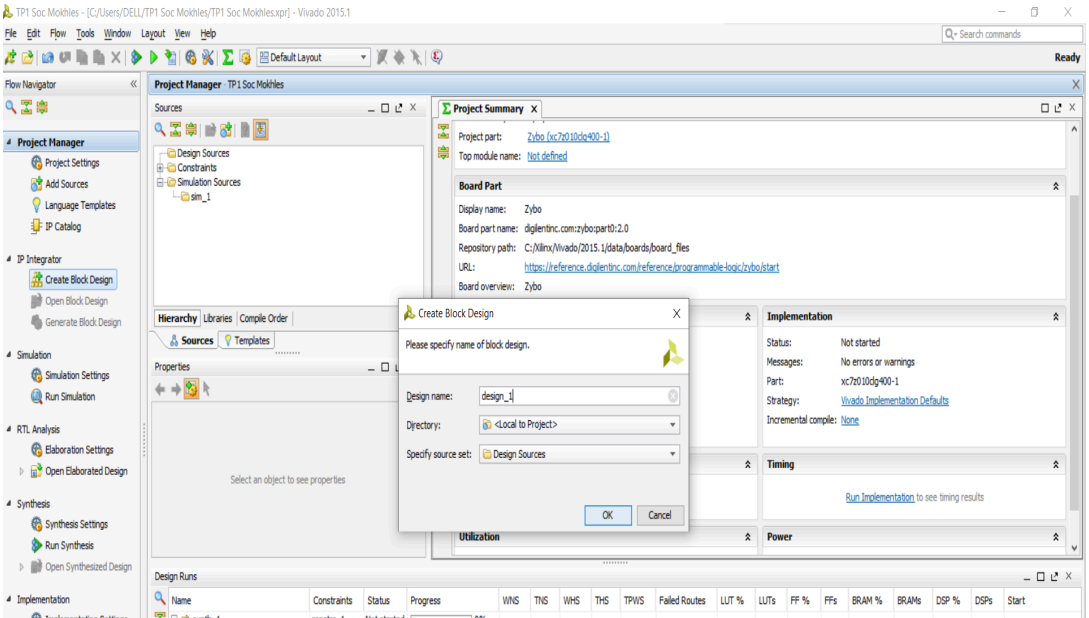

New Project
Project Name
Enter a name for your project and specify a directory where the project data files will be stored.
Project name: TP1 Soc Mokhles
Project location: C:/Users/DELL
Create project subdirectory
Project will be created at: C:/Users/DELL/TP1 Soc Mokhles
< Back
Next >
Finish
Cancel

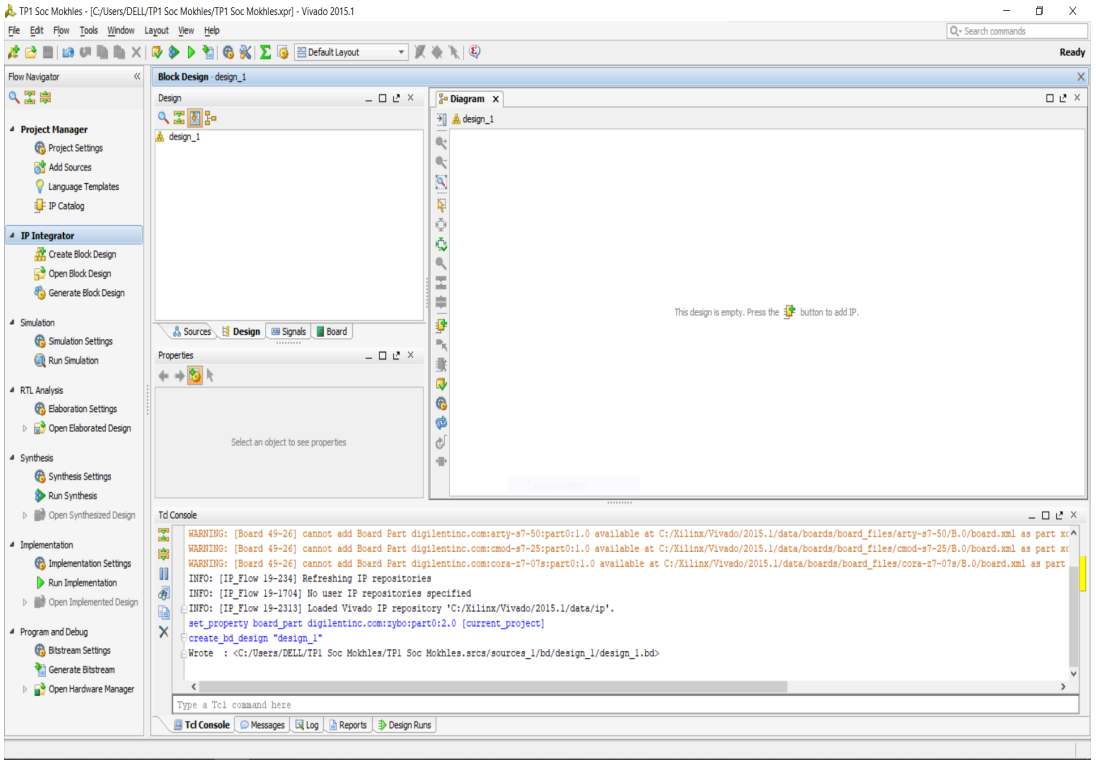

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

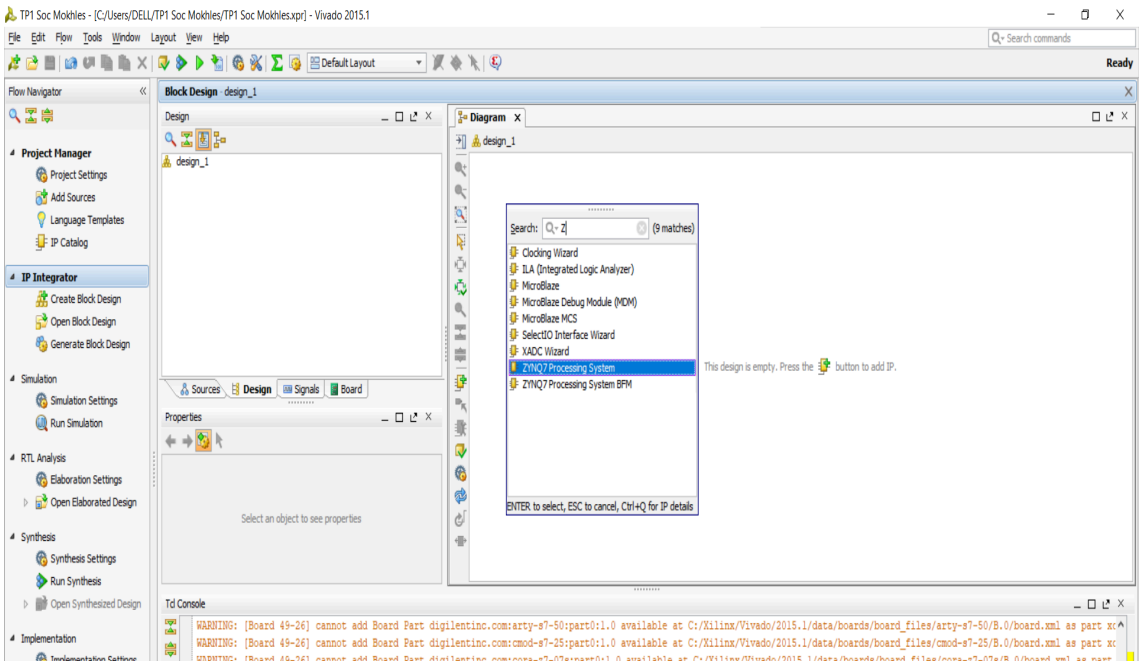

New Project
Add Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Press the button to Add Files, Add Directories or Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: Verilog
Simulator language: Mixed
< Back
Next >
Finish
Cancel


New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Select: Parts Boards
Filter
Vendor: All
Display Name: All
Board Rev: Latest
Reset All Filters
Search: Zybo
(3 matches)
Display Name
Vendor
Board Rev
Part
I/O Pin Count
File Version
Avail IOBs
Zybo Z7-10
digilentinc.com
B.2
xc7z010clg400-1
400
1.0
100
Zybo Z7-20
digilentinc.com
B.2
xc7z020clg400-1
400
1.0
125
Zybo
digilentinc.com
B.4
xc7z010clg400-1
400
2.0
100

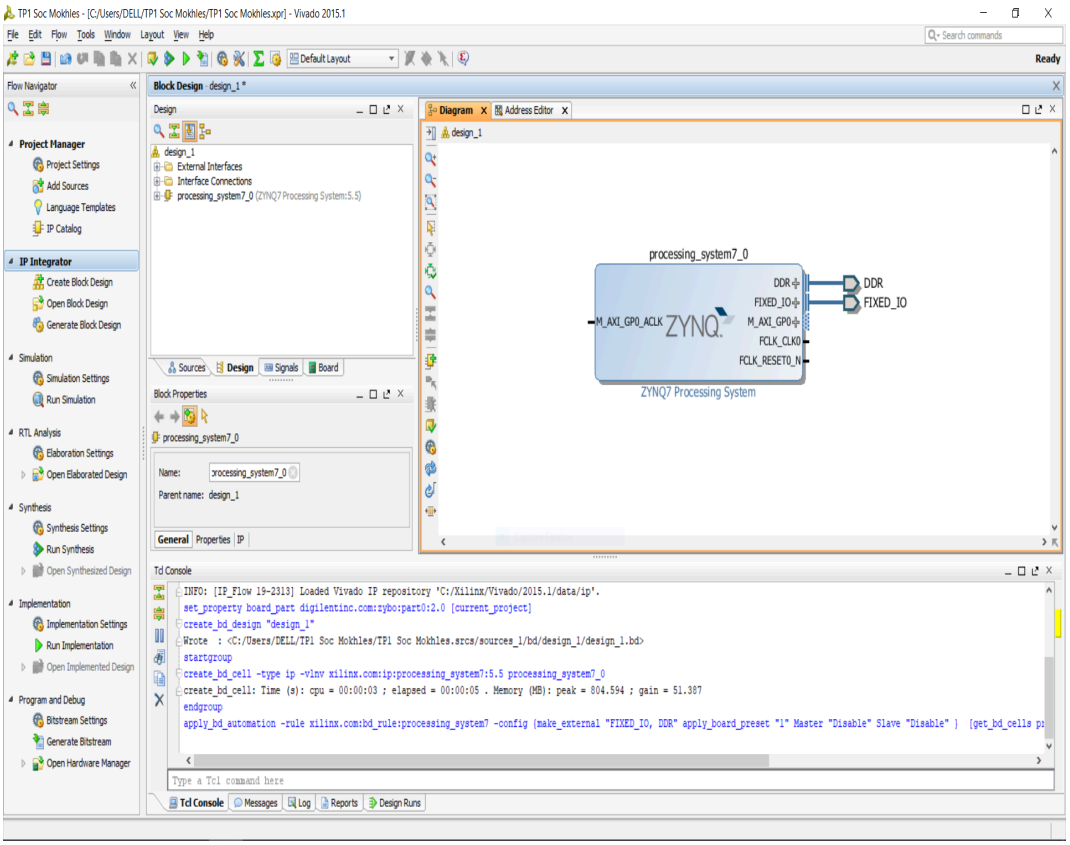
2. Création d'un nouvel Block Design :

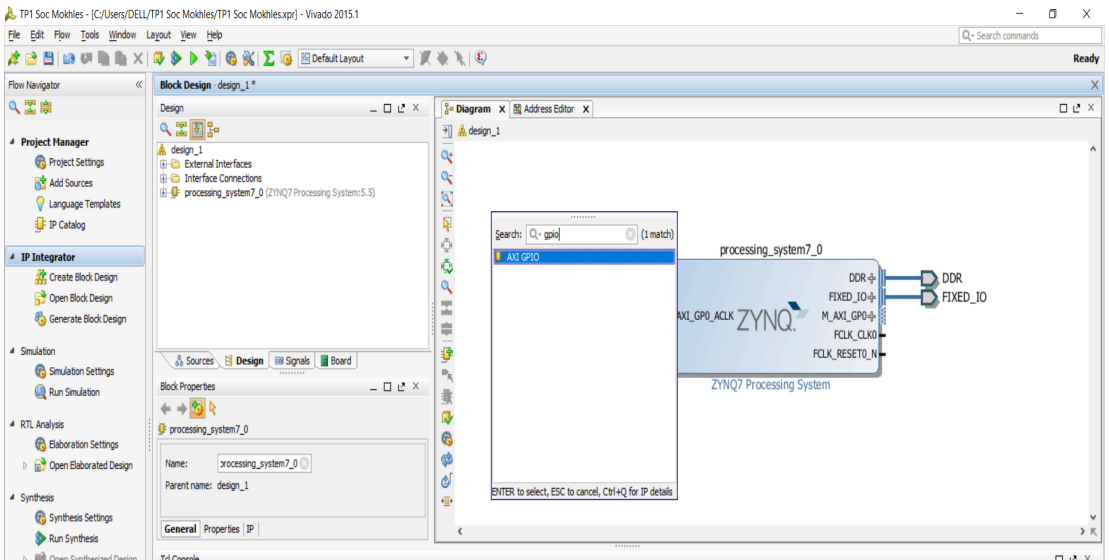


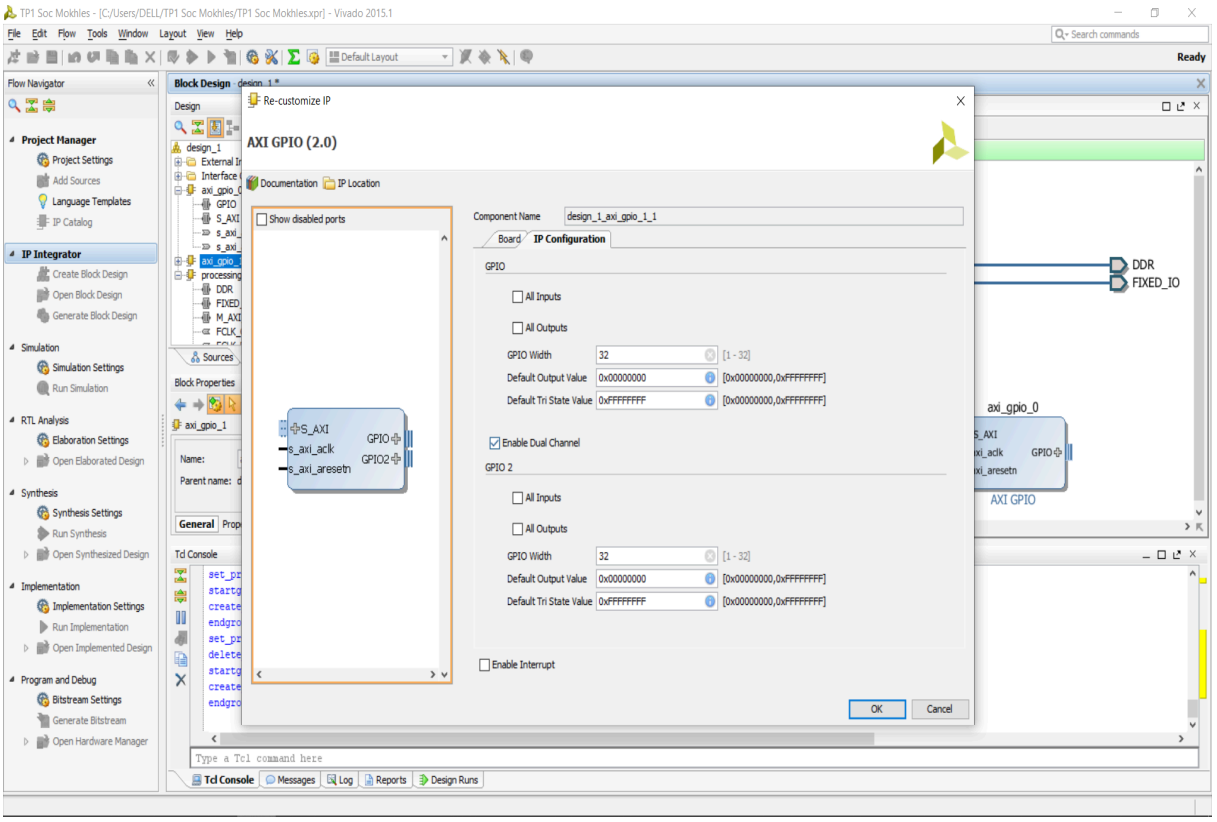

TP1 Soc Mokhles - [C:/Users/DELL/TP1 Soc Mokhles/TP1 Soc Mokhles.xpr] - Vivado 2015.1
File Edit Flow Tools Window Layout View Help
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Implementation Settings
Run Implementation
Open Implemented Design
Program and Debug
Bitstream Settings
Generate Bitstream
Open Hardware Manager
Block Design - design_1
Design
design_1
Sources Design Signals Board
Properties
Select an object to see properties
Diagram
design_1
This design is empty. Press the button to add IP.
Tcl Console
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:arty-s7-50:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/arty-s7-50/B.0/board.xml as part xc
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:cmod-s7-25:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/cmod-s7-25/B.0/board.xml as part xc
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:cora-z7-07s:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/cora-z7-07s/B.0/board.xml as part
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2015.1/data/ip'.
set_property board_part digilentinc.com:zybo:part0:2.0 [current_project]
create_bd_design "design_1"
Wrote : <C:/Users/DELL/TP1 Soc Mokhles/TP1 Soc Mokhles.srcs/sources_1/bd/design_1/design_1.bd>
Type a Tcl command here
Tcl Console Messages Log Reports Design Runs

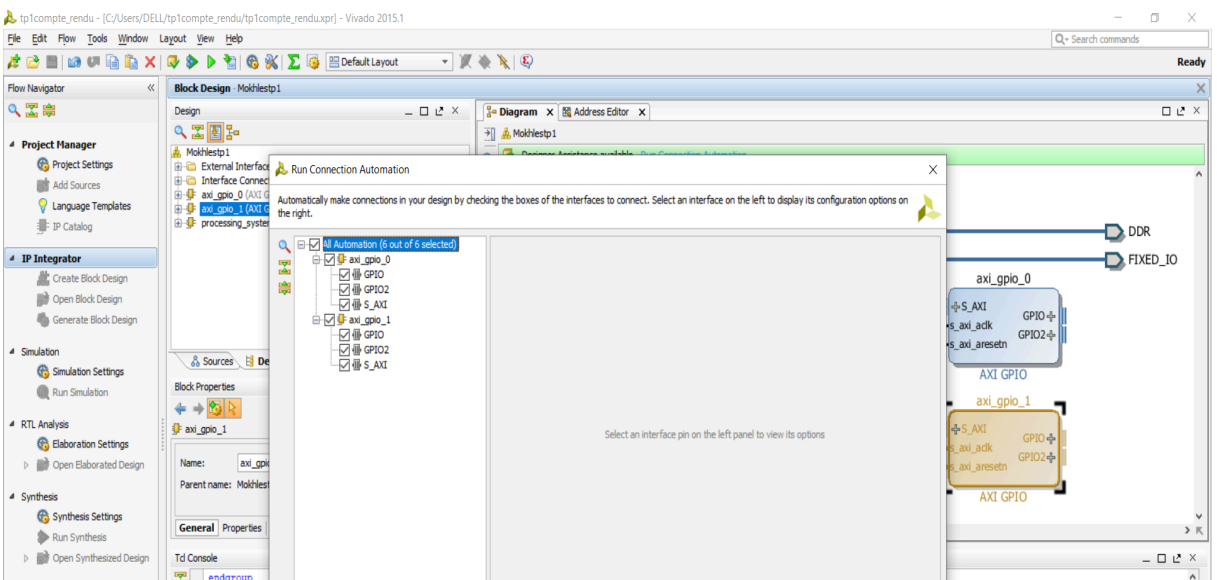

TP1 Soc Mokhles - [C:/Users/DELL/TP1 Soc Mokhles/TP1 Soc Mokhles.xpr] - Vivado 2015.1
File Edit Flow Tools Window Layout View Help
Default Layout
Ready
Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design
Implementation
Block Design - design_1
Design
design_1
Sources Design Signals Board
Properties
Select an object to see properties
Diagram
design_1
Search: Z (9 matches)
Clocking Wizard
ILA (Integrated Logic Analyzer)
MicroBlaze
MicroBlaze Debug Module (MDM)
MicroBlaze MCS
SelectIO Interface Wizard
XADC Wizard
ZYNQ7 Processing System
ZYNQ7 Processing System BFM
This design is empty. Press the button to add IP.
ENTER to select, ESC to cancel, Ctrl+Q for IP details
Tcl Console
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:arty-s7-50:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/arty-s7-50/B.0/board.xml as part xc
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:cmod-s7-25:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/cmod-s7-25/B.0/board.xml as part xc

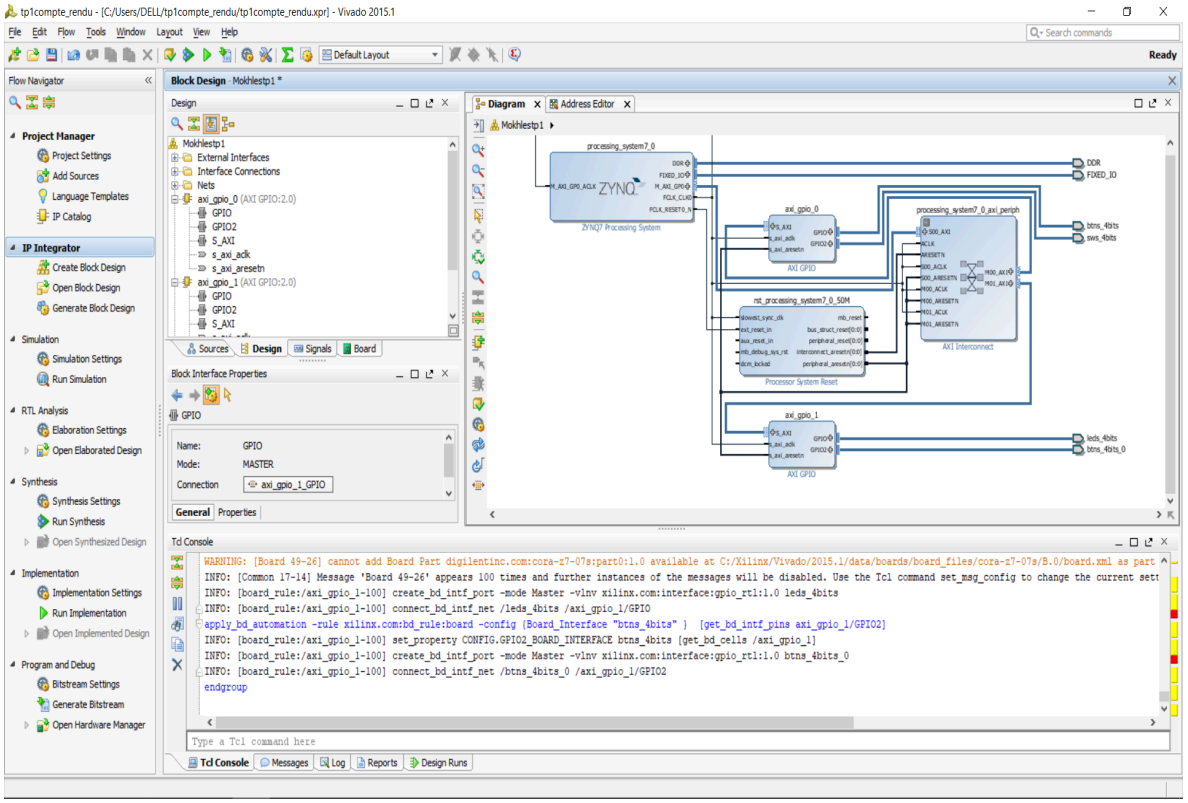
3. Ajout des blocs Zynq IP & GPIO :

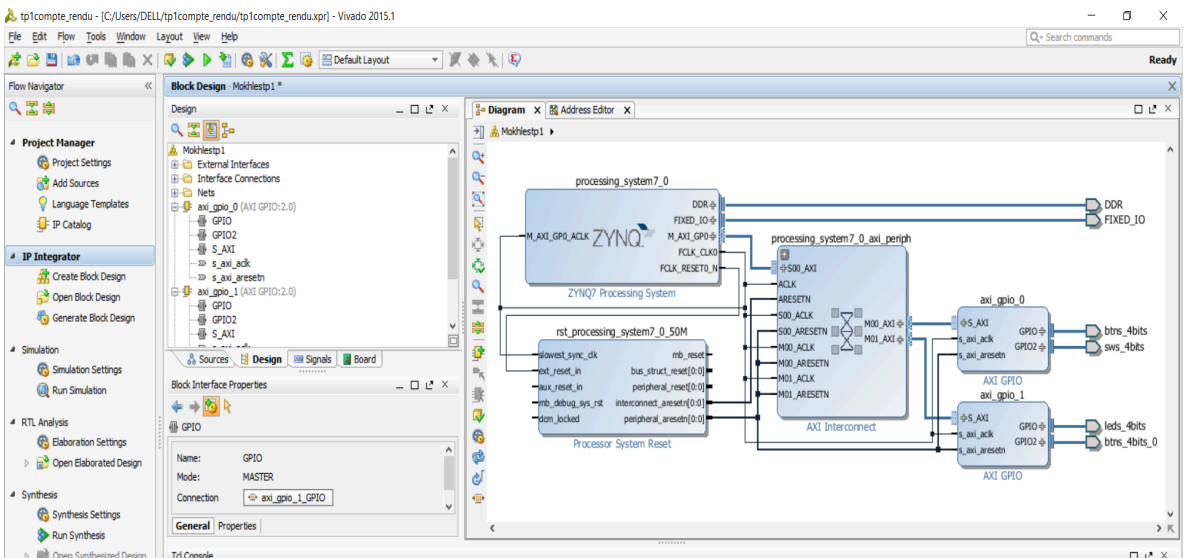


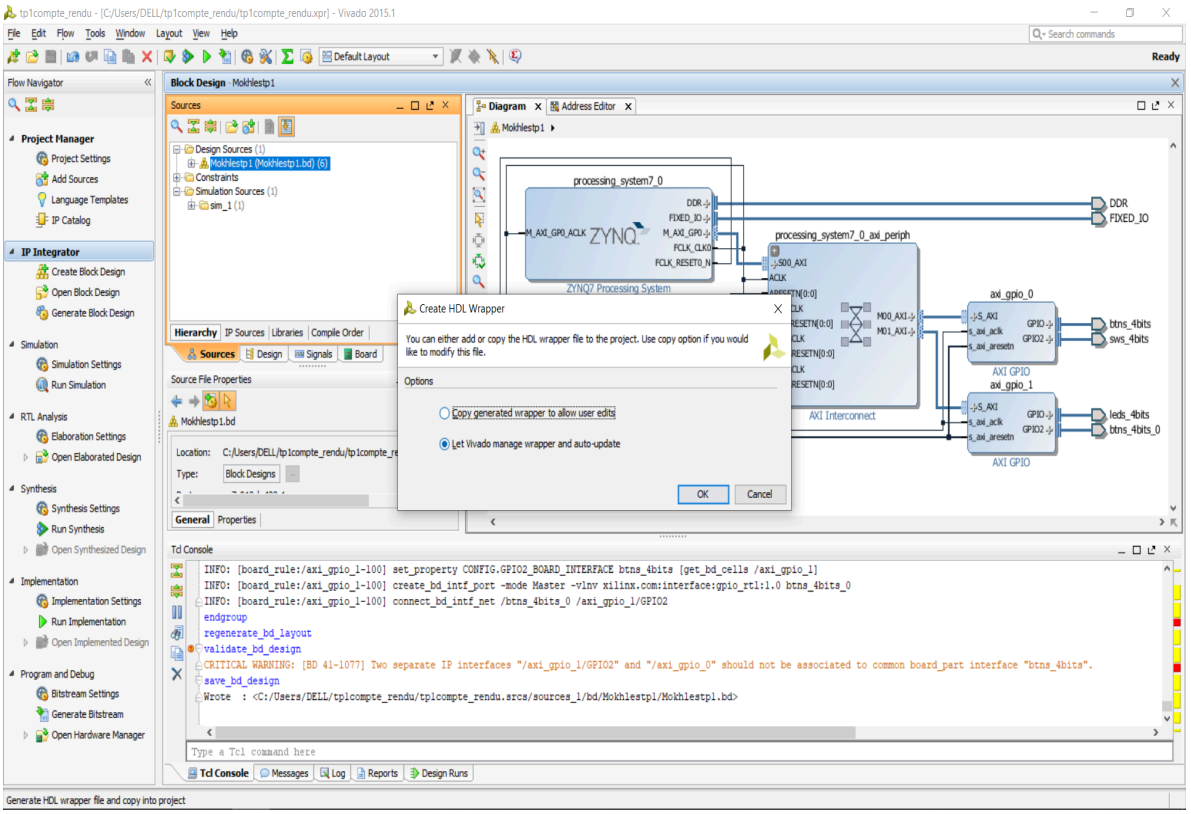


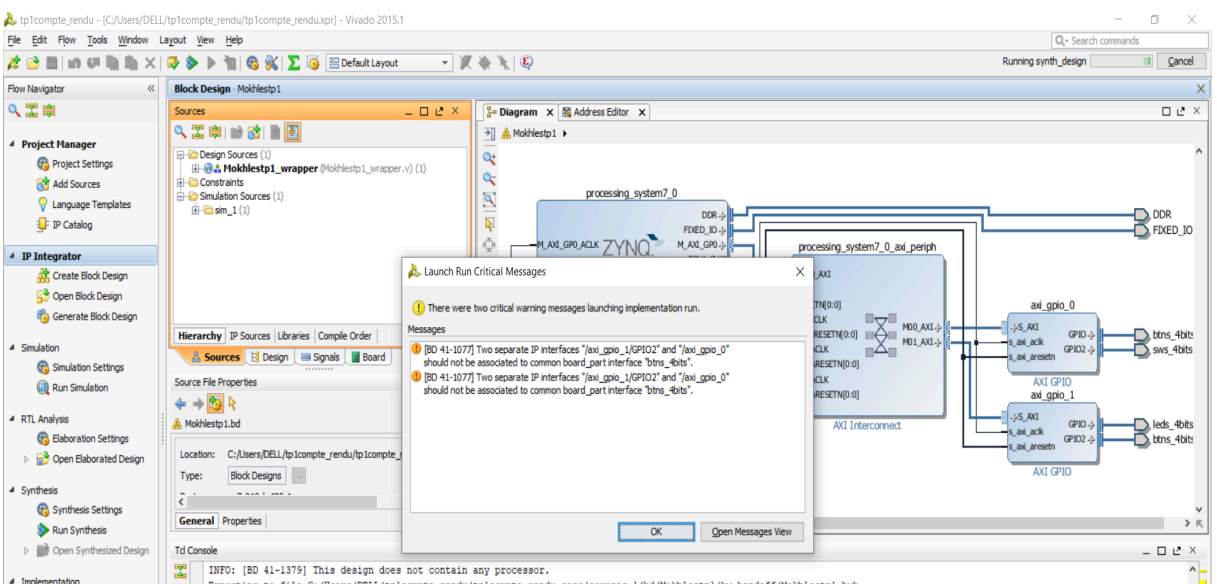

Re-customize IP
AXI GPIO (2.0)
Documentation
IP Location
Show disabled ports
Component Name
design_1_axi_gpio_1_1
Board
IP Configuration
GPIO
All Inputs
All Outputs
GPIO Width
32
Default Output Value
0x00000000
Default Tri State Value
0xFFFFFFFF
Enable Dual Channel
GPIO 2
Enable Interrupt
OK
Cancel
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
GPIO2
DDR
FIXED_IO
axi_gpio_0
AXI GPIO

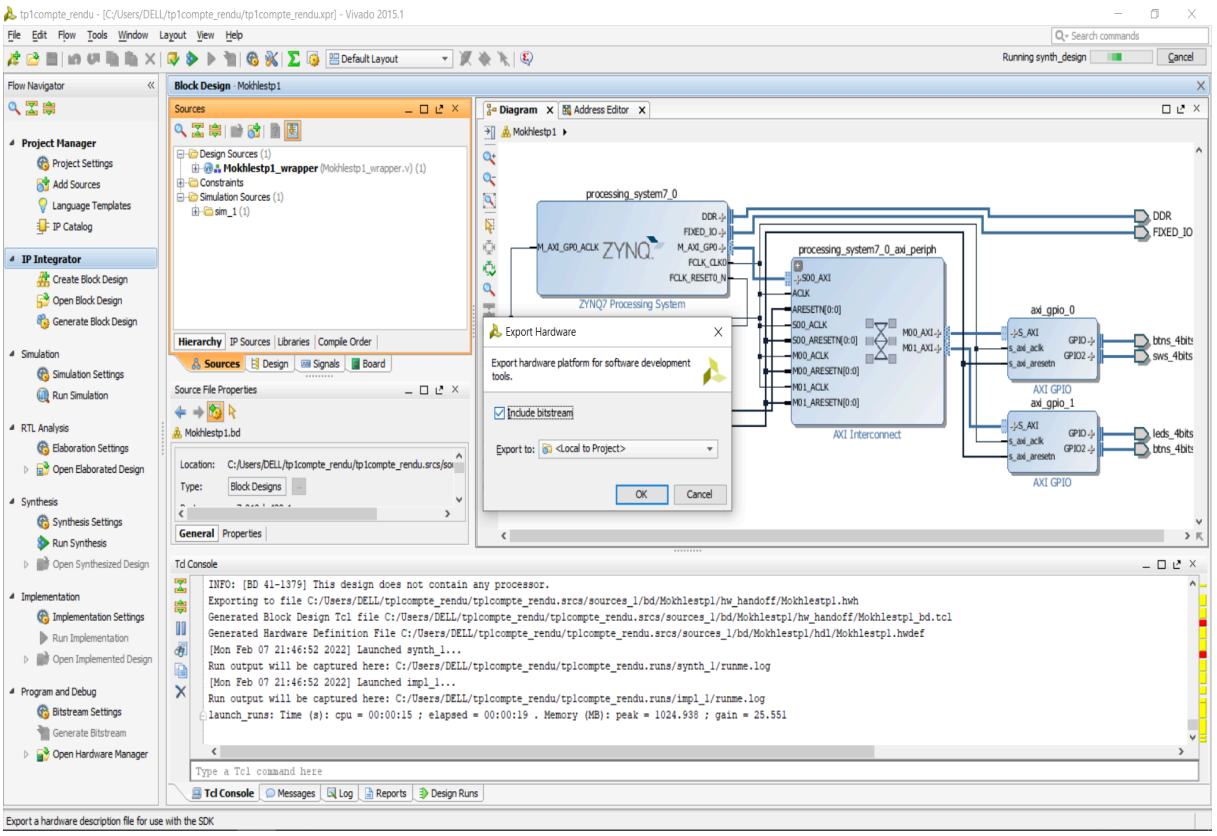

Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (6 out of 6 selected)
axi_gpio_0
GPIO
GPIO2
S_AXI
axi_gpio_1
Select an interface pin on the left panel to view its options
DDR
FIXED_IO
AXI GPIO


tp1compte_rendu - [C:/Users/DELL/tp1compte_rendu/tp1compte_rendu.xpr] - Vivado 2015.1
Block Design - Mokhlestp1 *
Diagram
Address Editor
processing_system7_0
ZYNQ7 Processing System
axi_gpio_0
AXI GPIO
processing_system7_0_axi_periph
AXI Interconnect
rst_processing_system7_0_50M
Processor System Reset
axi_gpio_1
DDR
FIXED_IO
btns_4bits
sws_4bits
leds_4bits
btns_4bits_0
Tcl Console
WARNING: [Board 49-26] cannot add Board Part digilentinc.com:cora-z7-07s:part0:1.0 available at C:/Xilinx/Vivado/2015.1/data/boards/board_files/cora-z7-07s/B.0/board.xml as part
INFO: [Common 17-14] Message 'Board 49-26' appears 100 times and further instances of the messages will be disabled. Use the Tcl command set_msg_config to change the current sett
INFO: [board_rule:/axi_gpio_1-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl:1.0 leds_4bits
INFO: [board_rule:/axi_gpio_1-100] connect_bd_intf_net /leds_4bits /axi_gpio_1/GPIO
apply_bd_automation -rule xilinx.com:bd_rule:board -config {Board_Interface "btns_4bits" } [get_bd_intf_pins axi_gpio_1/GPIO2]
INFO: [board_rule:/axi_gpio_1-100] set_property CONFIG.GPIO2_BOARD_INTERFACE btns_4bits [get_bd_cells /axi_gpio_1]
INFO: [board_rule:/axi_gpio_1-100] create_bd_intf_port -mode Master -vlnv xilinx.com:interface:gpio_rtl:1.0 btns_4bits_0
INFO: [board_rule:/axi_gpio_1-100] connect_bd_intf_net /btns_4bits_0 /axi_gpio_1/GPIO2
endgroup
Type a Tcl command here


tp1compte_rendu - [C:/Users/DELL/tp1compte_rendu/tp1compte_rendu.xpr] - Vivado 2015.1
Block Design - Mokhlestp1 *
processing_system7_0
ZYNQ7 Processing System
axi_gpio_0
AXI GPIO
processing_system7_0_axi_periph
AXI Interconnect
rst_processing_system7_0_50M
Processor System Reset
axi_gpio_1
DDR
FIXED_IO
btns_4bits
sws_4bits
leds_4bits
btns_4bits_0


Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
OK
Cancel
Generate HDL wrapper file and copy into project


Launch Run Critical Messages
There were two critical warning messages launching implementation run.
Messages
[BD 41-1077] Two separate IP interfaces "/axi_gpio_1/GPIO2" and "/axi_gpio_0" should not be associated to common board_part interface "btns_4bits".
[BD 41-1077] Two separate IP interfaces "/axi_gpio_1/GPIO2" and "/axi_gpio_0" should not be associated to common board_part interface "btns_4bits".
OK
Open Messages View



4. Résultat final :