Notes and action items of the Pisa workshop

1. **Constraints and requirements (Christoph)**
2. **Layout and Simulation (Armin, Fabrizio)**
    a. **Armin presentation:**
    vertex layout: is first layer on the beam pipe feasible? power from MAPS is only <20% of the beam pipe. How much vibrations induced during operations (vacuum pumps for instance)?
    the point of going inside the beam pipe is tricky and accelerator physicists says it would be very hard to control synchrotron radiation. They even say that the 1 cm radius beam pipe is very difficult
    outer vertex layout
    micro-channel cooling: How thin can the sensors be?
    Size of periphery in stitching -> Could be reduced significantly (W. Snoys)
    Other questions:
    Layer before lumical and inner timing layer (same technology as silicon wrapper? Benefits?)
    Redundancy in design
    Time resolution and integration time: Need to get firm requirements
    b. **Maria presentation:**
    Benefit of >2 T to be studied in detail, dependence on optics
    No impact of short barrel on impact parameter resolution, but on momentum resolution (will be added to backup)
    Anna: does the short barrel design impact the services routing?
    c. **Stefano presentation:**
    Mechanism for fast power-off of Belle II vertex detector -> Is this something an FCC-ee VXD should also be able to do?
    Carbon fibre solid thermal conductor: 380 μm thickness
    d. **Emmett**
    99% signal efficiency and 60% background rejection using only information of a single cluster. Higher rejection possible if using information from double-sided sensors. Depends on momentum (and physics process) -> May be bad for low-momentum physics
    Comment that NN could be run on whole pixel matrix for further improvements
    e. **Jessy**
    Question of mobility value to use iin small-electrode MAPS -> No TB information on this yet
    Eventually tune digitiser to TB/lab results
    May need different level of detail for different applications (some very precise e.g. to study hit rate, some less precise but faster for physics analysis)
    f. **General discussion points:**
        i. **Reconstruction software for integrated study of vertex+gaseous tracker + silicon wrapper around the corner**
            1. **Need to develop this centrally, together**

2. **Compare VXD layouts in full simulation e.g. also in terms of jet flavour tagging**

ii. **Final uncertainty on physics observable to actually compare layouts**

iii. **Need PhD students to contribute to high-level reconstruction and case studies**

iv. **$B^0 \rightarrow K^{*0} \tau^+\tau^-$, strange Yukawa, …?**

v. **Integrated optimisation of inner vertex + beam pipe (maybe it's overall better to be at larger radius but have a lower-X_0 beam pipe instead?)**

3. **Sensors R&D (Anna, Attilio)**

Topics for discussion

Inner vertex:

- it seems 3-5 um resolution can be achieved with charge sharing starting from 15-25 um pitch, either using geometry and digital readout (ARCADIA's presentation) or pulse height measurement (CE65 presentation).
  OCTOPUS: Novel cross shaped read-out should provide 3 um resolution
  ARCADIA: can the pixel size be reduced to achieve resolution below 4.6 um?
- Is 100 MHz/cm2 readout demonstrated?
  - are transceivers adequate?
    - Arcadia limited to 30 MHz/cm2,
    - MOSAIX has 10 Gbps transmitter: is that tested?
  - readout architectures without clock distribution are a key to low power: both ARCADIA and Octopus are promising, but need a full column 2 cm to verify there is no clogging in the readout architecture: timescale?
- Time resolution
  - do we have any request for ps resolution in the inner vertex? Probably not…
  - which time stamping capability is needed for efficient background rejection?
  - is that compatible with the power budget? (hope the mechanics session will provide some information about measured cooling capabilities)
  - OCTOPUS has released significantly the timing and power constraints for the intermediate step. Can it be more ambitious?
- Stitching:
  - which is the ultimate dead space for a 2D stitched solution (curved layout) or for just 1D stitching (like Belle2 or MOSAIX)
- 3D integration
  - can we benefit from 3D integration?
  - is this a possible way to achieve simultaneously a low power dissipation (<50 mW/cm2)and high hit rate capabilities (>100 MHz/cm2)?

- can the 3D integration help to achieve an aggressive timing performance?

Outer Vertex

- Alternative solution can be exploited due to the lower occupancy
    - how AC LGAD can be expanded to pixellated large areas
    - Can 3D integration be useful to separate sensor and readout?
- Are more simulation studies needed to define the requirements?
    - ultimate resolution to be achieved? 50 um pitch may be enough?
    - power consumption
    - material

General items:

- Schedule for access to the foundries
    - LF110 → A framework for common access has been defined within the INFN-LFOUNDRY agreement. Several runs planned between 2026-2028, a possible tool for FCC-ee collaborative design
    - TPSCo 65 → no clear schedule available at this time for R&D on future lepton colliders. How can we mitigate the situation?
    - Others?
- 3D integration
    - is the development timeline of several prototyping runs compatible with the FCC-ee timeline?
    - Is this technology really accessible cost-wise? Are there solution to reduce the entry cost for our community (like sharing different designs on the same wafers)?
- What are the perspectives for technology availability by the time of FCCee: what can we expect will be solved by new nodes?

Summary of Presentations

ARCADIA in LFoundry 110 nm CMOS

presentations by Manuel Rolo and Sabrina Ciarlantini

- A framework for common access has been defined within the INFN-LFOUNDRY agreement
- Several runs planned between 2026-2028, a tool for FCC-ee collaborative design
- Rate capability up to 100 MHz / cm2
- total power density < 30 mW/cm2

--> Resolution of 4.6 um with pixel pitch of 25x25 um2: is it possible to go lower ?

NAPA chip (*Mirella Vassilev*)

- Goals:
    - ns timing resolution
    - Power consumption compatible with large area and low material budget

Design in 65 nm CMOS TPSCo

- Simulation show that low power dissipation can be achieved with time resolution around 1 ns
- NAPA_p2 prototype submitted in CERN ER2 run to further study timing and power trade off, some building blocks of TDC included

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CE-65 ***(Eduardo Ploerer)***:
Lesson learned from analog prototypes
Excellent resolution was obtained in large-matrix 65 nm CMOS test structures at SPS testbeam

- Sub 3 μm spatial resolution for Standard process chips
- 15 μm Modified with Gap process just above 3 μm
- Staggered arrangement shows 16% improvement at 210 e threshold

--> Standard process with higher cluster size looks like the best choice for spatial resolution but it could increase the data rate at L1: should we think about different versions of the sensors for L1 with respect to the other layers?

- A firm timeline to include R&D sensors towards future lepton collider in 65 nm TPSCo is not available at the moment
→ how can we improve the situation?
- On the other side, an innovative approach is emerging from the presentations of Walter Snoeys (CERN) and Artur Apresyan (Fermilab):

Possibility of 3D structures with 65 nm TPSCo sensors wafers (MAPs, LGADs) bonded to 65 nm or 28 nm ASIC wafers by TSMC

- 2 layer wafer stacking offered in this technology will increase cost, but not the thickness, could stack a 65 nm sensor to a 65 nm or 28 nm readout.
- Present evolution towards wafer stacking and 3D integration in mainstream CMOS technology and CMOS imaging sensors for visible light very relevant for future detectors
- At FERMILAB LGAD wafers are being designed for TPSCo 12" wafers to be 3D integrated with 28 nm TSMC timing chips

--> is this a possible way to achieve simultaneously a low power dissipation (<50 mW/cm2)and high hit rate capabilities (>100 MHz/cm2)?

--> can the 3D integration help to achieve an aggressive timing performance?
--> is the development timeline of several prototyping runs compatible with the FCC-ee timeline?
--> Is this technology really accessible cost-wise?

4. **Mechanics (Nicola)**
    a. **beam pipe mock-up: carbon fiber outer shell could be very interesting**
    b. **beam pipe mock-up: vibrational studies**
    c. **beam pipe mock-up: how to connect the inner Vertex**
    d. **beam pipe mock-up: how to connect properly support the lumical and stability measurements**
    e. **beam pipe mock-up: installation sequence**
    f. **service integration: again vibration studies, interplay between relatively heavy and rigid services with very light mechanical structure and air flow**
    g. **service integration: sequence of installation and service connection**
    h. **curved sensors: more experience is needed also from other institutes**
    i. **curved sensors: study different support structures and installation sequence**
    j. **air cooling: vibration and stability studies, different types of fluids (air, nitrogen, helium), temperature of the air etc.**
5. **Readout and Electronics (Carl)**
    a. **Attilo**: serial power and light PCB from DRD3, focus on outer vertex and silicon wrapper. Prototyping based upon ATLASPIX3.1 MAP chip. Study of Al/kapton tapes from CERN shop and from LTU company with Oxford. Issues of temperature susceptibility of Al/kapton - blistering. Is this also a problem for CERN?

       Questions to consider:
        - Al tapes remain a niche process with (?) little commercial traction. How do we secure a stable and reliable process over a 20-25 year time frame?
        - The Serial Power architecture shown was minimal. What about protection and bypass for long serial chains? For ATLAS, at some point this was a no-g

    b. **David Novel FBK** - low mass electronics and MAPS packaging - study based upon ALPIDE and space applications. It is a wafer based process with tab bonding between layers. Palace used as EM solver. Nice process but what about size limitations? What are the longer term prospects for both availability.and evolution
    c. **Anna M** on wireless communication: focus on 60 GHz, RF xcvrs in 65-28 nm CMOS, demonstration at IHEP-CAS, using polarization methods to control

interference. Consider the use of TSV in the MAPS chips to pass RF radially out to the larger radius layers.
Questions - rad tolerance?, how much power is required?, what would a full system look like as a guide to work through whether (for example) we need to pass signals through layers, etc.

d. **Christoph** on trigger/triggerless readout: LEP used minimal triggers. He did a rough calculator of rates, data requirements, etc, concluded data and IPC were of similar scale, triggerless probably doable but simple low bias trigger still looked attractive
Questions - needs detailed considerations of how well we would understand the trigger efficiency. In the end, what would be harder - to make and understand the trigger with the required precision, or to have a system which could run triggerless and handle the BW. What about rates from other subsystems ie CALOR etc, Note TDAQ meeting at CERN Nov 6