OCP HPC Sub Project

Minutes - 11/01/2022

Meeting Transcript :
https://docs.google.com/document/d/1swYJ3Xzu5cFLAjsEWVMK2LdHEkg_otea/edit

Attendees

Attendee	Affiliation	11/01/2022
Phillipe Boisvert	Boyd	x
Matt Burns	Samtec	x
Kevin Cameron	Consultant	x
Allan Cantle	UntetherAI	x
Kinny Chen	Neuchips	x
Michael Choi	Samsung	x
Ender Demirel		x
Calum Devlin	CoolIT	x
Trent D'Hooge	LLNL	x
Chris Graves	Samtec	x
Rita Gupta	Sony Playstation	x
Paul Hartke	AMD/Xilinx	x
Zaid Krisberg	SUNY Downstate Medical Center	x
Brent Massey	Individual	x
Diana Pham	Molex	x
Totals		15

Meeting Objectives

Proposed Agenda for this meeting :

1) Introductions to New Attendees.
2) Summary of OCP HPC Activity at the OCP Global Summit
3) Discussion on bootstrapping HPCM around CXL Ecosystem Development

4) AOB

Meeting Discussion Notes

1) **Introductions to New Attendees.**

Kinny Chen - BD Manager Neuchips - participated in OCP global summit 2 weeks ago. Lot of OCP related projects that were interested in. So here to see if its worth joining the HPC SubProject. Requirements in the filed and contribute to the Community.
Neuchips do AI Silicon for recommendation systems.

Allan Cantle - Joined UntetherAI - Title Chief System and Solution architect. Continue working with OCP.

Diana Phan - Molex - picking a couple of subjects from HPC project. IO Side.

Matt Burns - Samtec - marketing manager at Samtec - research these markets and application.

Rita Gupta - Sony Playstation - recently joined in cloud gaming platforms - already using OCP V3 racks - curious as to what's going on.

Brent Massey - working on aggregation of layer 0 through 3 and looking at how we can make Blockchain usable across the world.

2) **Summary of OCP HPC Activity at the OCP Global Summit**

3) **Discussion on bootstrapping HPCM around CXL Ecosystem Development**

One item missing is the memory pooling. Now CXL technologies are available and for HPC environments we can create a memory pooling situation in the data center. With the HPCM architecture and CXL connected memory or storage we can create a memory environment for HPC. Michael's personal view for the future. Right now, so many interface technologies like OpenCAPI, GenZ, CCIX, they were going their own way, CXL is now bringing all the pieces from the other technologies under one umbrella. NVLink protocol is similar to CXL protocol. 16 byte protocol. CXL 3.0 is 64Gb/s PCIe speed. NVLink is now open source and they are also working on CXL. try to solve this memory sharing issue and this is what we can focus on in this workstream.

Broadcom is a heavy contributor to CXL Switching fabric enablement. Intel innovation conference and Samsung at OCP. CXL switch company CXL 2.0.

XConn -
Marvell had CXL memory pool appliance - memory pooling appliance
Elastic Cloud - CXL memory Pooling appliance.

Consider bigger scale like HPC. Optical

Maybe pull together a paper exercise. Look at a particular problem.
Contact CXL Consortium and see if any of their members would be interested in contributing towards the OCP HPC efforts.

CXL TTF - Technical Task Force - under CXL Board. Then many working groups gon on.
Michael represents CXL TTF for Samsung. Right now heavily focusing on CXL fabric enablement. Parallel baseline is already in place and we are working on 3.1 and 4.0. In CXL 4.0 trying to add complete fabric solution. In industry CXL is a little bit behind right now. Mostly working on 1.1 and 2.0. In samsung we have CXL memory expander but there is no CXL switch

CXL expander THe ask is to support the accelerators and mre like a CXL type 2.0. Memory

8 lane single port on CXL expander. 4 lane or 8 lane. Based on 8 lane you can have 4 of them on a 2 socket server.

4) **AOB**