

FACULTY OF SCIENCE
M.Sc. (PHYSICS/PE) III – SEMESTER REGULAR EXAMINATIONS, DEC-2016
DIGITAL LOGIC CIRCUITS
PAPER – III

Time: 3 Hours]

[Max. Marks: 70

Note: Answer all the following questions from Section – A and Section – B

Section – A

(5x4=20)

Answer the following questions in not more than **ONE** page each:

1. Simplify the Boolean expressions i) $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B} + ABC$ ii) $\overline{A}BC + AC$
2. Draw the circuit diagram of NOR Latch and explain its working.
3. Write a short note on LCD display.
4. What are the different modes of DRAM refreshing?
5. Draw the circuit diagram of Johnson's counter and explain its working.

Section – B

(5x10=50)

Answer the following questions in not more than **FOUR** pages each:

- 6 a) Simplify the Boolean expression.

$$Y = \overline{C}(\overline{A}\overline{B}\overline{D} + D) + \overline{A}\overline{B}C + \overline{D}$$

Using K-map method and implement the circuit using NAND gates.

(OR)

- b) Design Full Adder circuit. Draw the circuit diagram of a 4-bit parallel Adder using Full Adders and explain its working.

- 7 a) Draw the circuit diagram of Asynchronous (Ripple) counter and explain its working by drawing the timing diagram and count sequence.

(OR)

- b) Explain the working of one shot (mono stable multi vibrator) by giving its function table.

- 8 a) Draw the circuit diagram of a CMOS NAND gate and explain its working. Discuss about CMOS logic family series characteristics.

(OR)

- b) Explain the working of 3 to 8 line decoder and octal to binary encoder circuits.

- 9 a) Write an essay on semiconductor ROMs.

(OR)

- b) Describe the RAM architecture and discuss about RAM timing diagram.

- 10 a) Design synchronous counter with count sequence 000,010,100,110,000 and implement the circuit.

(OR)

- b) Describe the architecture of PROM, PLA and PAL and mention few applications of them.

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