Report on Two Days-VLSI SYSTEMS CONCLAVE

by **IEEE CAS Society (CASS) (SBC60981AG) in association with SSCS.**

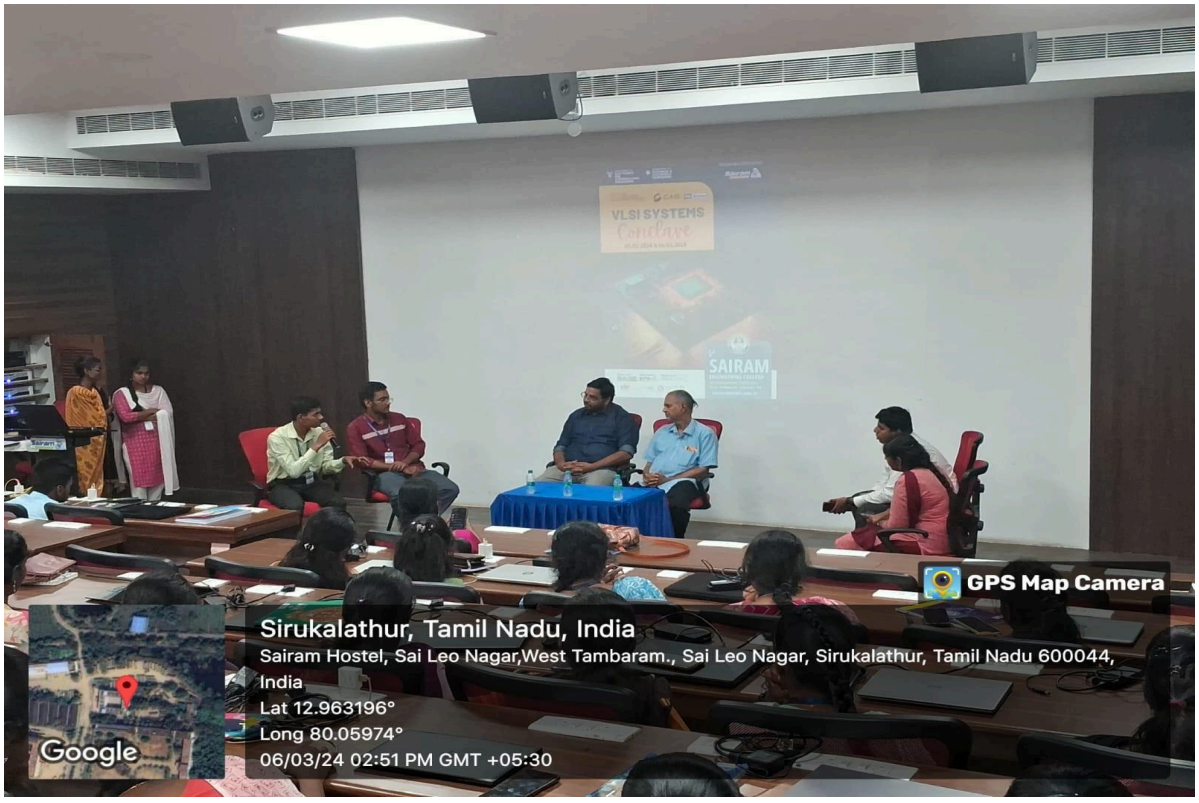
Date: 05.03.24 and 06.03.24
Time : 10.00am to 04.00pm
Venue: Beta Hall, G, Block, Sri Sai Ram Engineering College

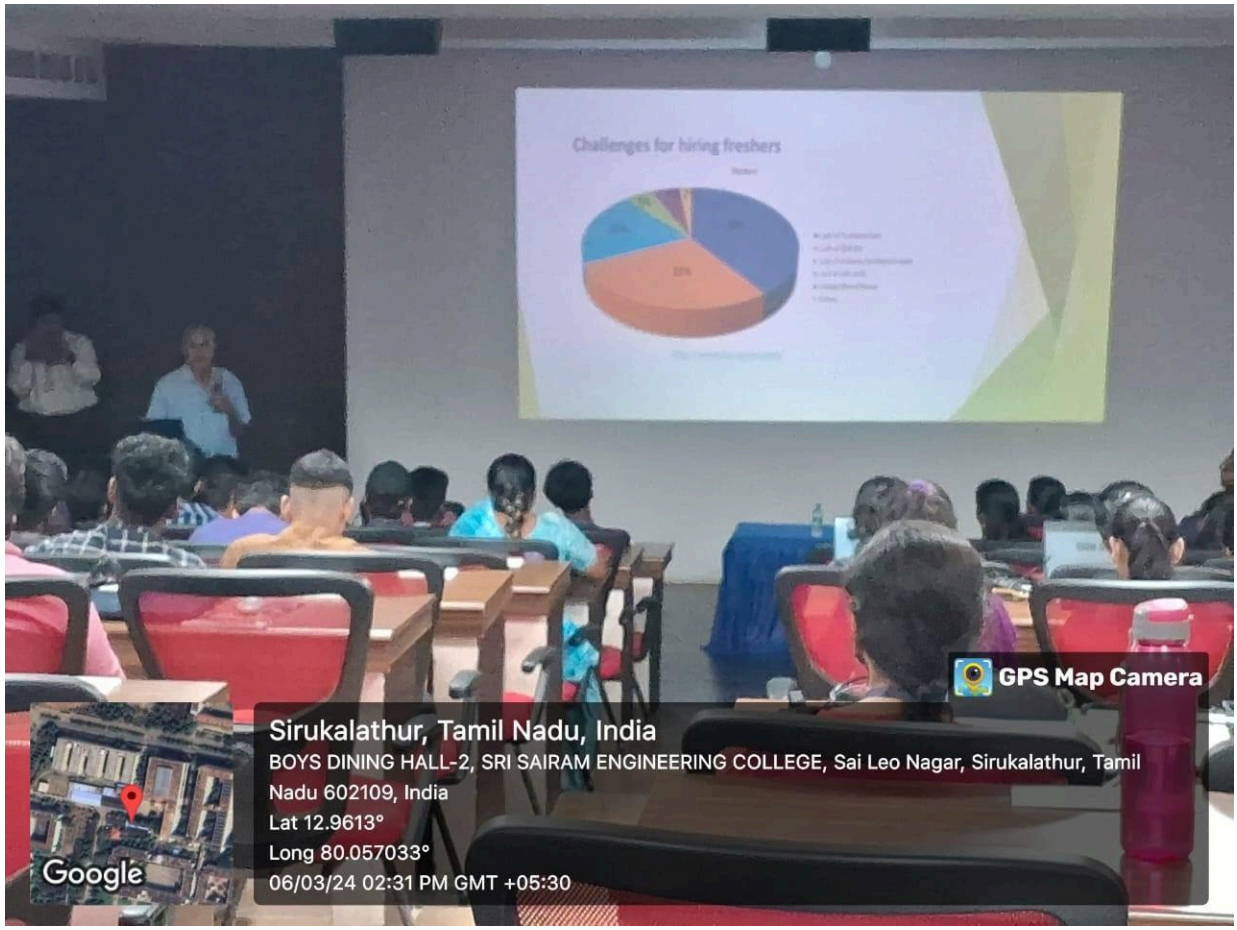
The VLSI Systems Conclave commenced with a welcome address by **Ms. S.Usha,** *Faculty Advisor , IEEE CAS society* followed by an inaugural address by **Mr. Samuel Tensingh,** *Associate Lecturer-VLSI, The University of Sydney, Australia* on the first day. The day's highlight included a hands-on session focused on Analog circuit layout, employing the Cadence tool. Attendees gained practical insights into the intricacies of designing analog circuits in the realm of VLSI systems. This session was handled by **Mr. S.Vinoth Kumar, Mr, Balaji and Mrs. G.Jayanthi**, *AP's from Sri Sairam Engineering College.*

On the second day, the conclave continued with an informative session by **Mr. T.A.Bharathwaj,** *Principal Design Engineer, Microchip Technologies*, and **Mr. S. Hariharan**, *Freelancer & Adjunct Faculty – IIITDM, Kancheepuram* on Physical design, delving into the complexities of shaping VLSI components for optimal functionality. Additionally, a panel discussion brought together experts to explore current trends, challenges, and future prospects in the field. Then the Valedictory function was held and the Vote of Thanks was proposed by **Dr.L.Kurinjimalar**, *Advisor, IEEE SSCS.*

Overall, the conclave provided a comprehensive platform for participants to deepen their understanding of VLSI systems, from practical circuit layout using advanced tools to the nuanced aspects of physical design. The collaborative environment fostered insightful discussions and networking opportunities, contributing to the overall success of the event.

We thank our CEO sir, Principal sir, Dean (Academics) &HOD -ECE and HOD-EEE whose guidance has been instrumental in bringing this event to fruition.

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