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Total No. of Questions: [09]

B. Tech. CSE (Internet or Things and Cyber Security Including Block Chain Technology)
(Semester – 3rd)

DIGITAL ELECTRONICS
Subject Code: BCSES1-303
Paper ID: [23113604]

Time: 03 Hours **Maximum Marks: 60**

Instruction for candidates:
1. Section A is compulsory. It consists of 10 parts of two marks each.
2. Section B consist of 5 questions of 5 marks each. The student has to attempt any 4 questions.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

Section – A **(2 marks each)**

Q1. Attempt the following:

a) If inputs to a 3-input XOR gate in Hex are 2A, 3B and 4C respectively, find its output in Octal.

b) Realize the truth table of the Boolean logic function: $F = A.\overline{B} + \overline{A}.C + B.\overline{C}$ along with its POS standard representation.

c) Construct i) AND and ii) NAND using NOR gates only.

d) Perform binary arithmetic $(10010)_2 - (11110)_2$ using 2's complement.

e) Compare and contrast various performance characteristics of TTL and CMOS logic family, qualitatively and quantitatively.

f) Realize the Truth table and Excitation table of a NAND based Set-Reset Flip-Flop.

g) List the implications of Serial and Parallel transfer of data in Registers, on Number of IC Pins, Time-taken and Destructive/Non-destructive readout.

h) Illustrate the utility of a Sample and Hold circuit in A/D converters.

i) Compare and contrast PLA and PAL type of programmable logic devices.

j) Classify and list various characteristics of memories.

Section – B **(5 marks each)**

Q2. Implement the function: $F = \sum m\,(1,\ 2,\ 4,\ 6)$ using i) NAND gates only ii) NOR gates only.

Q3. Realize a n-bit Carry Look Ahead Adder and compare its time delay with a Carry Ripple Adder for n=16.

Q4. Explain Racing in Flip Flops? Illustrate, how is it checked in JK Flip Flop?

Q5. Describe the working and salient features of a Dual Slope A/D converter.

Q6. Implement a full Subtractor using i) Multiplexers, ii) Decoders only.

Section – C **(10 marks each)**

Q7. Minimize the Boolean function, $Z = \sum m\,(2,\ 3,\ 4,\ 5,\ 13,\ 15) + d\,(8,\ 9,\ 10,\ 11)$ using Karnaugh Map and implement both original and simplified circuits using 2-inputs NAND gates only. Find the percentage saving achieved.

Q8. What is a digital counter? Design a self-starting synchronous counter using D Flip Flops with a counting sequence as 2, 6, 4, 0, 3 and repeat.

Q9. Write a complete technical note on *any two* of the following:

i) Error detecting and correcting codes

ii) Tri-state logic
iii) Field Programmable Gate Array and its applications