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Prof. Smilkstein
Very Large Scale Integration
29 April 2024

Transistor Level 8 Bit SAP-1 Computer

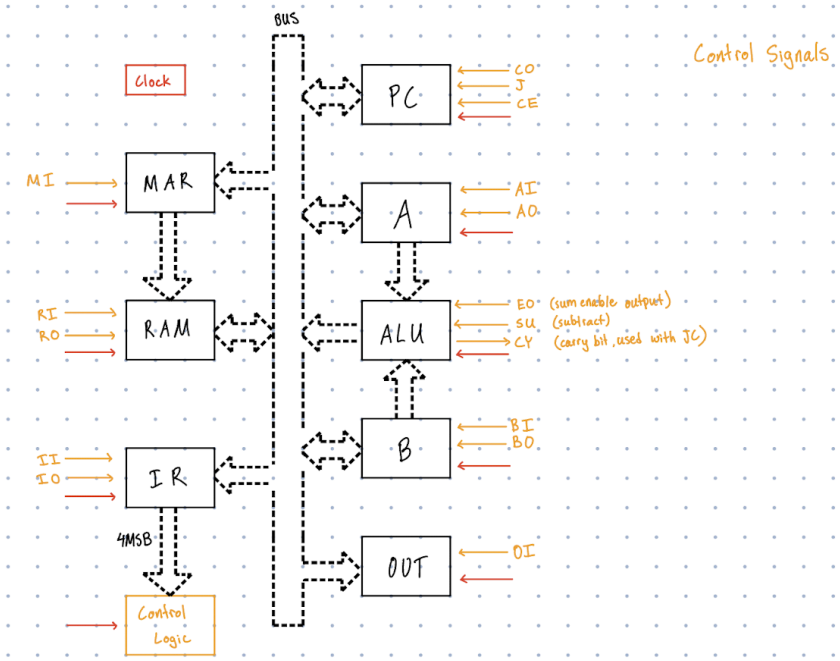
VLSI Midway Presentation
VLSI Final Presentation

3/21 - 3/28 Plan

- Unrelated to the project, but finish labs first!
- Continue research and finalize architecture (SAP-1 based, figure out exact RAM design, etc)
- Draw block diagram
- Decide which blocks to be made with which creation style (full custom, PCell, pushbutton/verilog)
    - Will very very likely use a combination of them, so figure out which one for each part in the block diagram
- This is just wrapping up step 1 and do 2a and 2c from the project overview list

3/21 - 3/28 Progress

- Drew block diagram



- Decided which cells would be which creation style

PCELL

- Clock
- Registers
- Program Counter
- ALU?

Verilog

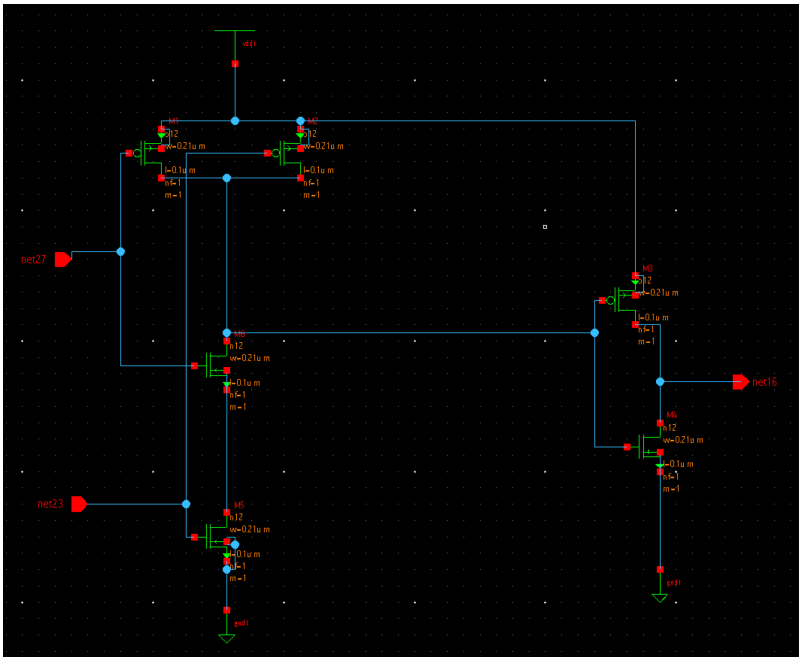
- RAM
- Controller

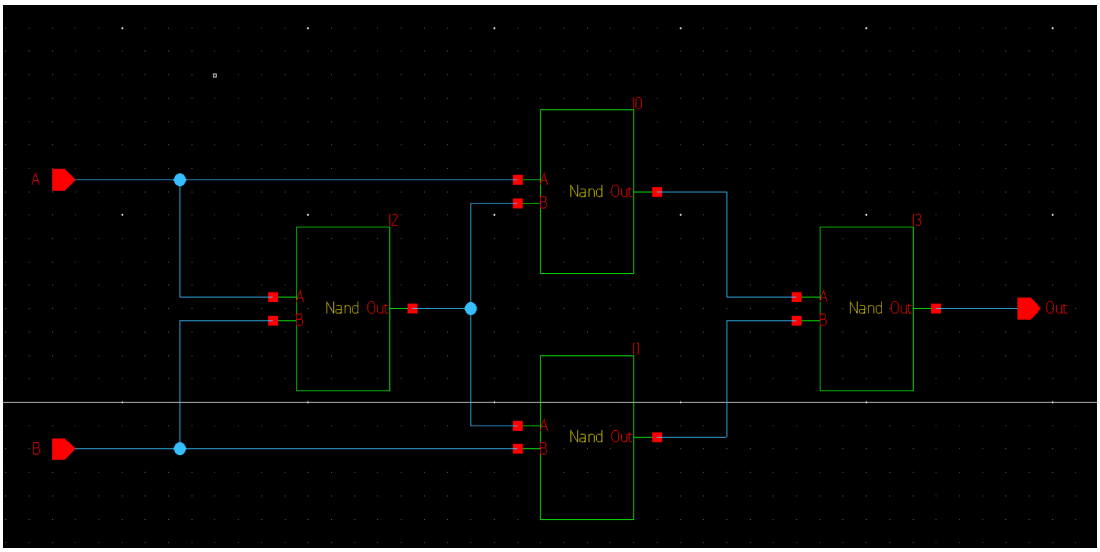
3/28 - 4/4 Progress

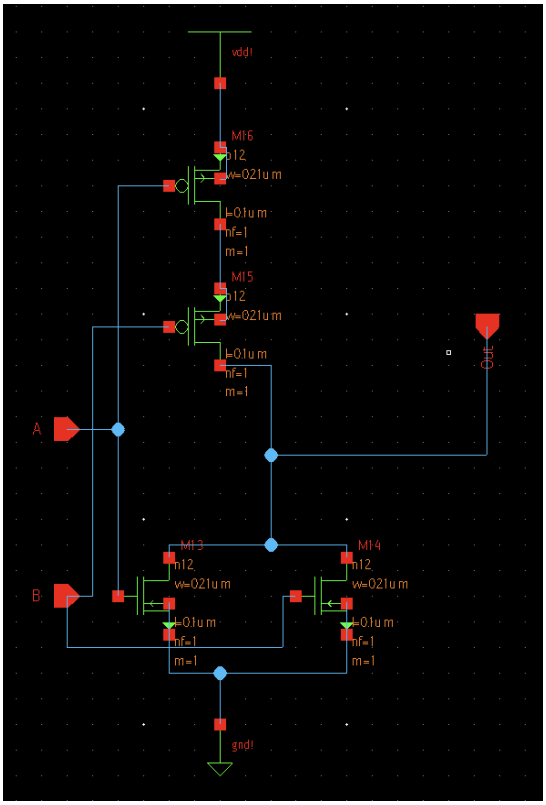
- Attempted (and failed) to make a Comparator
  - Struggled on this for ~3 hours
- Decided to leave PCell for a later day since couldn't make the clock
- Wrote SystemVerilog for RAM and ALU, as well as testbenches
  - https://drive.google.com/file/d/1n39oAYGuxq32STchSp5SnzR1GW8K8f53/view?usp=sharing

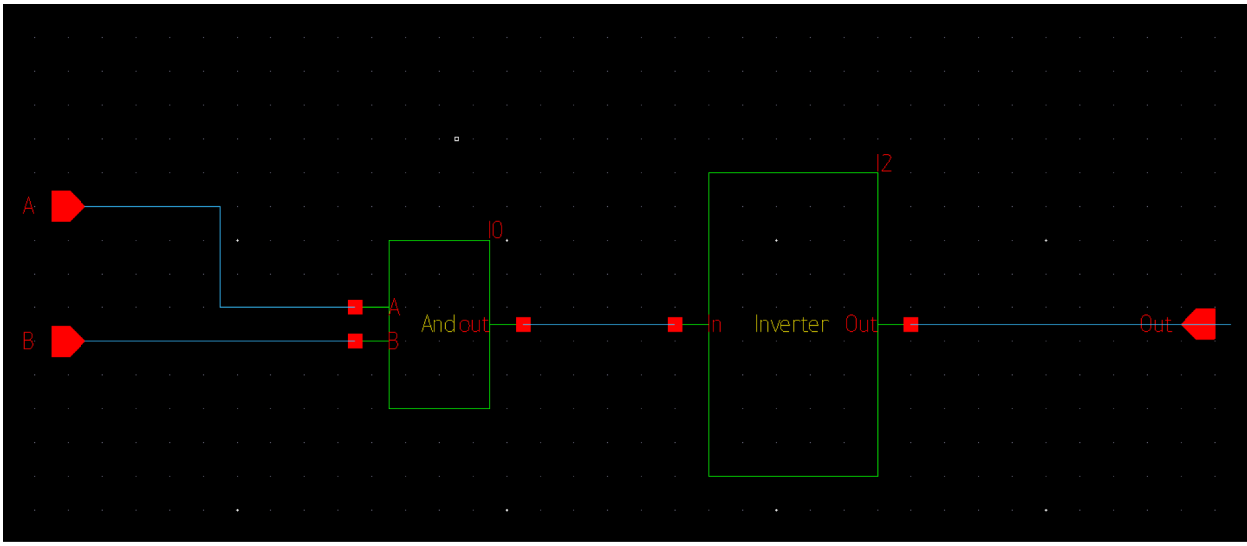
4/4-4/11 Progress

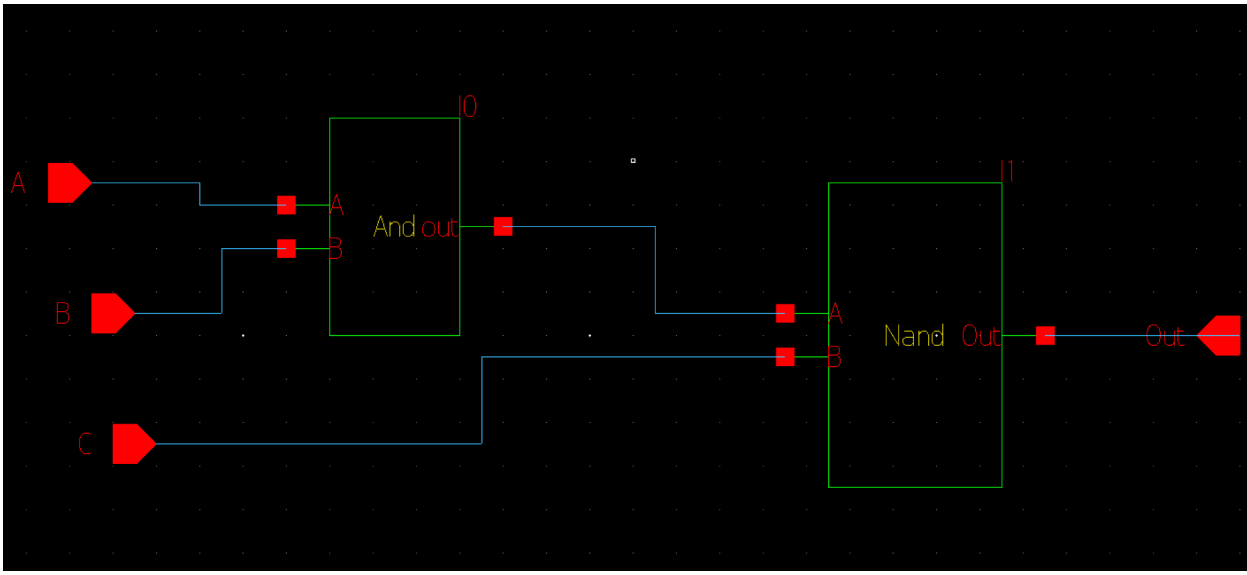
- Designed a bunch of PCell gates + more
  - And, Xor, Nor, Nand, 3InputNand (Pictured in order)



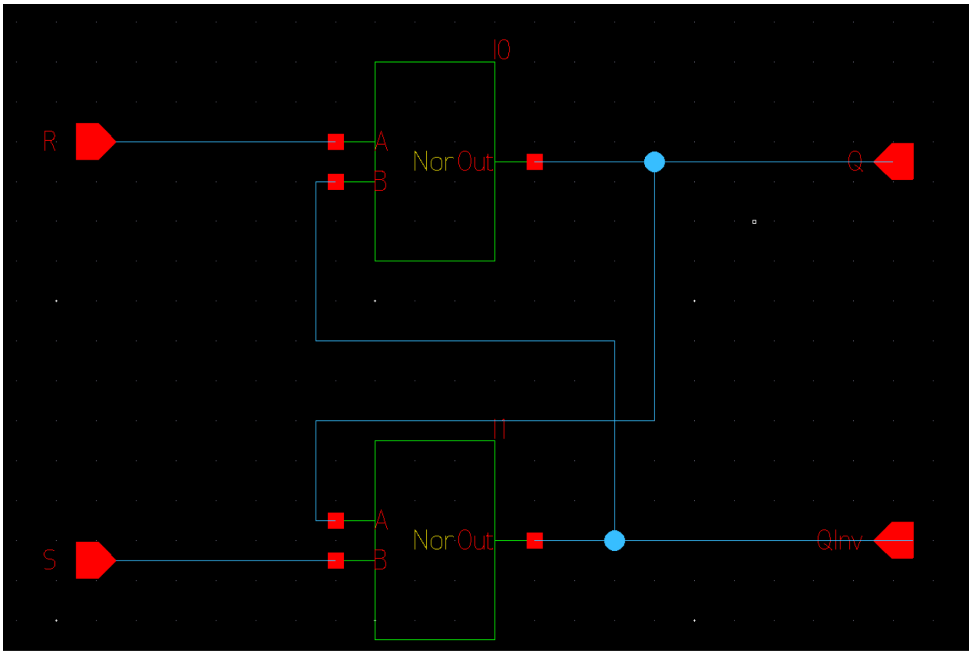

A
B
I0
I1
I2
I3
A
B
Nand
Out
Out


vdd!
MI6
pl2
w=021u m
l=0.1u m
nf=1
m=1
MI5
pl2
w=021u m
l=0.1u m
nf=1
m=1
Out
A
B
MI3
nl2
w=021u m
l=0.1u m
nf=1
m=1
MI4
nl2
w=021u m
l=0.1u m
nf=1
m=1
gnd!

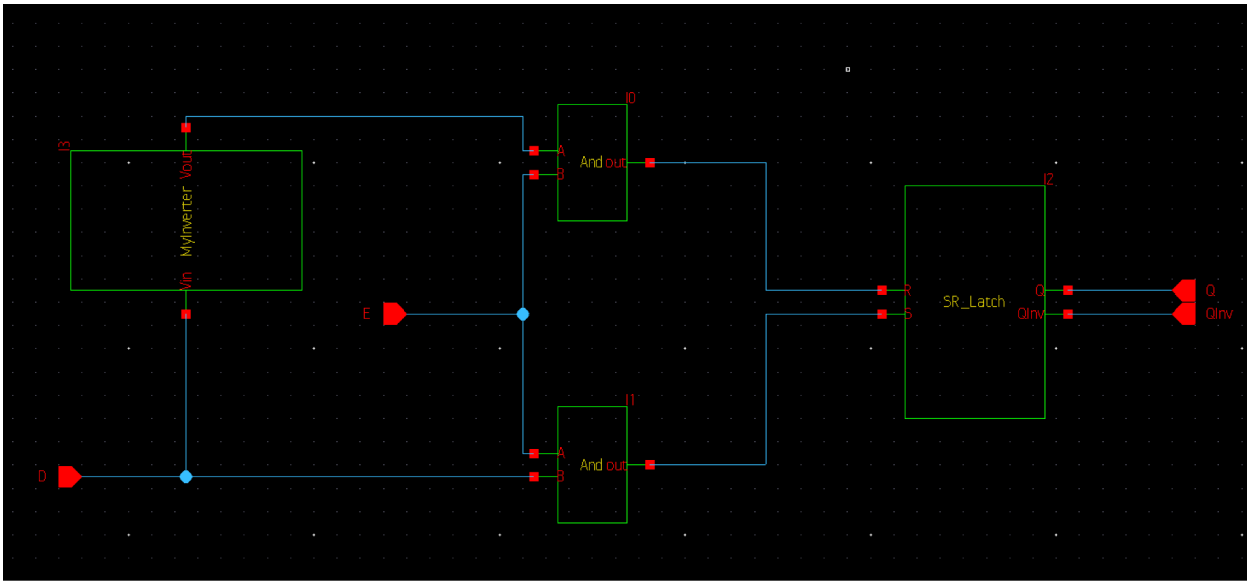

A
B
I0
A
B
And
out
I2
In
Inverter
Out
Out


I0
A
B
And
out
A
B
C
I1
Nand
Out
Out

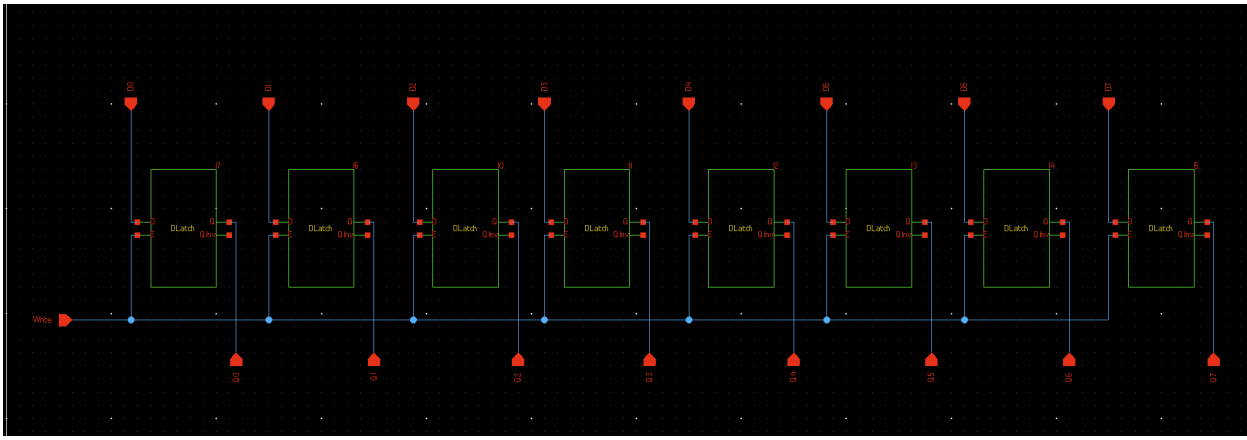
- SR_Latch

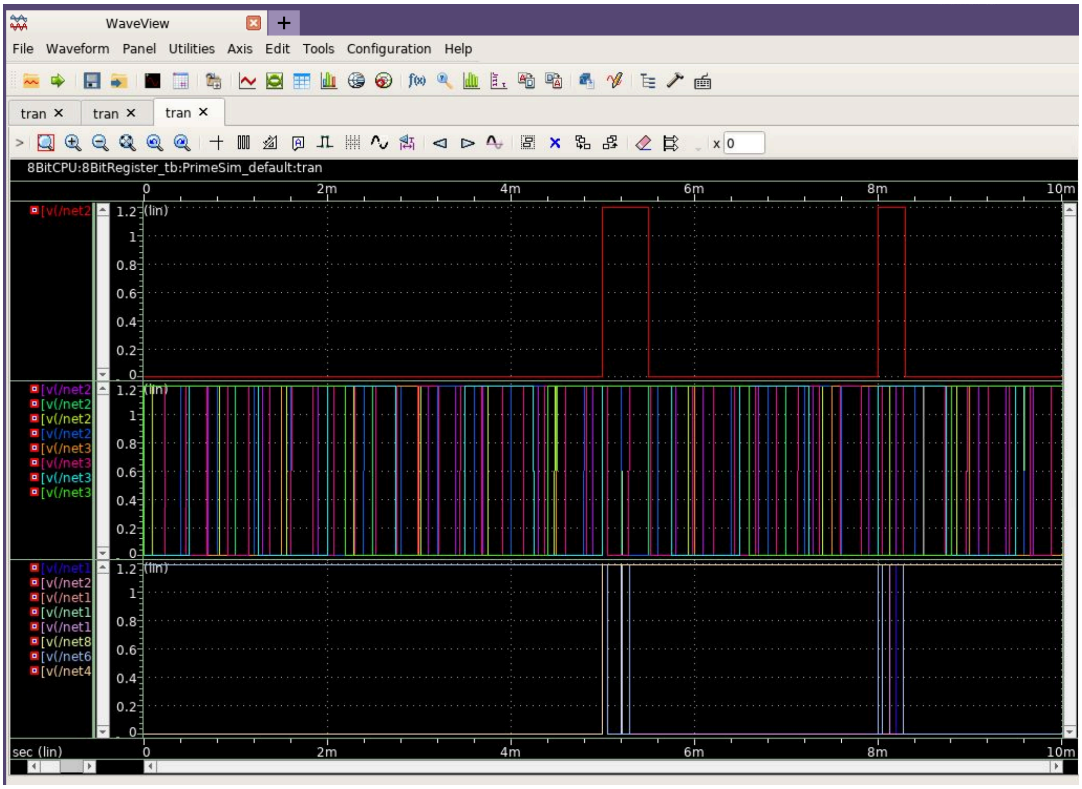


- DLatch

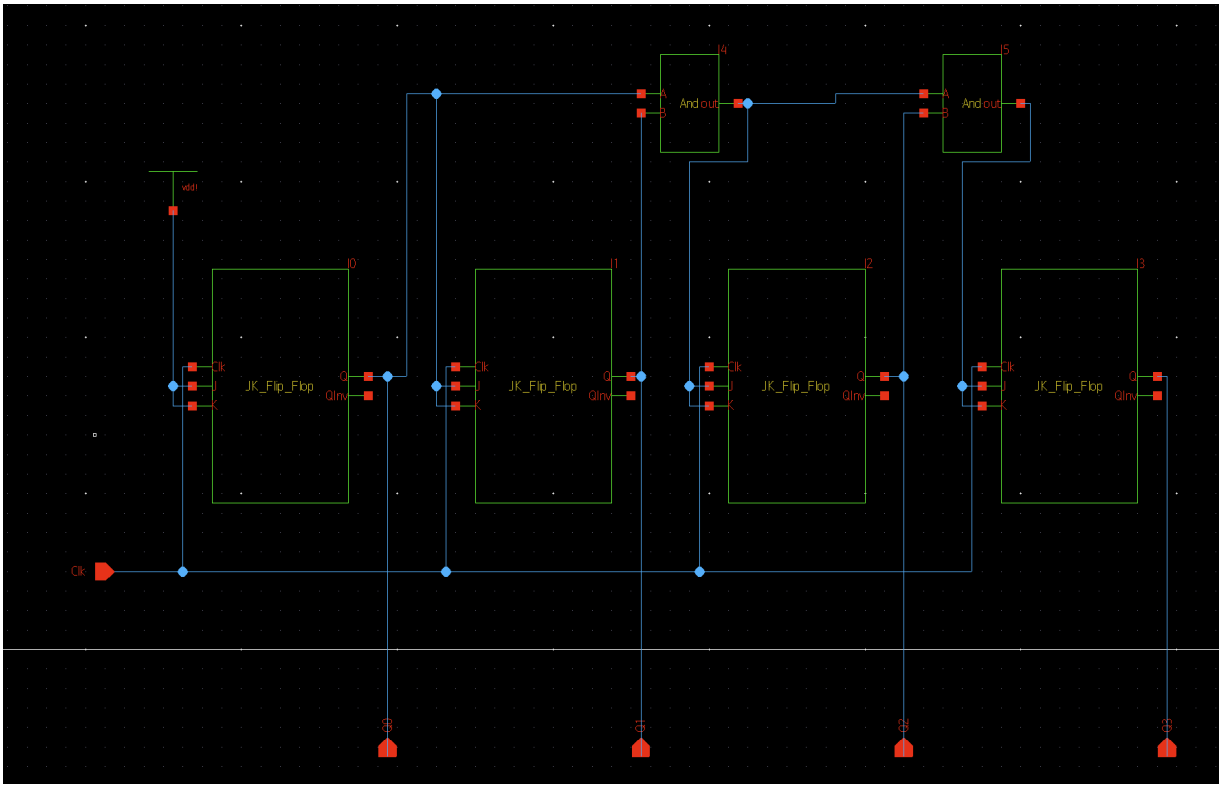


- Designed schematic for 8 Bit Register
  - Simulated, and works!

- 

- 

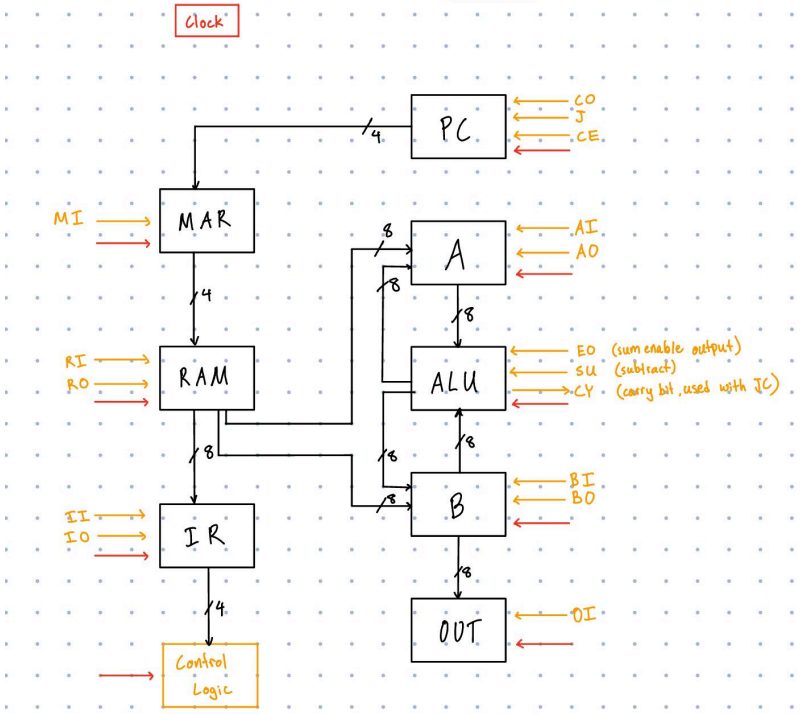
- Designed schematic for 4 Bit Counter
  - Simulation fails to run

- 

4/11-4/18 Progress

- Designed 5 more JK Flip Flops, since it was the JKFF that didn't simulate in the 4 Bit Counter
  - One simulates, but doesn't look right (the one I made from transistors simulates, the ones from gates/verilog don't)
  - All the others don't actually simulate
- Started writing SystemVerilog for a whole 8 Bit Computer Module
  - Made a good amt of PCell progress last week, but doesn't look like I am going to be able to finish
  - Started writing the Verilog as backup

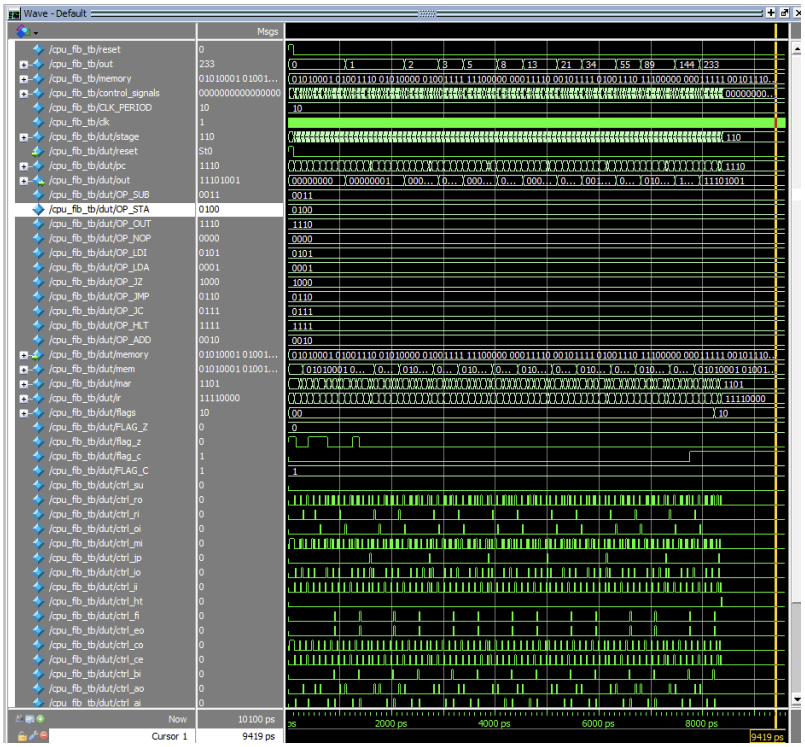
- New Block Diagram eliminating bus



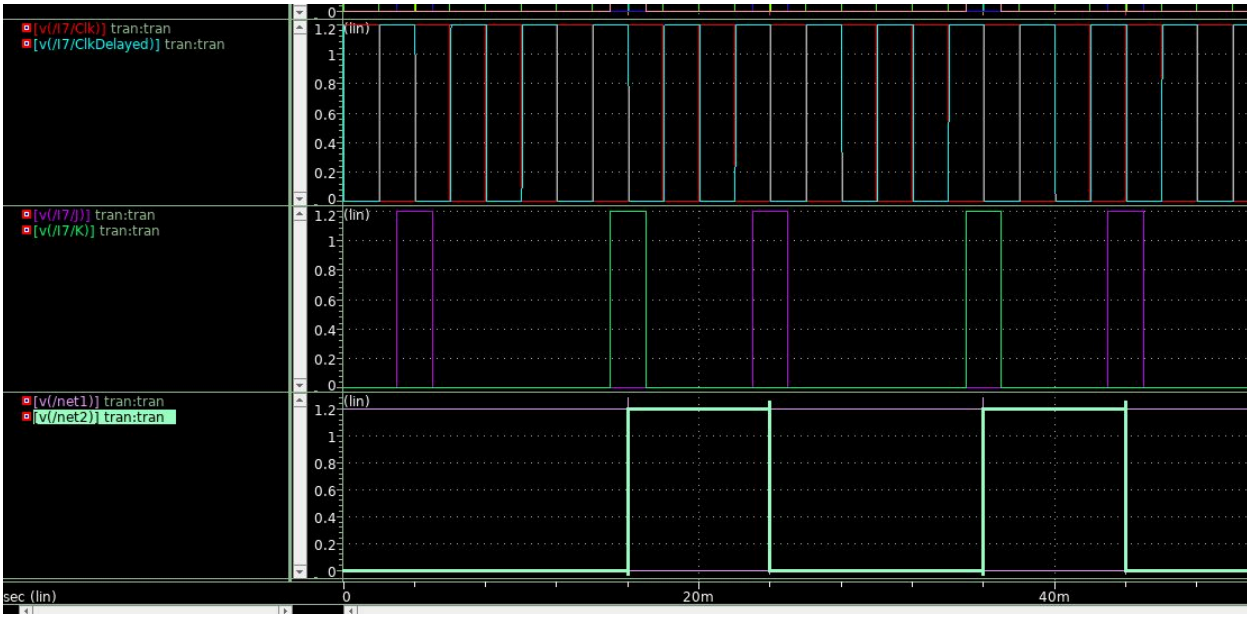
4/18-4/25 Progress

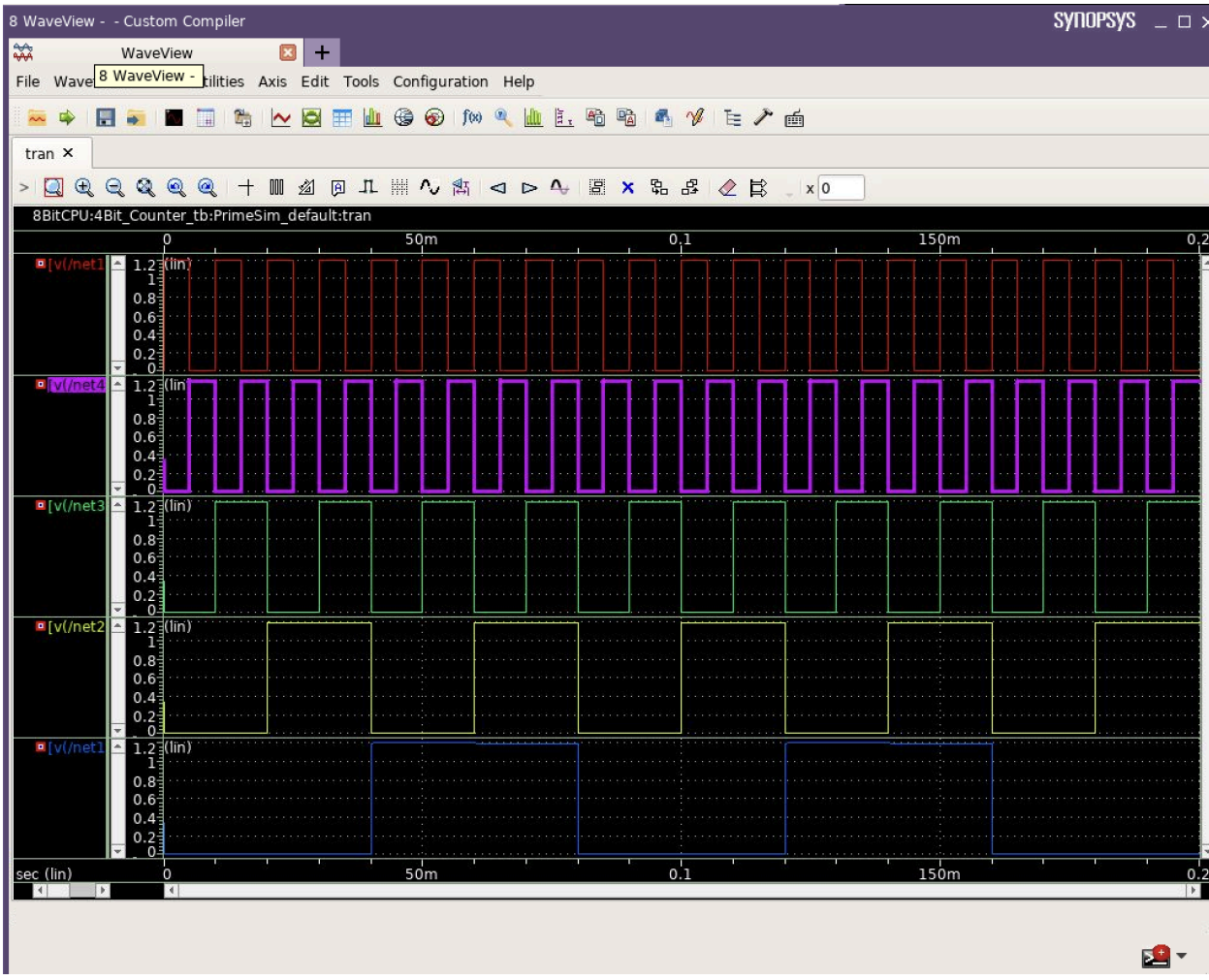
- Wrote Verilog for controller
- Wrote Verilog for the rest of the CPU - simulated - works!!
    - Ran Fibonacci program
    - https://drive.google.com/file/d/1SGNKKqwhTeqNn6zvzYRjhODoDTRbLxkP/view?usp=sharing

```
module cpu_fib_tb ();
    localparam CLK_PERIOD = 10;

    logic clk, reset;
    logic [7:0] memory [0:15];
    logic [0:15] control_signals;
    logic [7:0] out;

    cpu dut (clk, reset, memory, control_signals, out);

    initial begin
        clk = 0;
        forever #CLK_PERIOD clk = ~clk;
    end

    initial begin
        memory = {8'b01010001, 8'b01001110, 8'b01010000,
        8'b01001111, 8'b11100000, 8'b00011110,
        8'b00101111, 8'b01001110, 8'b11100000,
        8'b00011111, 8'b00101110, 8'b01111101,
        8'b01100011, 8'b11110000, 8'b0, 8'b0};
        reset = 1;
        #100;
        reset = 0;
        #10000;
        $stop;
    end
endmodule
```

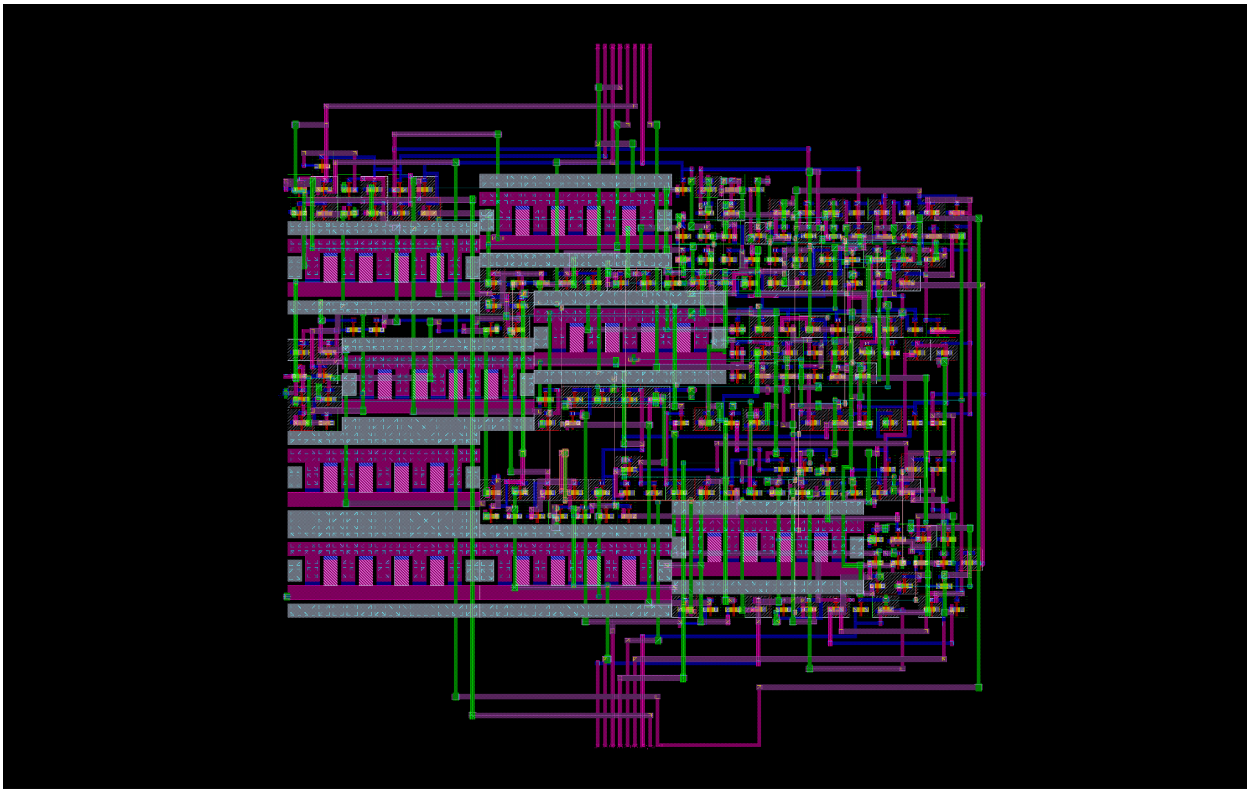
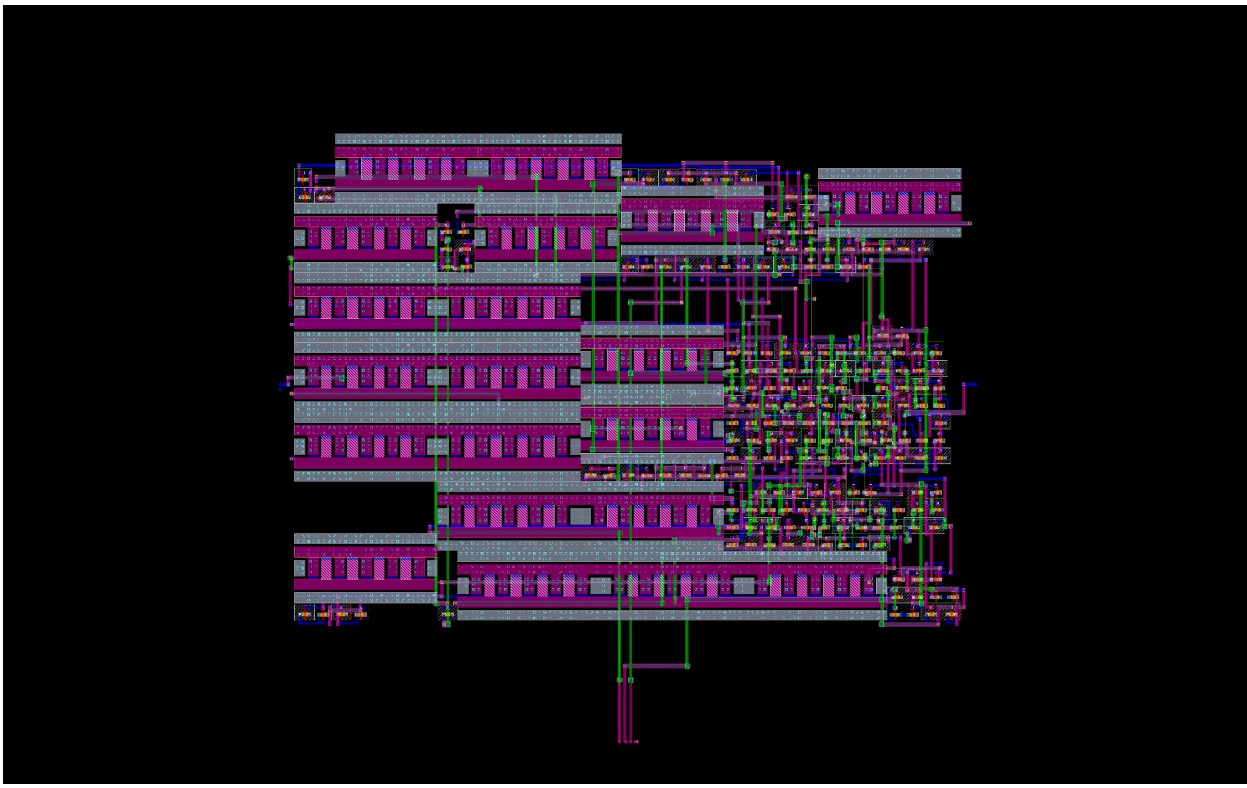


- Updated JK Flip Flop with non ideal inverter, works now!!

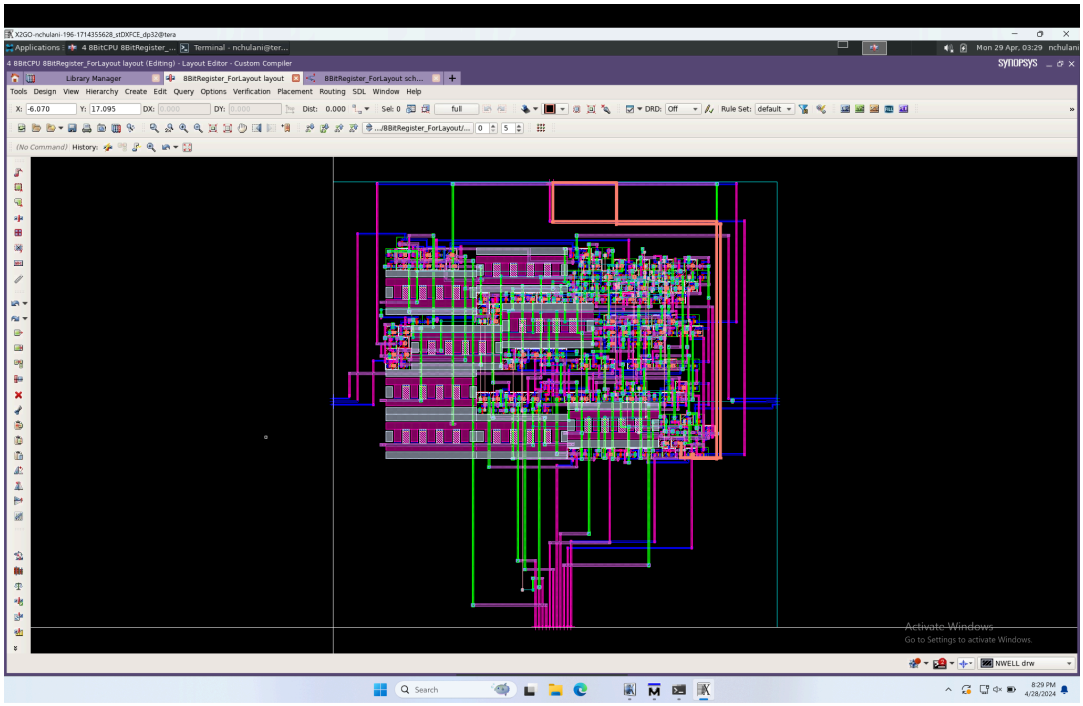
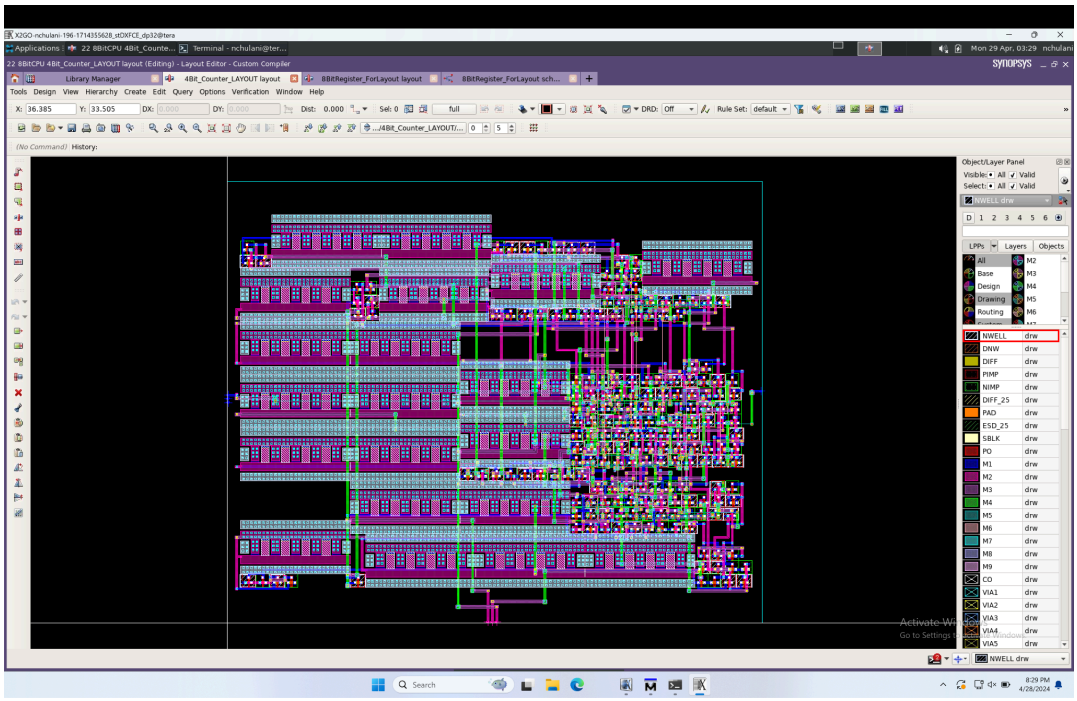
- 

- Used Updated JKFF in counter, simulated, works now!!
  - 

- Used push button flow to generate layouts + routing for PC and Register for fun

- Looks pretty cool :) … but probably not fully correct (tool to verify layout doesn't work, so can't run correctly, but, the schematics they are generated from are definitely correct!)
- 
- 

4/25-5/2 Progress

- Updated schematics for the layouts to include vdd and gnd pins, regenerated layouts for register and counter
- 
- 
- Took SystemVerilog cpu (the one that was simulated using ModelSim) through the design compiler - results here: https://drive.google.com/file/d/1gDdU3a-fL1EUIh7HeywYzaAShuyYkVD_/view?usp=sharing

Results Summary

I am incredibly happy with the progress I was able to make on this project, and with the amount I was able to learn (with lots and lots of help of course). I had started to think about whether or not this was a feasible project before Spring Break, and was a little nervous that I wouldn't be able to produce a significant amount of results or get anywhere near a finished product, since it certainly was a relatively large project. That being said, I was able to get very familiar with designing CMOS logic (which was the biggest goal), and I was even able to simulate the final CPU in Verilog. I got pretty much everything I wanted out of this project, since the whole goal was to completely remove any abstractions from the making of a computer, and by the end I was even able to produce a layout for parts of it (can't get much lower level than that!).

Locations of Project Materials

- All PCELL blocks (including a ton attempts that don't work) are stored at /home/nchulani/8BitCPU on the server
    - Final PCELL for register is 8BitRegister, with 8BitRegister_tb
        - 8BitRegister_ForLayout contains the final layout
    - Final PCELL for program counter is 4Bit_Counter, with 4Bit_Counter_tb
        - 4Bit_Counter_LAYOUT contains the final layout
    - Gates used were And, Nor, Nand_NEW, 3NandNEW, XOR, SR_Latch, DLatch, JK_Flip_Flop
        - Some have corresponding testbenches as well
- SystemVerilog cpu along with result of design compiler is at /home/nchulani/Synth8Bit
    - Original SV is CPU.sv, result is 8bitCPU.v
    - Both files are also linked
- Midway + Final presentations linked here