

Princess Sumaya University for Technology King Abdullah II School of Engineering Senior Design Projects

Design and simulations of a digital Low Drop-Out (LDO) with fast transient response

4	Advisor Name	Dr. Hani Ahmad Assi		
1	Co-Advisor Name			
2	Year / Semester	Fall 2016-2017		
3	Title of Senior Design Project	Design and simulations of a digital Low Drop-Out (LDO) with fast transient response		
4	Design to be Achieved	This project involves the design and simulations of digital PMOS LDO to achieve fast transient response to a sudden load change. This type of circuit is used in power management applications and circuits that are sensitive to supply variations.		
5	Engineering Standard	180nm CMOS standard Technology		
6	Design Requirements	The design shall achieve the following requirements:		
		1- Use180nm standard CMOS technology that conforms to Mixed		
		mode/RF specifications in the in following manufacturing		
		foundries:		
		a. United Microelectronics Corporation (UMC):		
		http://www.europractice-ic.com/technologies_UMC.php		
		b. Taiwanese Semiconductor Manufacturing Company		
		(TSMC):		
		http://www.europractice-ic.com/technologies_TSMC.php		
		2- The supply voltage shall be 3.3 V to conform to 180nm standard CMOS technology.		
		3- Regulated output at steady state shall be 2.5V.		
		4- Regulated output voltage shall not change more than +/- 200 mv		
		for a transient load from 0 to 100mA in 50ns.		
		5- The LDO shall handle loads up to 100mA.		
		6- Power Supply Rejection Ratio (PSRR) shall be more than 50 dB.		
		7- Quiescent current shall be below1mA.		
		8- Output cap shall be above 4.7uF.		
		9- For simulations, the latest UC Berkeley BSIM models for NMOS		
		and PMOS devices shall be used:		
		http://ptm.asu.edu/modelcard/180nm_bulk.txt		
		10- LT spice software is used to simulate the LDO.		



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7	Realistic Constrains	Economic	 Area of the whole module including power stage (PMOS) and control (Op-Amp, buffer and biasing) shall not exceed 0.5mm² given that the manufacturing cost is approximately \$1350/mm². 		
		Environmental	- LDO should be properly operating at the commercial temperature range standard which is 0-70C.		
		Manufacturability	LDO integrated circuit, if manufactured, shall achieve		
		and Sustainability	99% yield (3 sigma in a Gaussian distribution)		
		Other			
	Deliverables	Documentation	Yes		
8		Portfolio			
		Video			
		Other	Schematics and HSPICE Simulations		
9	Background of Students	Students should have passed electronics 2.			
10	Number of Students	3			

Advisor Signature

Co-Advisor Signature

Department Head Signature