PMOS Process Development Mid-Semester Documentation

By: Shagun Maheshwari

Motivation:

At present, the Hacker Fab process reliably supports phosphorus doping to create n-channels for NMOS devices. However, the absence of a method to form n-wells or p-channels prevents the fabrication of CMOS, which relies on both NMOS and PMOS.

Developing an effective process for n-wells and p-channels involves multiple hurdles. Chief among them is achieving the correct carrier density, controlling the n-well junction depth for proper isolation, and balancing the thermal budget to avoid excessive diffusion. A cross-sectional comparison of NMOS and PMOS highlights how interdependent these structures can be.

Precisely creating the n-well is particularly challenging since it can inadvertently lower the doping levels of the n-channel or enlarge the channel region. Meanwhile, doping the p-channel can also shift the doping profiles of both the n-well and the NMOS channels because the heat required to diffuse boron also drives phosphorus deeper.

Moreover, the total diffusion window is limited to around three hours. Under constant-source diffusion, either the phosphorus concentration or the diffusion period must be restricted to prevent extending the drive-in time needed for a uniform dopant profile. Carefully calibrating these steps is crucial to ensure the desired electrical characteristics, maintain device performance, and minimize defects.

.

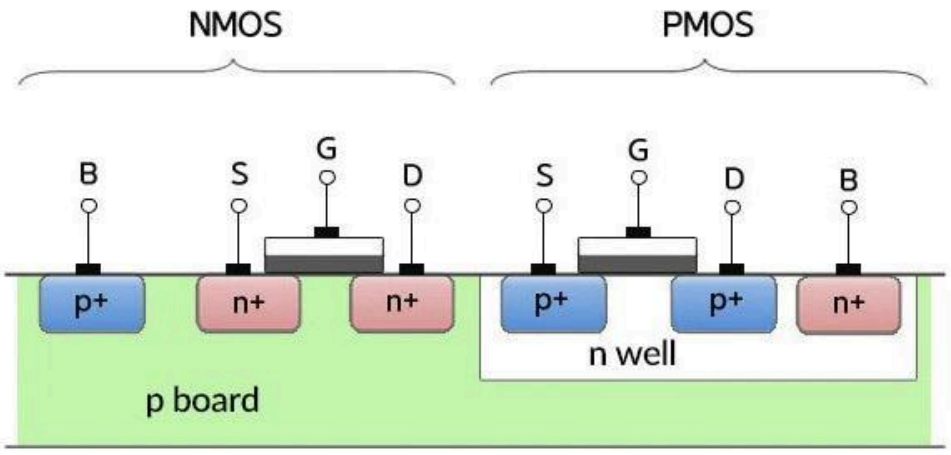


Figure 1: CMOS diagram [1]

The primary motivation for this semester's experiments is to refine the fabrication process of dopant regions (junction depth, dopant concentration) to enable the development of PMOS transistors in order to build CMOS technology. The first step to tackling this is to improve the understanding and characterization of dopant profiles in n-well and p-type regions. Once this is achieved it will enable the hacker fab to refine their diffusion models with correct concentration parameters provided by experimental results to be used to develop a robust CMOS fabrication process.

1. Background

1.1 Capacitance Voltage Measurements:

In order to determine the dopant concentration, dopant profile, and junction depth of the n-well and p-channel regions, we utilize the MOS Capacitor structure and perform capacitance-voltage (CV) measurements. The goal is to translate the CV measurements into dopant profiles (dopant concentration vs depth), and then compare the experimental results to simulation results from the diffusion model to refine it.

Essentially, the MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and the metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

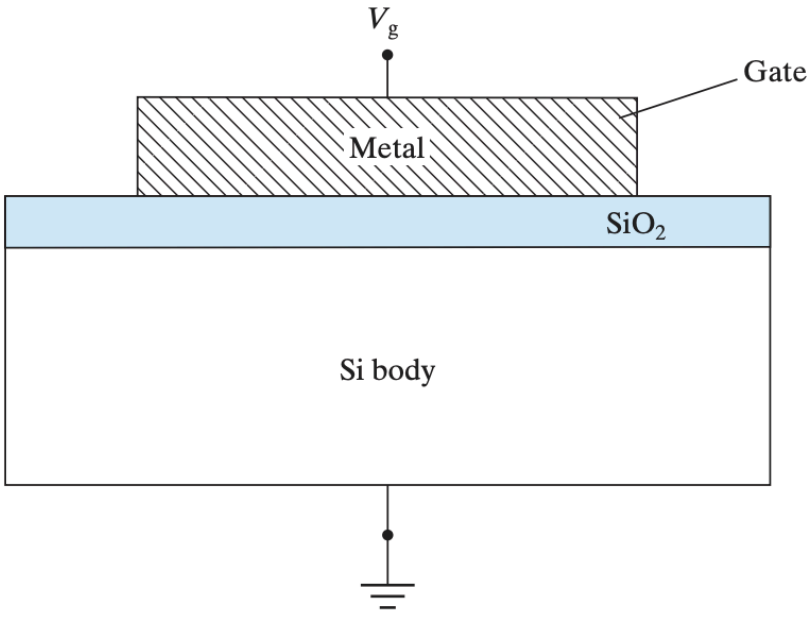


Figure 2: MOSCAP diagram [2]

The most important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. The purpose of the DC voltage bias is to allow sampling of the material at different

depths in the device. The AC voltage bias provides the small-signal bias so the capacitance measurement can be performed at a given depth in the device. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

1.2 Operating regions of the MOSCAP (p-type):

Accumulation (Negative Vg):

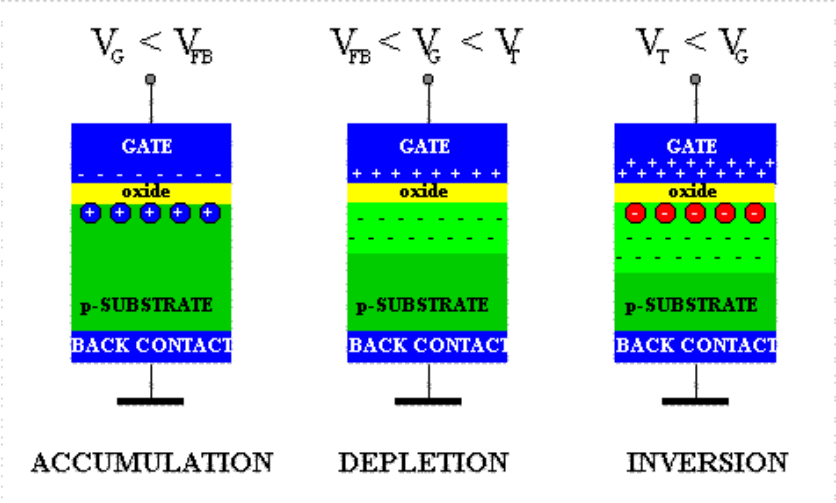
- When the gate is negatively biased, holes accumulate at the surface/valence band
- Little to no depletion forms so Cmos = Cox (oxide capacitance)

Depletion (Moderately positive Vg):

- As the gate becomes positive, holes are repelled, forming a depletion region
- Region acts as a dielectric as it can no longer contain or conduct charge
- Capacitance is Cox and Cd (depletion capacitance) in series, resulting in capacitance decrease

Inversion (Strongly positive Vg):

- Minority carriers (electrons) appear at the surface, forming an n-type inversion layer.
- High-Frequency: Minority carriers cannot respond quickly to the AC signal, measured capacitance in inversion stays below Cox



- Low-Frequency: Minority carriers can follow the slower AC signal, inversion-layer capacitance becomes approaches Cox

Figure 3: Accumulation, Depletion, Inversion regions of p-type MOSCAP [3]

Figure 4 below illustrates a high frequency and low frequency C-V curve for a p-type MOSCAP. As a DC sweep voltage is applied to the gate, it causes the device to pass through accumulation, depletion, and inversion regions.

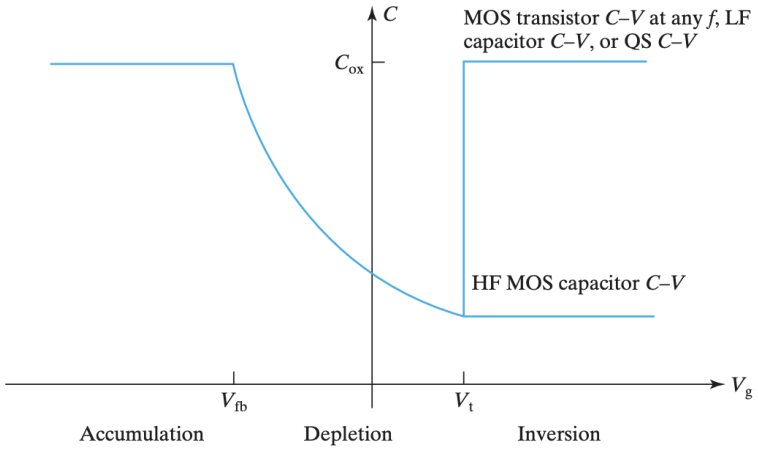


Figure 4: CV plot at high and low frequencies of a p-type MOSCAP [4]

1.3 Extracting Parameters from C-V Measurements:

Accurate C–V (capacitance–voltage) measurements of a MOS capacitor yield three critical parameters related to the substrate doping:

1. Overall doping concentration
2. Doping profile versus depth
3. Junction (or depletion) depth

Each of these can be determined by analyzing how the MOSCAP capacitance changes under different bias conditions.

1.3.1 Doping Concentration

A straightforward way to determine the average substrate doping Nsub is to measure the inverse-square capacitance ($1/C^2$) as a function of the gate voltage V_G in the depletion region. Plotting $1/C^2$ vs. V_G typically yields a linear region; its slope is related to the doping concentration via:

$$N_{SUB} = \frac{2}{q\varepsilon_S A^2 \left(\frac{\Delta 1/C^2}{\Delta V_G} \right)}$$

N_{SUB} = substrate doping concentration
q = electron charge (1.60219×10^{-19}C)
A = gate area (cm^2)
ε_S = permittivity of the substrate material (F/cm)
V_G = gate voltage (V)
C = measured capacitance (F)

This formula assumes operation in depletion (not strong inversion) and a clear linear region from which to extract the slope.

$$N(W) = \frac{2}{q \cdot \epsilon_{si} \cdot \epsilon_0 \cdot A^2} \left[\frac{d}{dv} \left(\frac{1}{C^2} \right) \right]^{-1}$$

$$W = A \cdot \epsilon_{si} \cdot \epsilon_0 \left(\frac{1}{C} - \frac{1}{Cox} \right)$$

1.3.2 Doping Profile

Beyond a single “average” doping, one can extract how doping varies with depth into the substrate (the doping profile). Changing the DC gate bias modifies the depletion region width Wdep. For each incremental voltage step, a different capacitance is measured, corresponding to a different depth.

By repeating the measurement at various bias conditions (and hence depletion widths), we can map out N(Wdep) versus Wdep.

1.3.3 Junction Depth

Under strong inversion and high-frequency measurements, the depletion region width saturates at a maximum Wdep,maxW. Any further increase in gate voltage primarily expands the inversion layer, not the depletion region. The minimum depletion-region capacitance Cdep,min then corresponds to this maximum depletion width.

$$W_{\text{dep,max}} = \frac{\varepsilon_s A}{C_{\text{dep,min}}}$$

In a p–n structure, this Wdep,max can be interpreted as the physical junction depth, which is the depletion boundary location when the surface is strongly inverted.

2. Planned Experiments:

1. P-type substrate MOSCAP (Experiment 1)

2. N-well in P-doped Si MOSCAP (Experiment 2)
3. P-doped channels in the N-well MOSCAP (Experiment 3)

3. Experiment 1: P-type substrate MOSCAP

3.1 Goal

Fabricate a p-type MOSCAP and conduct C-V measurements to extract the doping profile. This is a baseline experiment to test our fabrication process, C-V testing effectiveness, and analysis steps.

3.2 P-type MOSCAP design

In a typical MOSCAP, the measurement setup applies the gate voltage on a metal electrode above the oxide, with the chip's backside serving as the reference. This works for a standard p-type MOSCAP, but it causes problems when measuring an N-well or p-channel device. Specifically, if you measure from the top metal to the chip's backside for an N-well, you end up capturing the capacitance of the underlying p-type substrate rather than the N-well itself.

To solve this, we modified the design to include two metal (aluminum) contacts on the surface: one on the oxide layer (the gate) and another directly contacting the substrate. As shown in the figure below, this ensures that the measurement truly corresponds to the N-well or p-channel region we want to characterize.

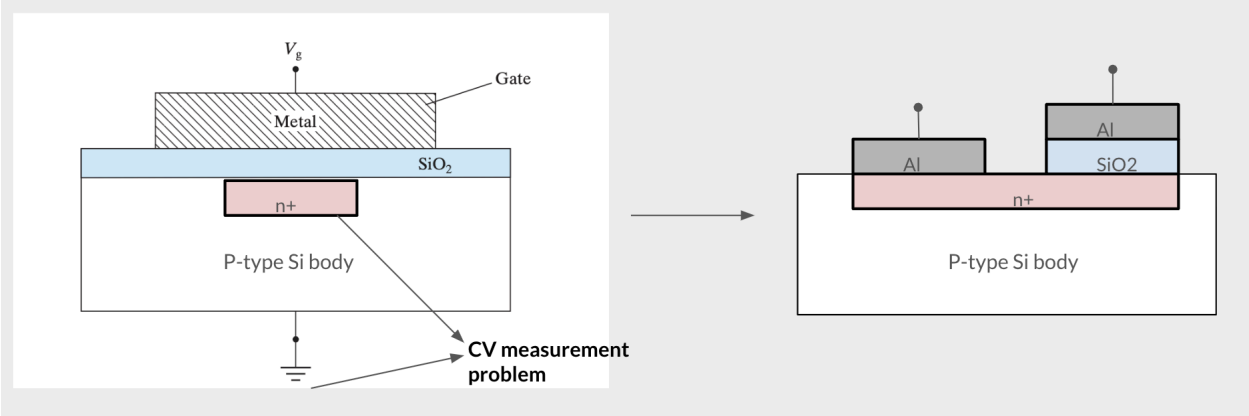


Figure 5: Schematic of N-well MOSCAP

As a result the patterns we utilize to fabricate a p-type MOSCAP is showcased below in Figure 6. The larger grey box is used to represent the aluminum contact and the smaller 3 rectangular boxes used to create the MOS.

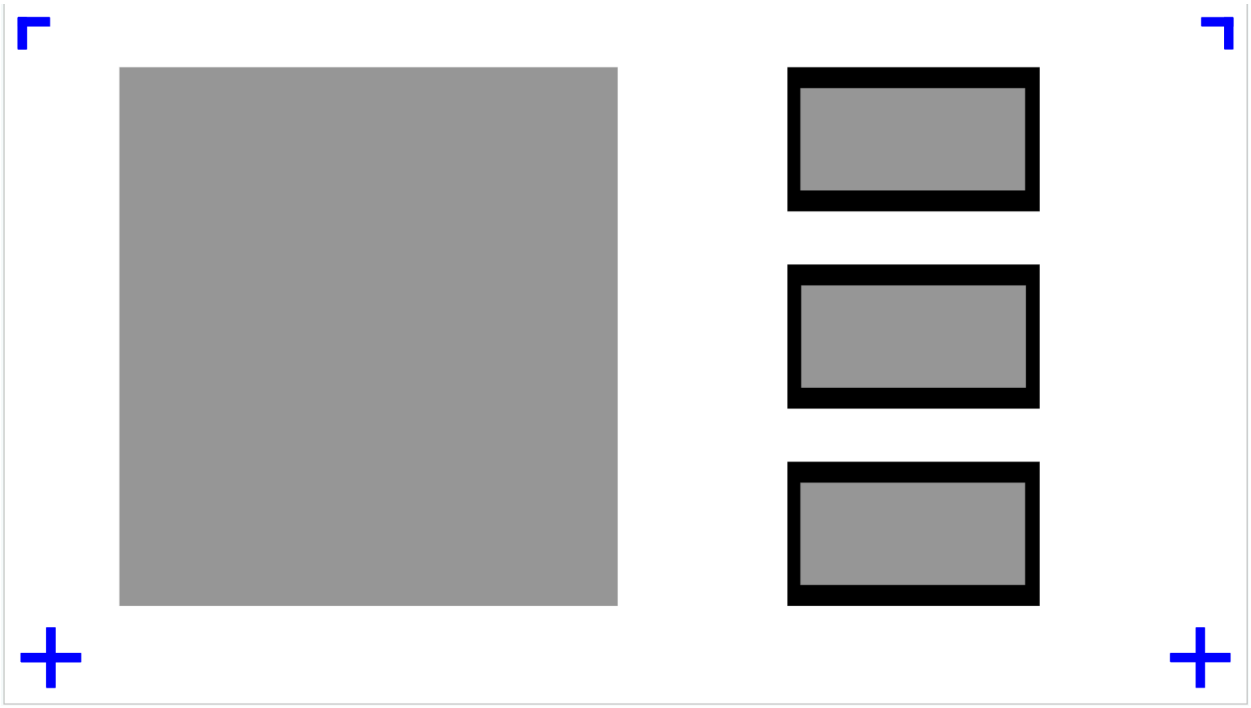
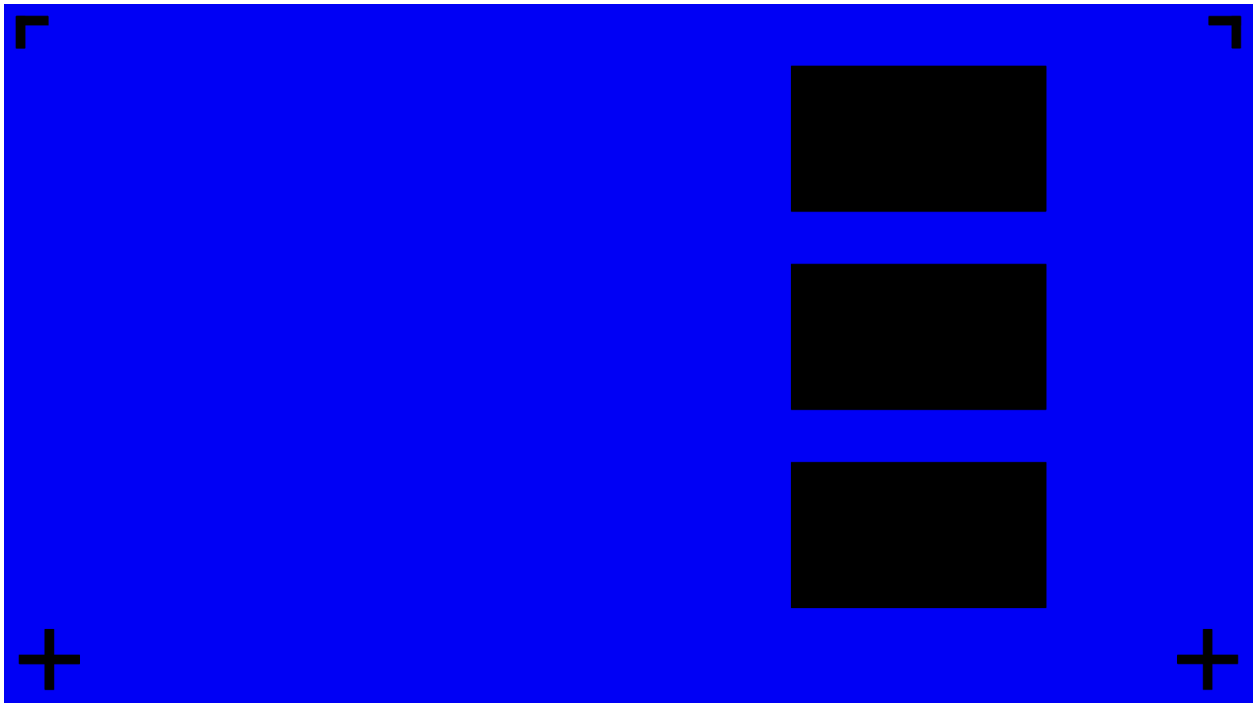
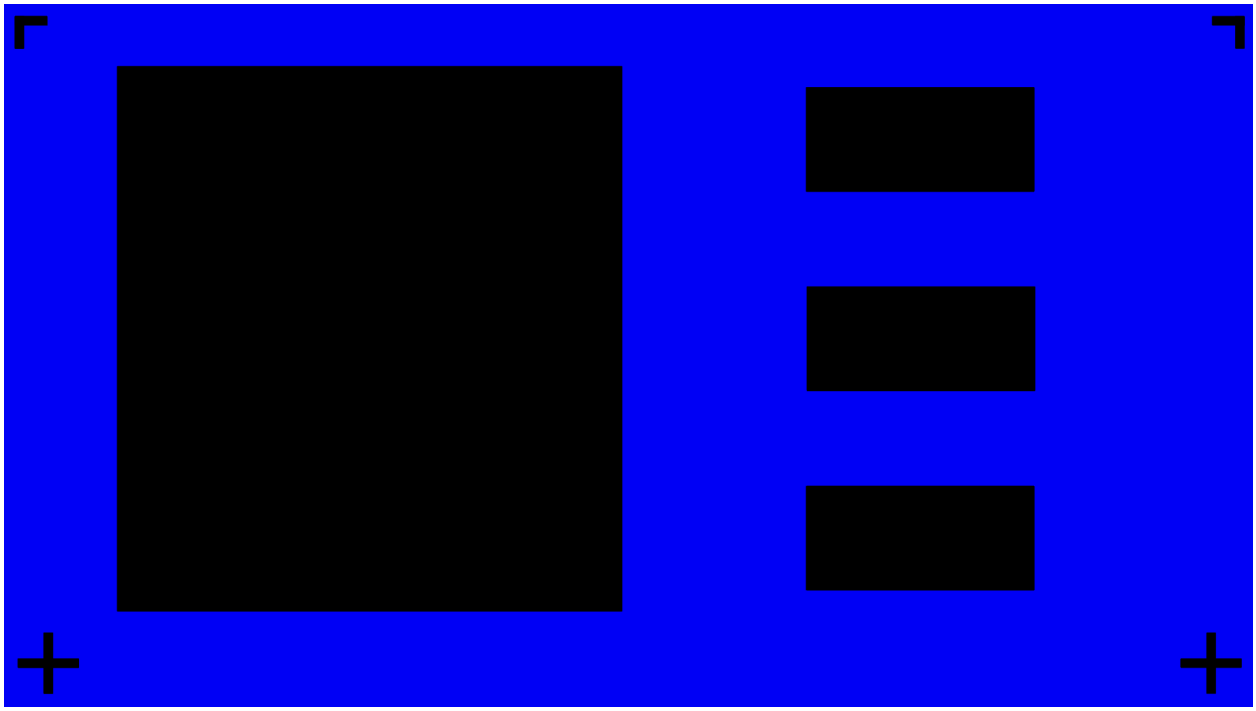


Figure 6: P-type MOSCAP Pattern[6]

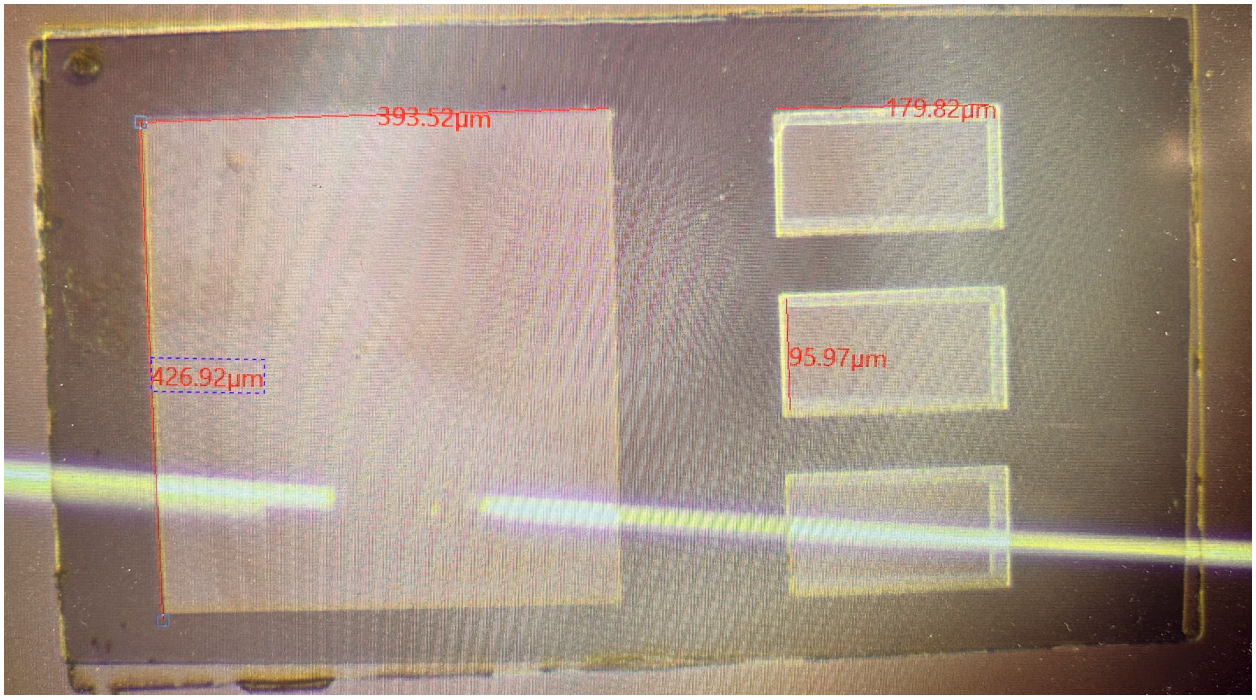
First Pattern to create the 3 MOS rectangles:



Second Pattern to create the aluminum contact for probing:



Dimensions of the fabricated pattern:



Link to all the patterns for P-type MOSCAP:

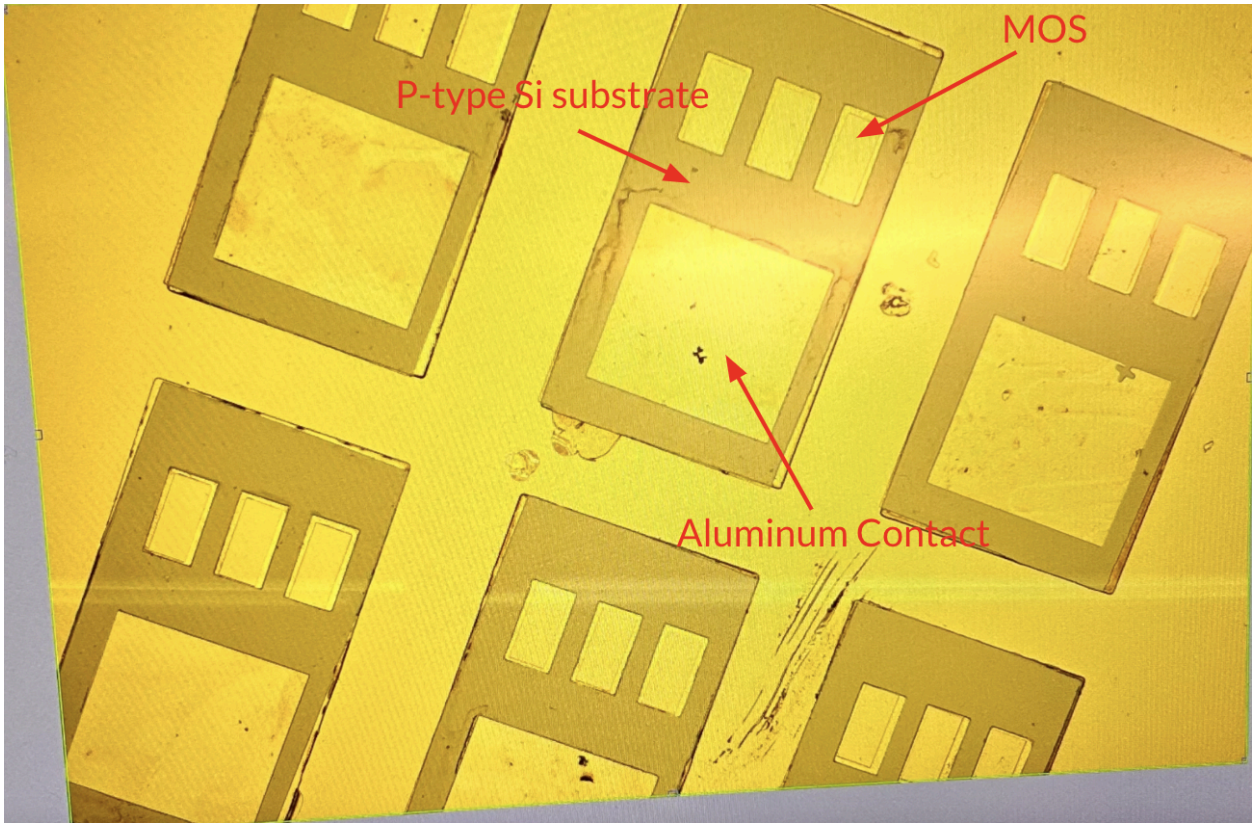
Maheshwari_Shagun_CV testing MOScap Pattern

3.3 Fabrication

Materials

- Dopant: Filmtronics P504 SOG (Phosphorus Doped SiO2)
- Al Thermal Deposition Source: Pure Al wire
- Substrate: University Wafer <100> single crystal p type silicon (5-10 ohm-cm)
- Oxide Etchant: Buffered HF oxide etchant
- Aluminum Etchant: Aluminum (Nitric, Acetic, Phosphoric Acids)
- FabuBlox Process: https://www.fabublox.com/process-editor/e3f683d1-9579-4761-847e-099c88ebb8c9

Completed fabrication of the P-type MOSCAP:



3.4 C-V Testing setup

C-V testing parameters:

- Sweep from -10 to 10V
- Frequency: 1MHz

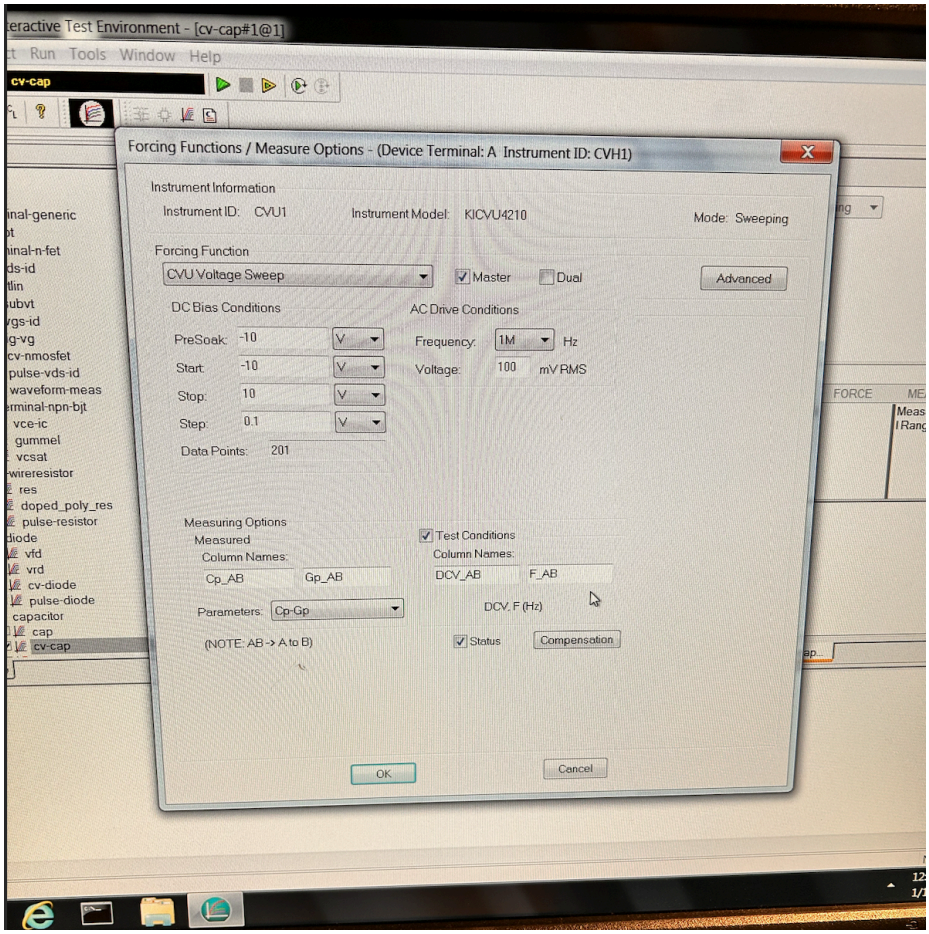
Tools:

- Probe station setup
    - Probe station - Karl Suss PM5
    - 2 probes, manipulators, and coaxial cables
- Microscope setup
    - Camera - AmScope MU1000-HS and AmScope viewing software
    - Light – MI-150 Fiber Optic Illuminator
- Keithley semiconductor analyzer system
    - Keithley 4200-SCS Semiconductor Parameter Analyzer
    - Keithley 2636a Sourcemeter
    - Keyboard and mouse

Procedure Links:

- https://docs.hackerfab.org/home/standard-operating-procedures/probe-station-sop
- https://docs.hackerfab.org/home/fab-toolkit/metrology-characterization/cv-measurements

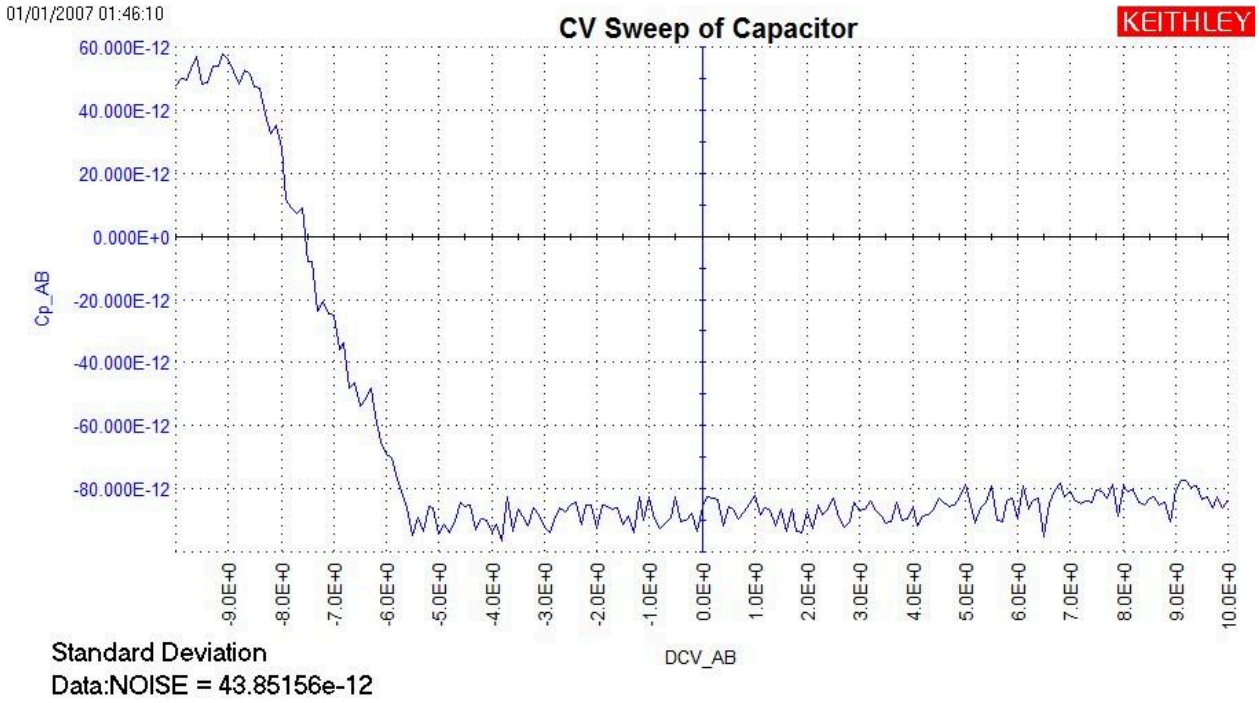
C-V testing parameters in cv-cap:



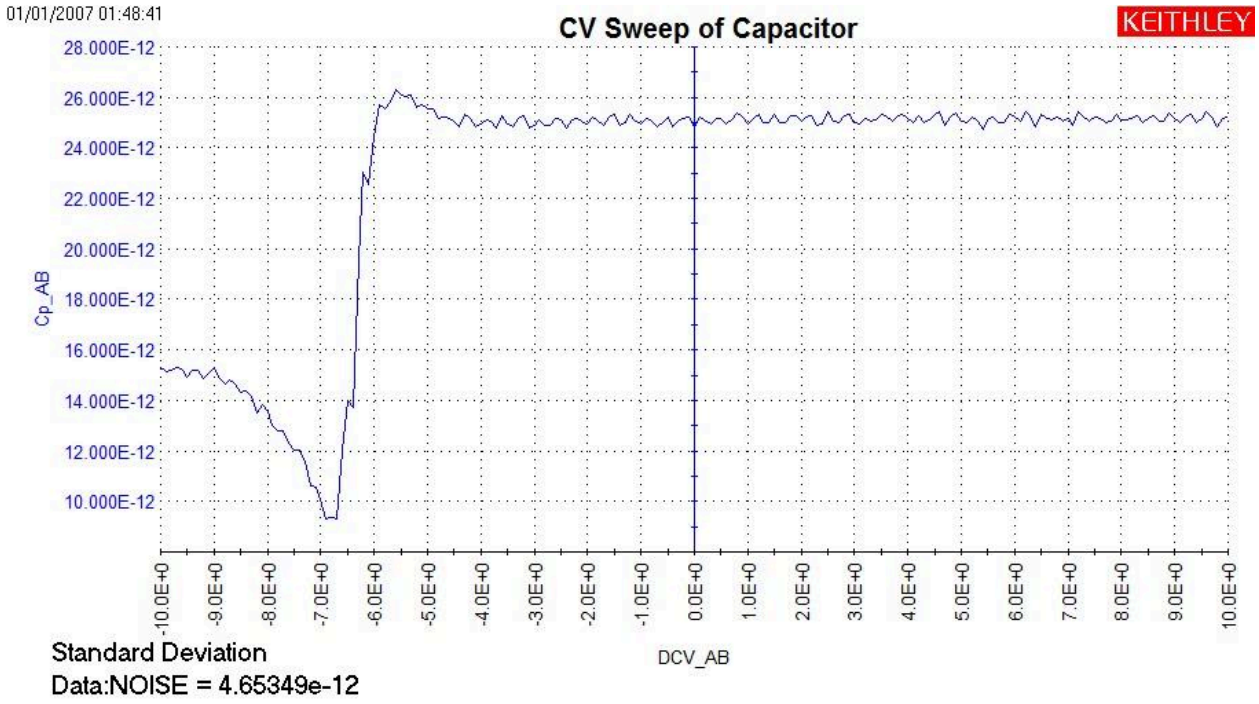
3.5 Results

Below are the results for high frequency and low frequency measurements across 3 copies of the same pattern.

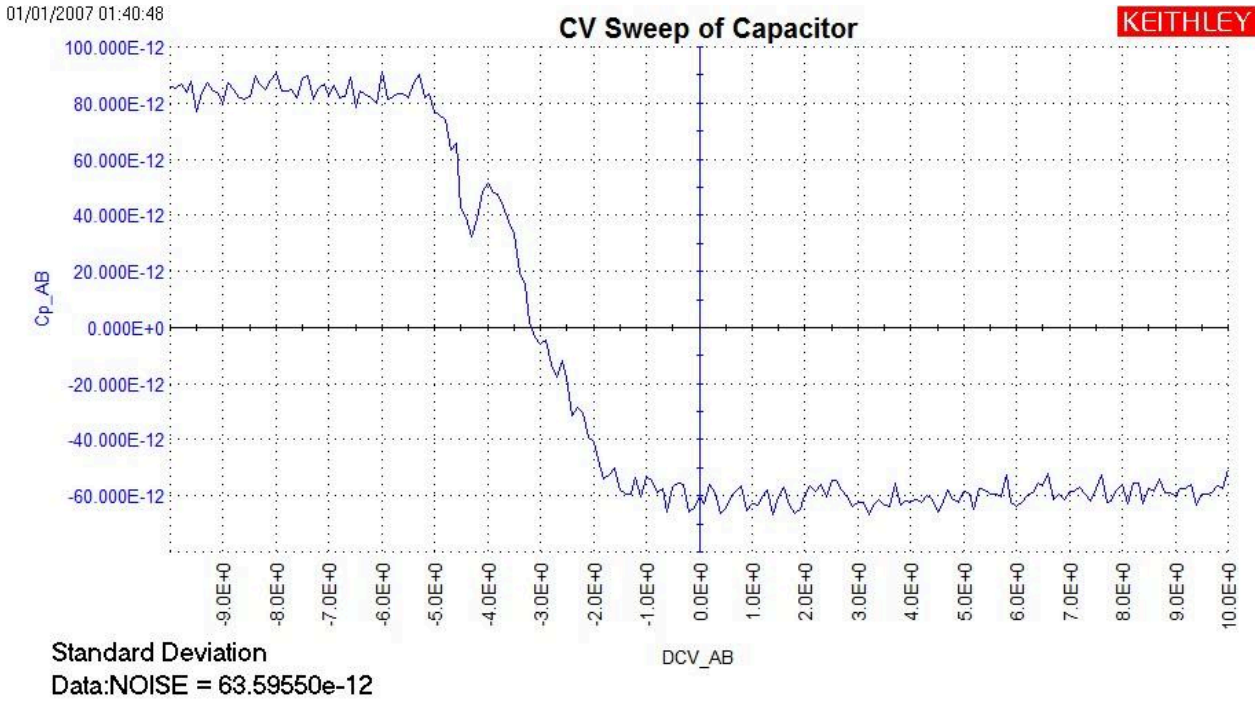
MOSCAP 1 High Frequency (1Mhz):



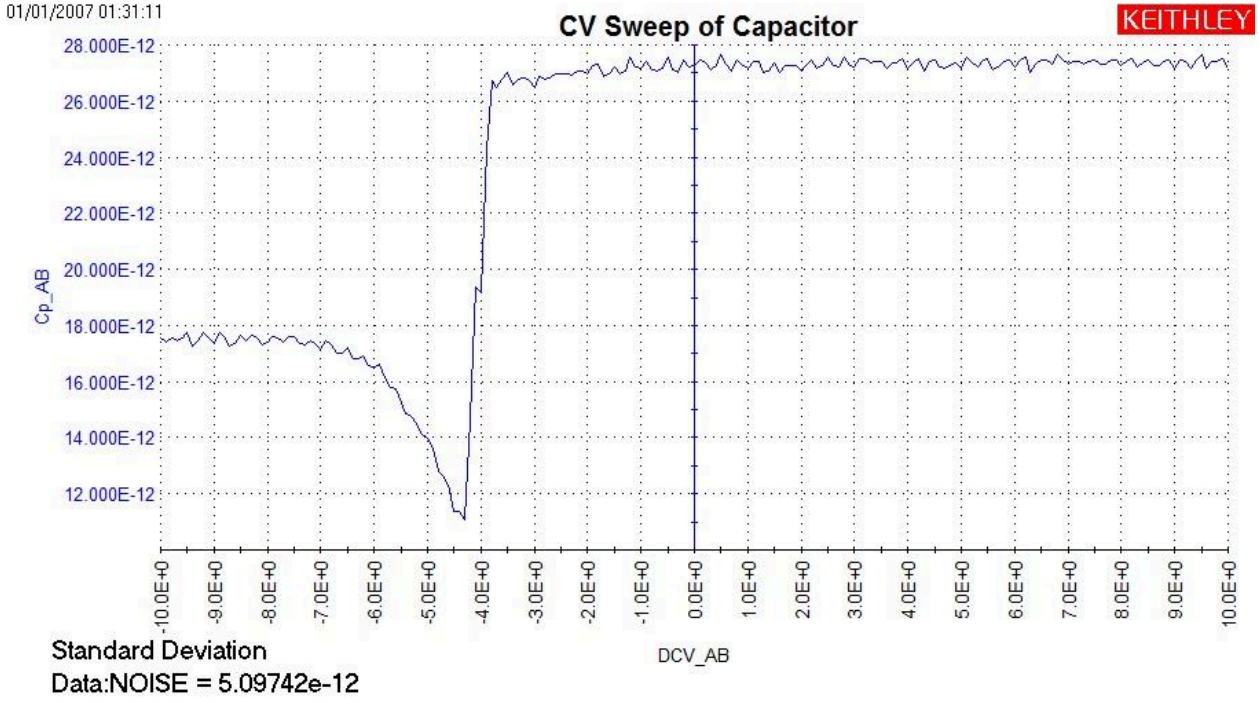
MOSCAP 1 Low Frequency:



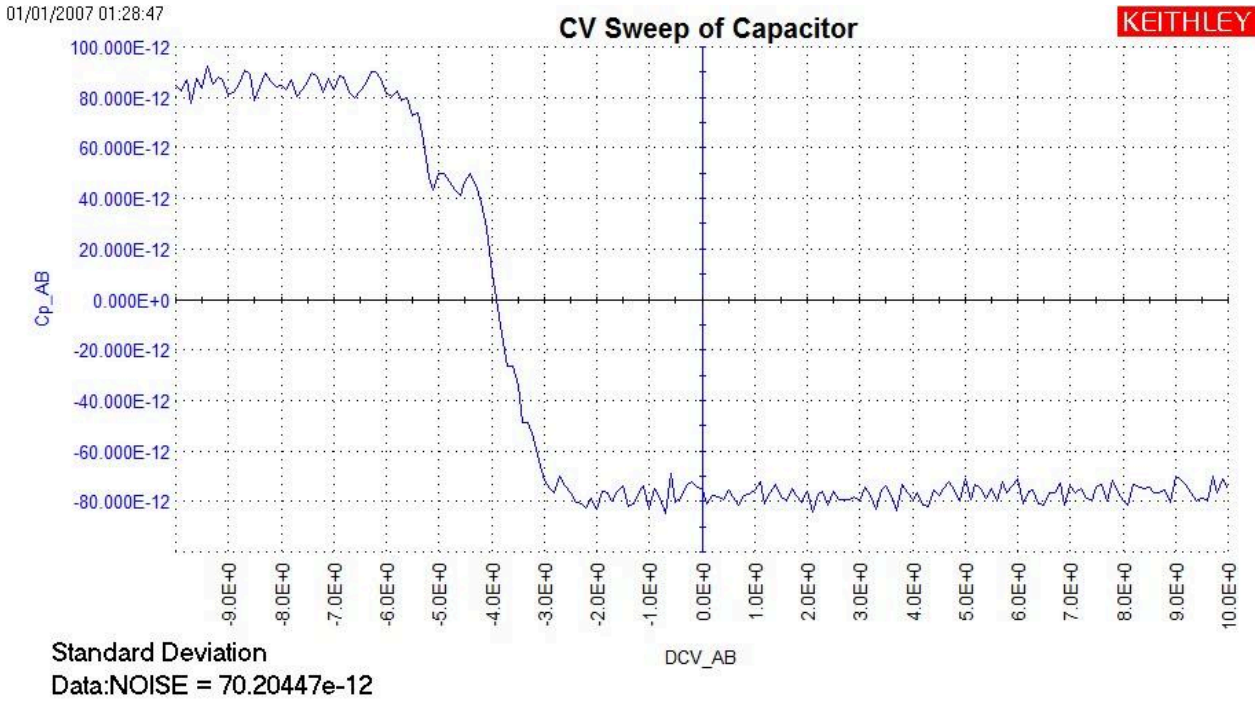
MOSCAP 3 High Frequency (1Mhz):



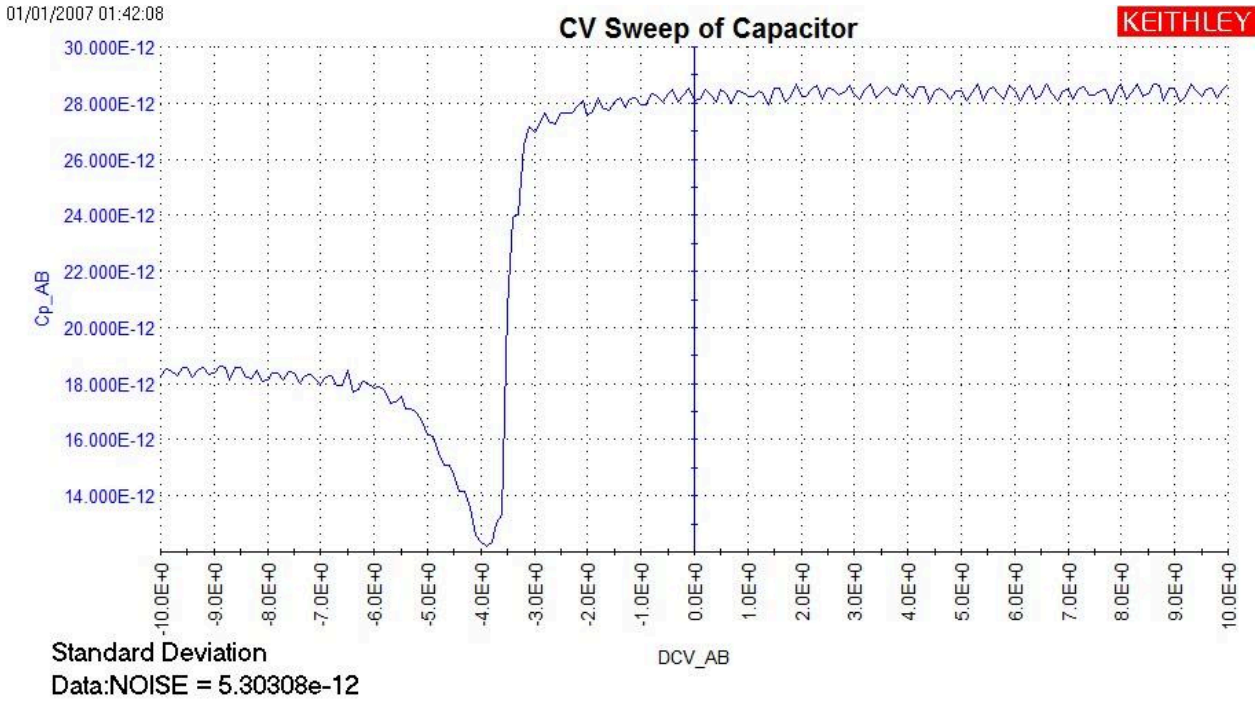
MOSCAP 3 Low Frequency:



MOSCAP 4 High Frequency (1Mhz):



MOSCAP 4 Low Frequency:

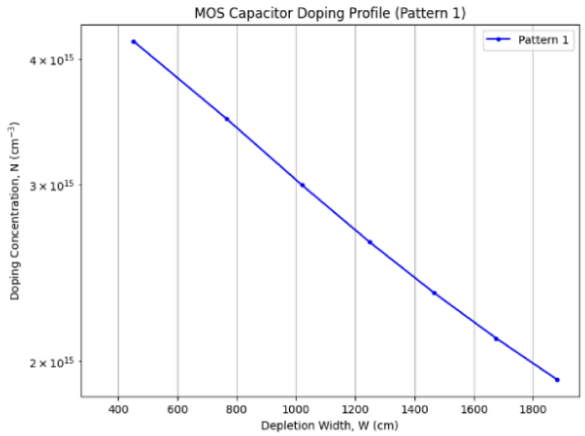


The high frequency and low frequency C-V plots follow the rough curve of the C-V plots outlined in literature for P-type MOSCAPS as showcased in Figure 4.

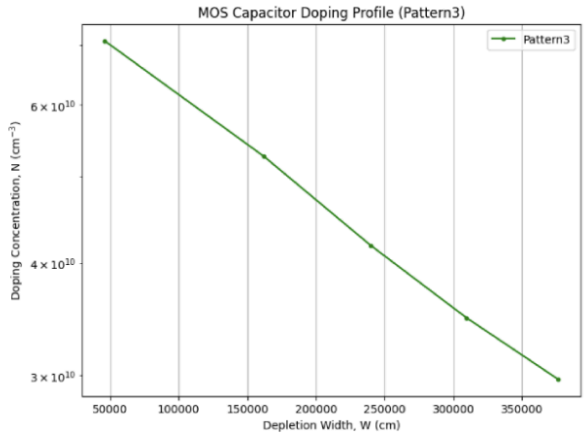
3.6 Analysis

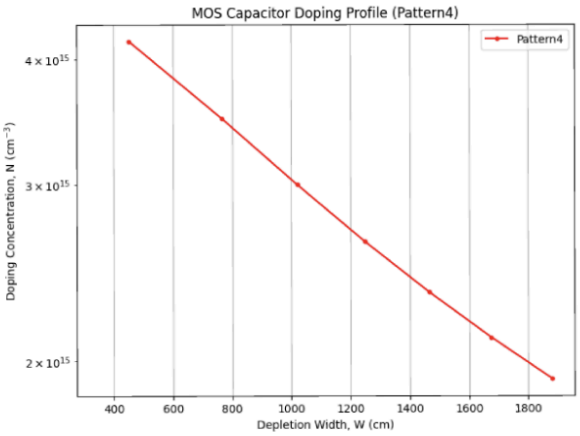
In order to extract the dopant profile from our C-V measurements, we only look at the high frequency C-V curves and extract the capacitance (and corresponding voltage) values from the depletion region.

Code: Copy of DopantProfile2.ipynb



The nearly straight-line results indicate that the wafer's p-type doping is both light and uniform, so the measured doping does not vary much with depth in the depletion region. Because the analysis focuses only on the true depletion regime of the MOS capacitor (rather than including accumulation or inversion data), the extracted doping appears constant and changes only slightly with depletion width. These findings match what one would expect from a well-fabricated MOSCAP on a uniformly doped wafer, suggesting that the process and measurements were done successfully, and that the wafer's doping level aligns with its specifications.





4. Experiment 2: N-well in P-doped Si MOSCAP (In Progress)

For the second experiment our goal is to fabricate N-well MOSCAPs and ensure the N-well has uniform carrier concentration. The purpose of this experiment is to conduct C-V measurements and analyze the resultant dopant profiles to see how well they match up with our diffusion model code: Diffusion Model_S25.ipynb. The inputs that we will vary within the diffusion model are the constant source diffusion time and the drive-in diffusion time. As a result, we will get the dopant profile as the output.

The big assumption made in the diffusion model code is the surface concentration value for P504 dopant as that was not provided within the Filmtronics data sheet.

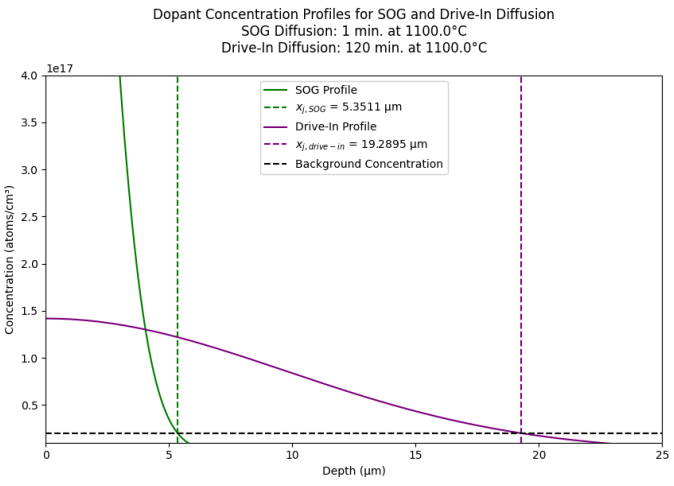
PRODUCT DESCRIPTION
PHOSPOROUS FILM DIFFUSION DATA

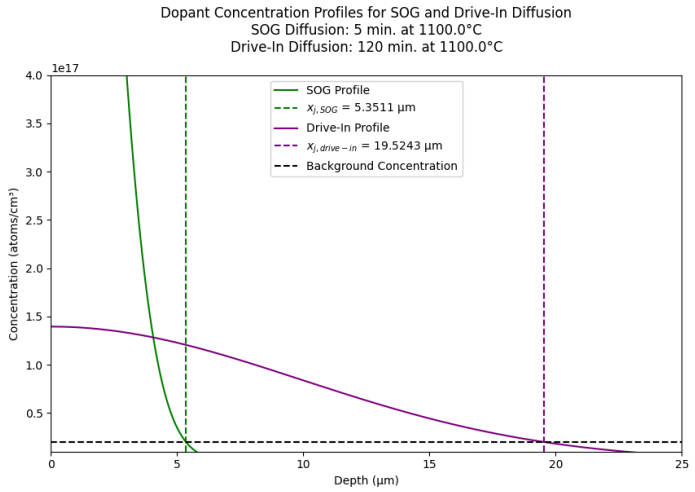
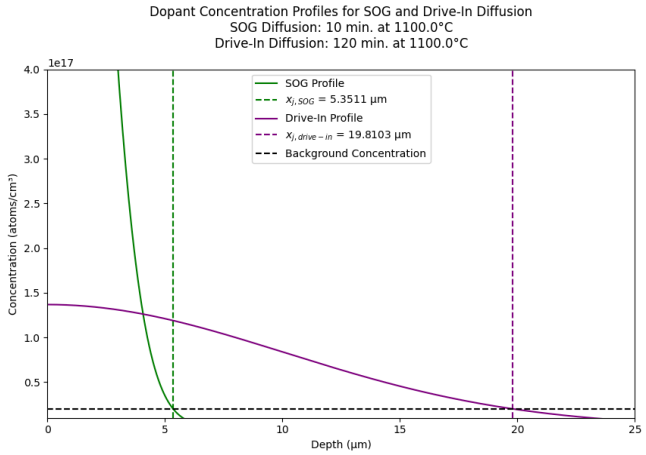
Diffusion Results
Spin Speed 5000 rpm
Silicon Polished P Type 111 10-20 ohm-cm

	30 Minutes 1100°C 25% O_2, 75% N_2	**2.5 Hours** 1100°C 25% O_2, 75% N_2	**60 Minutes** 1220°C 25% O_2, 75% N_2	**90 Minutes** 1235°C 25% O_2, 75% N_2
Solution	Sheet Resistance ohm/square	Sheet Resistance ohm/square	Sheet Resistance ohm/square	Sheet Resistance ohm/square
P450*				0.08
P451*				0.09
P452*				1.00
P509	3.6	2.1	2.8	2.1
P508	4.8	2.2	3.7	3.0
P507	5.8	3.5	5.0	4.0
P506	7.6	3.9	13.0	5.1
P505	20.4	7.5	16.0	7.5
P504	39.2	11.6	40.0	10.6
P503	92.1	25.3	46.0	14.6
P502	182.0	38.5	71.0	17.0
P501	310.0	42.7	91.0	18.0
P500	735.0	47.8	130.0	24.0

By comparing experimental data with the diffusion model's predictions, we can determine the dopant concentration and refine our model's accuracy. Since the total diffusion time must stay below 2.5 hours to ensure MOSCAP functionality, it's crucial to limit the constant-source diffusion period so that the drive-in stage produces a uniform dopant distribution.

Below, we outline the planned N-well fabrication experiments in which the constant-source diffusion time is varied. These time intervals were derived from the diffusion model, identifying the minimum constant-source duration needed to maintain a uniform carrier concentration while meeting overall process constraints.

Temperature	**Constant Source Diffusion time**	**Drive in Diffusion time**	**Plots from diffusion model**
1100 degrees C	1 min	2 hours	

	5 min	2 hours	
	10 min	2 hours	

Within our fabrication process we will additionally be conducting an RCA clean to each of the 3 chips before growing the oxide and after diffusion, to minimize defects and errors in our fabrication process.

The SOP for the RCA clean is outlined here:
Standard Operating Procedure (SOP) for RCA Clean of MOSCAPs

6. Bill of Materials

No additional materials for this project as the Hacker Fab already had the necessary materials and supplies, therefore the cost of the materials used is already included in the operating cost of the Hacker Fab. The materials utilized are listed below.

Materials

- Dopant: Filmtronics P504 SOG (Phosphorus Doped SiO2)

- Al Thermal Deposition Source: Pure Al wire
- Substrate: University Wafer <100> single crystal p type silicon (5-10 ohm-cm)
- Oxide Etchant: Hydrofluoric acid
- Aluminum Etchant: Aluminum (Nitric, Acetic, Phosphoric Acids)

7. References

[1] https://semiconductor.samsung.com/us/support/tools-resources/dictionary/semiconductor-glossary-cmos/

[2] http://sam.zeloof.xyz/wp-content/uploads/2021/01/CV-resource1.pdf

[3] https://km2000.us/franklinduan/articles/ecee.colorado.edu/~bart/book/book/chapter6/ch6_2.htm

[4] http://sam.zeloof.xyz/wp-content/uploads/2021/01/CV-resource1.pdf

C. Hu, "MOS Capacitor," Modern Semiconductor Devices for Integrated Circuits, Prentice Hall, 2009, pp. 157–192.

Hewlett-Packard, Analysis of Semiconductor Capacitance Characteristics: 4280A 1 MHz C Meter/C–V Plotter, Hewlett-Packard Co., Application Note, c. 1980s.