Date:05/21/21

Attendees: Allan, Ali, Anthony, Anu, Craig, David A., David R., Denis, DJ, Giridhar, Gus, Halil, Javi, JP, Kevin, Michael, Mudasir, Myron, Nick, Quinn, Ravi A, Ravi S, Reza, Sam, Scott, Shriganesh, Suresh, Swami, Thomas, Bill, Young, Bapi

https://global.gotomeeting.com/join/950275429

1. Rolling Agenda:
    a. 5/21:
        i. LETI again,
        ii. Storage workshop
        iii. Rohit@Google
    b. 5/28: No meeting
    c. 6/4: David on CDX
    d. 6/11:
    e. 6/25: Storage PoC workshop
    f.
2. Agenda:
    a. LETI
        i. Anu - how are 3D and interposer related.
        ii. Roadmap - photonic interposer? BIll - What does photonic interposer. mean. Photonic interposer means waveguide in a chip. Defined an optical network on chip in the interposer. Working on a demonstrator
        iii. Ravi - what types of chiplets do you have in your library - demo at ISSCC 20? Complex system with 96 cores. Application - high performance compute for edge application.
        iv. Packaging - currently microbump, moving to hybrid copper bonding.
        v. Working on memory - aiming to put it in the interposer.
        vi. What is the energy/bit for the d2d link - 0.59 pj/bit. What is the IP used for D2D communication? - own
        vii. Is the interposer active - yes
        viii. DJ - is there a thermal modeling tool? Thermal simulation will be useful input to the community.
        ix. Are we working on a SerDes - BoW mea
    b. Young
        i. Storage workshop on 6/25
        ii. Software is going to be challenging - asking for comments
        iii. AIm to generate a community and develop a working TCO model
    c. Rohit
        i. Working on an open chiplet specification
        ii. Presented at the end user group

iii. Modeled after an ieee standard. Do want to make it flexible to make it broadly adoptable.
iv. https://docs.google.com/document/d/1b4A_dpuCifnMMwbUh4DwVX6STb7kbSpPf11cDGRLJI8/edit?usp=sharing&resourcekey=0-Tn6jBsOwfUl5mjWOQ4Y63w

3. Announcement
    a.
4. Weekly workstream minutes
    a. BoW - https://github.com/opencomputeproject/ODSA-BoW/issues/38:
        i.
    b. CDX - https://docs.google.com/document/d/1ZVA1_qMWSdIhjHBF21pwucmy9LqAID8f_Qwpog8VcxI/edit?usp=sharing
    c. Link Layer - https://docs.google.com/document/d/1vIbfsgkG4ef8Sqs1IBb1_tvIIjl-ffJS0T8-PnESxTk/edit?usp=sharing
        i.
    d. PIPE - https://docs.google.com/document/d/1g9m6FdBaWzHj8BIRl5ADIbJVT-GR_8ODVaxHTg5Snw0/edit?usp=sharing
        i.
    e. PoC HW https://docs.google.com/document/d/1UOdbOrF2TG7zZQCadLFZ1ujljAkl3FXra5wGJ-QkZ1o/edit?usp=sharing
        i.
    f. PoC SW - https://docs.google.com/document/d/1kpqZL1mH-sMOdA0wWFOcnNLoctSZdo68jw-UEVcqLZo/edit?usp=sharing
        i. Working on remote access
    g. Open HBI - contact Kenneth Ma
    h. Business workflow
        i.
5. Speaker ideas
    a. HBM Thermal Management
    b. Quality and Reliability - ESD, aging, electromigration - Bill HIR workgroup, ANSYS, packaging reliability - thermal effects, mechanical - as applies to chiplets
    c. Anyone making chiplets - commercial talks focused on chiplets
    d. Memory access discussion - HBM, GenZ, OMI - how do they become compatible with chiplets - WD/Micron/IBM/Samsung/SK/Seagate - new protocol? Sequence of memory-focused talks - Allan - October
    e. Prof. Flynn from Michigan
    f. DARPA official CHIPS - Eelco - October/November
    g. CHIPS - Andreas - October

h. TSMC - Bill, Suresh
i. Transaction Protocol for D2D review
j. Bit errors in substrates
k. End user workgroup - DJ
l. Any other foundry (Global) or AMAT?
m. Ken, Open HBI in February
n. Quinn in February - Software
o. Someone @ ARM in Q1
p. Bill@IEEE in March for the HIR
q. Allan - Modular design for mini OAM, bare die on the module
r. Sam will come up with something
s. Ali - top-level architecture - modular design
t. Philippe@Boyd - thermal management
u. Nhat@Rambus - check on internal talks, cover the ISSCC talk
v. Shahab@ISSCC talks - chase them down
w. Ravi - disaggregation of SRAM, persistent memory,
x. DJ@End User in Feb
y. Jawad - How do we use existing chips as chiplets - panel. How do we define a chiplet, isn't this MCM packaging? What's different? What is the current MCM biz model, state of flow. How do understand the die sales model and its relevance for chiplets. Can we use the PoC as a starting point + Ali
z. Ali@Mature process nodes
aa. Get panelists to do longer talks.
bb. OAM expert to do a talk