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Department of Computer Science and Engineering

| Academic Year | : | 2025-2026 | Course Name | : | Digital Design and Computer Organization |
|---------------------|---|-----------------------------------|-------------|---|---|
| Semester | : | 3 RD SEM | Course Code | : | BCS302 |
| Scheme | : | 2022 | L: T:P: C | : | 3:0:2:0 |
| Total Contact hours | : | 40 Hours Theory + 20 Hours Lab | CIE Marks | : | 50 |
| Course Plan Author | : | Mrs. Aruna R | SEE Marks | : | 50 |
| Date | : | 12-08-2025 | Total Marks | : | 100 |

Course Prerequisites:

• BASIC ELECTRONICS AND PSP

Learning Objectives:

- To demonstrate the functionalities of binary logic system
- To explain the working of combinational and sequential logic system
- To realize the basic structure of computer system
- To illustrate the working of I/O operations and processing unit

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes. 1. Chalk and Talk 2. Live Demo with experiments 3. Power point presentation

Course Outcomes:

| CO | A | t the end of the course, student should be able to | Blooms' Level |
|-----|----|---|---------------|
| CO1 | | Apply the K-Map techniques to simplify various Boolean expressions. | L3 |
| CO2 | | Design different types of combinational and sequential circuits along with Verilog programs | L3 |
| CO3 | •• | Describe the fundamentals of machine instructions, addressing modes and Processor performance | L2 |
| CO4 | | Explain the approaches involved in achieving communication between processor and I/O devices. | L2 |
| CO5 | : | Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance | L4 |

Blooms' Taxonomy:

| L1 | L2 | L3 | L4 | L5 | L6 |
|----|----|----|----|----|----|
|----|----|----|----|----|----|



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| Remembering | Understanding | Applying | Analyzing | Evaluating | Creating |
|-------------|---------------|----------|-----------|------------|----------|
| | | _ | | | |

Program Outcomes:

| PO1 | : | Engineering knowledge | PO7 | | Environment and sustainability |
|-----|---|--|------|----|--------------------------------|
| PO2 | : | Problem analysis | PO8 | •• | Ethics |
| PO3 | | Design/development of solutions | PO9 | : | Individual and team work |
| PO4 | : | Conduct investigations of complex problems | PO10 | •• | Communication |
| PO5 | | Modern tool usage | PO11 | •• | Project management and finance |
| PO6 | : | The engineer and society | PO12 | •• | Life-long learning |

Program Specific Outcomes:

| PSO1: | To understand and process the principles of mathematics in the field of information Science by applying different design principles. |
|-------|---|
| PSO2: | To impart the knowledge by experimental methods in multidisciplinary domains. |
| PSO3: | To inculcate communication skills and teamwork in developing the sustainable software's by imparting professional and ethical values. |

CO-PO-PSO Mapping:

| СО | Program Outcomes | | | | | | | | | | | | | |
|--------|------------------|------|------|------|------|------|------|------|------|-------|-------|-------|-------|-------|
| | PO 1 | PO 2 | PO 3 | PO 4 | PO 5 | PO 6 | PO 7 | PO 8 | PO 9 | PO 10 | PO 12 | PSO 1 | PSO 2 | PSO 3 |
| CO1 | 2 | - | - | 1 | - | - | - | - | - | - | - | 2 | - | 1 |
| CO2 | 2 | 3 | - | - | - | - | - | - | - | - | - | - | 2 | 2 |
| CO3 | 2 | - | - | 1 | 2 | - | - | - | - | - | - | - | 2 | - |
| CO4 | 1 | - | 2 | - | - | - | - | - | - | - | - | - | 1 | - |
| CO5 | 2 | - | 2 | 1 | - | - | _ | - | - | - | - | 1 | 2 | 1 |
| Target | 2 | 3 | 2 | 1 | 2 | - | - | - | - | - | - | 1 | 2 | 1 |

Course Content (Syllabus):

| Module 1 | СН | | | |
|--|----|--|--|--|
| Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit. Text book 1: 1.9, 2.4, 2.5, 2.8, 3.1, 3.2, 3.3, 3.5, 3.6, 3.9 | 08 | | | |
| Module 2 | | | | |
| Combinational Logic: Introduction, Combinational Circuits, Design Procedure, Binary Adder-Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, | | | | |



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| Multiplexer, Encoder. Sequential Logic: Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops. | |
|--|----|
| Text book 1: 4.1, 4.2, 4.4, 4.5, 4.9, 4.10, 4.11, 4.12, 5.1, 5.2, 5.3, 5.4. | |
| 20.00 2 0 0 1. 2.2, 2.2, 2.0, 2.0, 2.2, 2.22, 2.2, 2. | |
| Module 3 | |
| Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. | |
| Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes. | 08 |
| Text book 2: 1.2, 1.3, 1.4, 1.6, 2.2, 2.3, 2.4, 2.5 | |
| Module 4 | |
| Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions. | 08 |
| Text book 2: 4.1, 4.2.1, 4.2.2, 4.2.3, 4.4, 5.4, 5.5.1 | |
| Module 5 | |
| Basic Processing Unit: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction. Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance. | 08 |
| Text book 2: 7.1, 7.2, 8.1 | |

PRACTICAL COMPONENT OF IPCC

| Sl. | Experiments |
|--------|---|
| N O | Simulation packages preferred: Multisim, Modelsim, PSpice or any other relevant |
| 1 | Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same using basic gates. |
| 2 | Design a 4 bit full adder and subtractor and simulate the same using basic gates. |
| 3 | Design Verilog HDL to implement simple circuits using structural, Data flow and Behavioral model. |
| 4 | Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor. |
| 5 | Design Verilog HDL to implement Decimal adder. |



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| 6 | Design Verilog program to implement Different types of multiplexer like 2:1, 4:1 and 8:1. |
|---|---|
| 7 | Design Verilog program to implement types of De-Multiplexer. |
| 8 | Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D. |

Schedule of Instruction:

| Class No | | Topic | Date | RBT | СО | Mode |
|-------------|---|--|------|-----|-------------|--------------------------|
| Mod | ule-1 | Introduction to Digital Design | | | | |
| 1. | Introd | luction to subject | | L1 | | PPT |
| 2. | Binary | y Logic | | L1 | | Chalk & Talk |
| 3. | Basic ' | Theorems and Properties of Boolean Algebra | | L1 | | Chalk & Talk |
| 4. | Boolea | an Functions | | L1 | | Chalk & Talk |
| 5. | Digita | l Logic Gates | | L2 | | Chalk & Talk |
| 6. | Introd | luction, The Map Method, Four-Variable Map | | L2 | | Chalk & Talk |
| 7. | Don't- | Care Conditions, | | L2 | Co1& Co2 | Chalk & Talk |
| 8. | NAN | D and NOR Implementation | | L2 | C02 | Chalk & Talk |
| 9. | | Hardware Description Language – Verilog Model of a circuit | | L2 | | PPT |
| 10. | Revisi | ion of module1- | | | | ONLINE QUIZ & Discussion |
| Mod | ule-2 | Process Management | | | | |
| 11. | Introd | uction, Combinational Circuits | | L2 | | PPT |
| 12. | Design | n Procedure | | L2 | | Chalk & Talk |
| 13. | Binary | y Adder- Subtractor, Decoders | | L2 | | Chalk & Talk |
| 14. | Encod | ers, Multiplexers | | L3 | CO2, | Chalk & Talk |
| 15. | HDL N | Models of Combinational Circuits – Adder | | L3 | CO3 | Chalk & Talk |
| 16. | Multip | olexer, Encoder. | | L3 | | Chalk & Talk |
| 17. | Sequential Logic: Introduction, Sequential Circuits | | | L3 | | PPT/Chalk & Talk |
| 18. | Storage Elements: Latches, Flip-Flops | | | L3 | | Chalk & Talk |
| 19. | Revisi | ion of module2 | | | | ONLINE QUIZ & Discussion |
| Mod | ule-3 | Process Synchronization | | | | |
| 20. | Functional Units | | | L3 | | PPT/Chalk & Talk |



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| Class No | | Торіс | Date | RBT | СО | Mode |
|-------------|---|---|------|---------------------|-----|---------------------|
| 21. | Basic | Basic Operational Concepts, Bus structure, L3 CO3, CO4 | | | | PPT/Chalk & Talk |
| 22. | Perfor | Performance – Processor Clock, L3 | | | | |
| 23. | Basic | Performance Equation, | | L3 | | PPT/Chalk & Talk |
| 24. | Clock | Rate, Performance Measurement. | | L3 | | PPT/Chalk & Talk |
| 25. | | ine Instructions and Programs: Memory Location ddresses, Memory Operations, | | L3 | | PPT/Chalk & Talk |
| 26. | Instruction and Instruction sequencing, L3 | | | | | PPT/Chalk & Talk |
| 27. | Addre | ssing Modes. | | | | PPT/Chalk & Talk |
| 28. | Revisi | on – Module 3 | | | | Test |
| Mod | ule-4 | Memory Management | | | | |
| 29. | Inpu | t/output Organization: Accessing I/O Devices, | | L3 | | PPT/Chalk & Talk |
| 30. | Interru | ipts – Interrupt Hardware, | | L3 | | PPT/Chalk & Talk |
| 31. | Enabli | ng and Disabling | | L3 | | PPT/Chalk & Talk |
| 32. | Interr | upts, | | L3 | CO4 | PPT/Chalk & Talk |
| 33. | Handl | ing Multiple Devices, | | L3 | | PPT/Chalk & Talk |
| 34. | Direct | Memory Access: Bus Arbitration, | | L3 | | PPT/Chalk & Talk |
| 35. | Speed | , size and Cost of memory systems. | | L3 | | PPT/Chalk & Talk |
| 36. | Cache Memories – Mapping Functions. | | | L3 | | PPT/Chalk & Talk |
| 27 | D | | | | | Role Play |
| 37. | | ion of module4 | | | | Test |
| Mod | uie-5 | File System, Implementation of File System | | | | - |
| 38. | Basic | Processing Unit: Some Fundamental Concepts: | | L1 | | PPT/Chalk & Talk |
| 39. | Register Transfers, | | | L1 | | PPT/Chalk & Talk |
| 40. | Performing ALU operations, L2 | | | PPT/Chalk & Talk | | |
| 41. | fetching a word from Memory, Storing a word in memory | | | L2 | CO5 | PPT/Chalk & Talk |



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| Class No | Topic | Date | RBT | CO | Mode |
|-------------|--------------------------------------|------|-----|----|--------------------------------------|
| 42. | Execution of a Complete Instruction. | | L2 | | PPT/Chalk & Talk |
| 43. | Pipelining: Basic concepts, | | L2 | | Role Play /Chalk & Talk |
| 44. | Role of Cache memory, | | L1 | | Role Play /Chalk & Talk |
| 45. | Pipeline Performance. | | L1 | | PPT/Chalk & Talk |
| 46. | Revision of module5 | | | | Test |

Practical Component of IPCC

| Lab | Topic | Date | RBT | CO | Mode |
|-----|---|------|-----|-----|-------------------------|
| 1. | Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same using basic gates. | | L2 | CO1 | |
| 2. | Design a 4 bit full adder and subtractor and simulate the same using basic gates. | | L3 | CO1 | PPTs, |
| 3. | Design Verilog HDL to implement simple circuits using structural, Data flow and Behavioral model. | | L3 | CO2 | Chalk & Talk, |
| 4. | Design Verilog HDL to implement Binary Adder-Subtractor - Half and Full Adder, Half and Full Subtractor. | | L1 | CO2 | Practical Simulation |
| 5. | Design Verilog HDL to implement Decimal adder. | | L2 | CO2 | |
| 6. | Design Verilog program to implement Different types of multiplexers like 2:1, 4:1 and 8:1. | | L3 | CO2 | |
| 7. | Design Verilog program to implement types of De-Multiplexer. | | L3 | CO2 | |
| 8. | Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D. | | L3 | CO2 | |

Textbooks



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| T1 | M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education. | | | | | |
|-------|--|--|--|--|--|--|
| T2 | Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill. | | | | | |
| Web I | Web links and Video Lectures (e-Resources): | | | | | |
| | https://sites.google.com/skit.org.in/aruna-r/about-faculty | | | | | |
| | https://cse11-iiith.vlabs.ac.in/ | | | | | |

Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are 25 marks and that for the practical component is 25 marks.
- 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and 10 marks for other 14.09.2023 15.09.2023 Annexure-III 14.09.2023 MKV-TEMPLATE for IPCC (26.04.2022) assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for 25 marks).
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC. CIE for the practical component of the IPCC
- 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test (duration 02/03 hours) after completion of all the experiments shall be conducted for 50 marks and scaled down to 10 marks.
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 25 marks.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC. SEE for IPCC Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours) 1. The question paper will have ten questions. Each question is set for 20 marks. 2. There will be 2 questions from each module. Each of the two questions under a module (with a



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maximum of 3 sub-questions), should have a mix of topics under that module. 3. The students have to answer 5 full questions, selecting one full question from each module. 4. Marks scored by the student shall be proportionally scaled down to 50 Marks The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

| Assessment Schedule: | | | | | | | |
|----------------------|------------------------------|-----------------------|------------------|-------------------|-----------|-------------|--|
| Sl.No. | Assessment type | Contents | СО | Duration In Hours | Mark s | Date & Time | |
| 1 | CIE Test 1 | M1, M2 | CO1, CO2, CO3 | 1.5 | 30 | | |
| 2 | CIE Test 2 | M3, M4 | CO3, CO4, CO5 | 1.5 | 30 | | |
| 3 | Assignment 1 | M1, M2 | CO1, CO2 | | 10 | | |
| 4 | CLASS TEST | M3, M4, M5 | CO3, CO4, CO5 | | 10 | | |
| 6 | Lab assessment Marks | M1, M2, M3, M4, M5 | CO1-CO5 | - | 15 | | |
| 7 | Lab assessment -Lab Internal | M1, M2, M3, M4, M5 | CO1-CO5 | 2 | 10 | | |
| 8 | Semester End Examination | M1, M2, M3, M4, M5 | CO1-CO5 | 3 | 50 | | |

^{**}The sum of three tests, two assignments, and practical sessions will be out of 100 marks and will be scaled down to 50 marks

RB – Text Book/Reference Book, *L – Lecture, V- Videos or any other mode, *RBT – Revised Blooms' Taxonomy, L: T: P: C – Theory/Lecture: Tutorial: Practical/Drawing: Credits, SEE: Semester End Examination, CIE: Continuous Internal Evaluation, Seminar: Group of 6-8 students, Module 1,2,3,4 & 5,

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40%(40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation)and SEE (Semester End Examination) taken together.



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Faculty In charge Course Coordinator HOD