SIR C R REDDY COLLEGE OF ENGINEERING, ELURU-7
DEPT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MID - II

AY & SEM : 2021-22(Sem-II) **Date: 21-06-2022**
Class : II/IV B.Tech (ECE-A,B&C) **Marks: 30**
Subject & Code: DICD (R2022042) **Duration: 90 Min**

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Answer all the questions. Each question carries equal mark. 3X10=30M

Q1a. Explain the operation of Shift Register and HDL code? (5M)
Q1b. Design Asynchronous Up/Down counter and write HDL code? (5M)

Q2a. Write short notes on depletion type NMOS 2 input NOR gate? (5M)

Q2b. Realize NMOS & CMOS complex logic gates using the Boolean function

$Z = \overline{A(D + C) + BE}$? (5M)

Q3a. Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table ? (5M)

Q3b. Draw the D latch by using CMOS logic and explain its operation in detail? (5M)

S.NO	QUESTION	MARKS	CO	RBT
1A	Explain the operation of Shift Register and HDL code?	5	3	K2
1B	Design Asynchronous Up/Down counter and write HDL code?	5	3	K1
2A	Write short notes on depletion type NMOS 2 input NOR gate?	5	4	K3
2B	Realize NMOS & CMOS complex logic gates using the Boolean function $Z = \overline{A(D + C) + BE}$?	5	4	K3
3A	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table?	5	4	K1
3B	Draw the D latch by using CMOS logic and explain its operation in detail?	5	4	K3

S.No	Course Outcomes
CO1	Learn the Hardware Description Language (VHDL & VERILOG).
CO2	Understand the structure of commercially available digital integrated circuit families.
CO3	Analyze and design combinatorial and sequential logic circuits using HDL code.
CO4	Interpret the digital logic circuits using MOS logic circuits

KNOWLEDGE LEVELS

REMEMBERING	UNDERSTANDING	APPLYING	ANALYZING	EVALUATING	CREATING
K1	K2	K3	K4	K5	K6

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MID - I

AY & SEM : 2021-22(Sem-II) **Date: 26-04-2022**
Class : II/IV B.Tech (ECE-A,B&C) **Marks: 30**
Subject & Code: DICD (R2022042) **Duration: 90 Min**

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Answer all the questions. Each question carries equal mark. 3X10=30M

Q1a. Explain structural modeling style with syntax and example HDL code? (5M)
Q1b. Explain all modeling styles of Verilog HDL file with syntax? (5M)

Q2a. Design ALU (IC74381) and explain the functionality with HDL code? (5M)
Q2b. Design and implement four bit parallel adder and HDL code? (5M)

Q3a. Write briefly about Hazards in sequential circuits? (5M)
Q3b. Design Priority encoder (IC74148), write the HDL code? (5M)

S.NO	QUESTION	MARKS	CO	RBT
1A	Explain structural modeling style with syntax and example HDL code?	5	1	K2
1B	Explain all modeling styles of Verilog HDL file with syntax	5	1	K1
2A	Design ALU (IC74381) and explain the functionality with HDL code	5	3	K3
2B	Design and implement four bit parallel adder and HDL code?	5	3	K3
3A	Write briefly about Hazards in sequential circuits?	5	2	K1
3B	Design Priority encoder (IC74148), write the HDL code?	5	3	K3

S.No	Course Outcomes
CO1	Learn the Hardware Description Language (VHDL & VERILOG).
CO2	Understand the structure of commercially available digital integrated circuit families.
CO3	Analyze and design combinatorial and sequential logic circuits using HDL code.
CO4	Interpret the digital logic circuits using MOS logic circuits

KNOWLEDGE LEVELS

REMEMBERING	UNDERSTANDING	APPLYING	ANALYZING	EVALUATING	CREATING
K1	K2	K3	K4	K5	K6

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