RF Analog Circuits With Really Good Features

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***Abstract*—A high-speed transmitter for XXX interface was proposed by using XXXXX. The proposed XXXX chip in a 65nm CMOS process works at frequencies up to 6Gbps , occupies XXXX mm2 and consumes XXX mW at 1V.**

Keywords—xxxx-mode, transmitter, , parellel link

I. INTRODUCTION

High-speed serial link circuits are mostly included in a large digital chip as an analog IP to transmit and receive high-speed serial data between two large digital chips. The main body of the large digital chips are designed by using a Verilog synthesis technique while the high-speed serial link circuits are implemented by using a full-custom design. Recently, some components of high-speed serial link circuits

II. DESIGN OF BUILDING BLOCK

The proposed voltage-mode transmitter consists of two branches for differential operation; each branch is composed of a 2-to-1 multiplexer, a pre-driver, a main driver, an FFE pre-driver, and an FFE driver with the FFE pre-driver output connected to the FFE driver input of the opposite branch. The 2-to-1 multiplexer was implemented with a 2-input NAND gate that works at data rates up to 9Gbps.

Fig. 1. Proposed Circuit Design

III. MEASUREMENT RESUTLS

The proposed output driver for the differential voltage-mode transmitter was fabricated in a 65nm CMOS process (Fig. 2). The fabricated output driver chip was connected to a 1.4m FR4 differential micro-strip line with a measured loss

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REFERENCES

[1] W. Deng, et al., “A 0.0066mm2 780□W Fully Synthesizable PLL with a Current-Output DAC and an Interpolative Phase-Coupled Oscillator Using Edge-Injection Technique,” IEEE International Solid-State Circuits Conference (ISSCC), pp. 266-267, Feb. 2014

[2] W. Deng, et al, “A 0.011 mm2 PVT-Robust Fully-Synthesizable CDR with a Data Rate of 10.05 Gb/s in 28nm FD SOI,” IEEE Asian Solid-State Circuits Conference (ASSCC), pp. 285-288, Nov. 2014