

Frank Vahid Publications

Textbooks

[zyBooks on C++, C, Java, Digital Design, Quantitative Reasoning, Statistics, Computer Organization, Coral, Technical Communication, others.](#)

(2012-2023) Highly-interactive learning material written natively for the web, replacing textbooks and homework systems. Use animation, learning questions, tools, and some text; shown to improve student learning outcomes, participation, and motivation. Used by 1000+ universities, 1,000,000+ students, and 3,000+ instructors to date. Supported by several NSF grants and Google.

[Digital Design](#) By Frank Vahid, John Wiley and Sons publishers, 2nd ed, 2011.

Emphasizes RTL design, optimization/tradeoffs at multiple levels of abstraction, and practical applications; includes extensive examples and explains concepts intuitively and constructively for students. Used in dozens of universities including Univ of Michigan, Texas A&M, Notre Dame, Princeton, UC Irvine, Univ of Arizona, and more. Additional books, which may accompany Digital Design or be used standalone, are "VHDL for Digital Design" and "Verilog for Digital Design". See <http://www.ddvahid.com> for info on all three books, sample slides, online tools, etc.

[Programming Embedded Systems: An Introduction to Time-Oriented Programming](#) By Frank Vahid and Tony Givargis, published by UniWorld Publishing, (c) 2011. Teaches disciplined embedded programming involving

behavior capture using a synchronous state machine computation model to appropriately deal with time-ordered and time-interval behavior common in embedded applications, and structured implementation of the model in C code on a microcontroller. Includes creating a task scheduler for multiple tasks, as well as bit-level manipulation, introduction to control systems and signal processing, and targeting FPGAs via an HDL.

[Embedded System Design -- A Unified Hardware/Software Introduction](#) By

Frank Vahid and Tony Givargis, published by J. Wiley and Sons, (c) 2002.

Emphasizes top-down design involving tradeoffs between programmable processor and custom digital processors. Describes various memory technologies and approaches to interfacing. Includes a digital camera design

example.

[Specification and Design of Embedded Systems](#) By Dan Gajski, Frank Vahid, Sanjiv Narayan, and Jie Gong, published by Prentice Hall, 1994. *Possibly the first book title on embedded systems.*

Journal and Conference Papers

- F. Vahid and A. Pang. Experiences Teaching a CS1 Common Course across 7 Institutions. SIGCSE 2024. [paper](#)
- F. Vahid, A. Pang, B. Denzler. Towards Comprehensive Metrics for Programming Cheat Detection. SIGCSE 2024. [paper](#)
- F. Vahid. CS1 Instructors: Flexibility in Content Approaches is Justified, and can Enable More Cross-University Cooperation. SIGCSE 2024. [paper](#)
- A. Pang and F. Vahid. **Variability-Inducing Requirements for Programs: Increasing Solution Variability for Similarity Checking.** ITiCSE 2023. doi: 10.1145/3587102.3588855 [conference paper](#)
- C. Gordon, S. Zhao, F. Vahid. **Ultra-Lightweight Early Prediction of At-Risk Students in CS1.** SIGCSE 2023. doi: 10.1145/3545945.3569764 [conference paper](#)
- F. Vahid, K. Downey, L. Areizaga, A. Pang. **Experiences Teaching Coral Before C++ in CS1.** SIGCSE 2023. doi: 10.1145/3545945.3569732 [conference paper](#)
- F. Vahid, K. Downey, A. Pang, C. Gordon. **Impact of Several Low-Effort Cheating-Reduction Methods in a CS1 Class.** SIGCSE 2023. doi: 10.1145/3545945.3569731 [conference paper](#)
- Gordon, C.L., Lysecky, R. and Vahid, F., 2022. **Less Is More: Students Skim Lengthy Online Textbooks.** *IEEE Transactions on Education.* doi: 10.1109/TE.2022.3199651. [paper link](#)
- Gordon, C., Lysecky, R. and Vahid, F., 2022, August. **Programming learners struggle as much in Python as in C++ or Java.** In *2022 ASEE Annual Conference & Exposition.* [paper](#)
- Gordon, C., Vahid, F. and Lysecky, R., 2022, August. **Understanding and Promoting Earnest Completion in Online Textbooks.** In *2022 ASEE Annual Conference & Exposition.* [paper](#)
- Vahid, F. and May, D., 2022, August. **Auto-Awarding Points for Incremental**

Development in Programming Courses. In *2022 ASEE Annual Conference & Exposition*. [paper](#)

- Vahid, F., Zhao, S. and Allen, J., 2022, August. **Automated Zoom Chat Analysis Including Chat-Based Polls for an Online Introductory Programming Course.** In *2022 ASEE Annual Conference & Exposition*. *Best paper award*. [paper](#)
- Vahid, F., Givargis, T. and Miller, B., 2022, August. **RIOS: A Task Scheduler in Source Code for Teaching and Implementing Concurrent or Real-Time Software.** In *2022 ASEE Annual Conference & Exposition*. [paper](#)
- Alzahrani, N. and Vahid, F., 2022, August. **Detecting Possible Cheating In Programming Courses Using Drastic Code Change.** In *2022 ASEE Annual Conference & Exposition*. [paper](#)
- Kelly, J., Edgcomb, A., Bruno, J., Gordon, C. and Vahid, F., 2022. **Theory to Practice: Reducing Student Attrition in Online Undergraduate Math.** *International Journal of Research in Education and Science*, 8(2), pp.187-206. <https://doi.org/10.46328/ijres.2622> [paper](#)
- Gordon, C., Lysecky, R. and Vahid, F., 2021, October. **The shift from static college textbooks to customizable content: A case study at zyBooks.** In *2021 IEEE Frontiers in Education Conference (FIE)* (pp. 1-7). IEEE. doi: 10.1109/FIE49875.2021.9637289. [paper link](#)
- Vahid, F., Lysecky, R., Miller, B.A. and Vanderbeek, L., 2021, July. **Coding Trails: Concise Representations of Student Behavior on Programming Tasks.** In *2021 ASEE Virtual Annual Conference Content Access*. doi: 10.18260/1-2--36802. [paper](#)
- Alzahrani, N. and Vahid, F., 2021, July. **Common Logic Errors for Programming Learners: A Three-Decade Literature Survey.** In *2021 ASEE Virtual Annual Conference Content Access*. doi: 10.18260/1-2--36814. [paper](#)
- Alzahrani, N. and Vahid, F., 2021, July. **Progression highlighting for programming courses.** In *2021 ASEE Virtual Annual Conference Content Access*. [paper](#)
- Kazakou, E., Edgcomb, A.D., Rajasekhar, Y., Lysecky, R. and Vahid, F., 2021, July. **Randomized, Structured, Auto-graded Homework: Design Philosophy and Engineering Examples.** In *2021 ASEE Virtual Annual Conference Content Access*. [paper](#)
- Gordon, C.L., Lysecky, R. and Vahid, F., 2021, July. **The rise of program auto-grading in introductory cs courses: A case study of zylabs.** In *2021 ASEE Virtual Annual Conference Content Access*. [paper](#)

- Allen, J.M. and Vahid, F., 2021. **An analysis of using coral many small programs in CS1.** *Journal of Computing Sciences in Colleges*, 36(10), pp.9-16. [paper](#)
- Alzahrani, N. Vahid, F., 2021, March. **Progression Highlighting for Programming Courses.** *Journal of Computing Sciences in Colleges*. [paper](#)
- Allen, J.M. and Vahid, F., 2021, March. **Concise graphical representations of student effort on weekly many small programs.** In *Proceedings of the 52nd ACM Technical Symposium on Computer Science Education (SIGCSE)* (pp. 349-354). doi: 10.1145/3408877.3432551 [paper](#)
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- Allen, J.M. and Vahid, F., 2020, June. **Experiences in Developing a Robust Popular Online CS1 Course for the Past Seven Years.** In *2020 ASEE Virtual Annual Conference Content Access*. doi: 10.18260/1-2--34629 [paper](#)
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Shows that binary-level partitioning and synthesis of a real highly-optimized h264 video decoder application is competitive with source (C) level partitioning/synthesis. Also introduces several simple C coding guidelines that greatly improve synthesis results.
- Gordon-Ross, A. and Vahid, F., 2005, October. **Frequent Loop Detection Using Efficient Non-Intrusive On-Chip Hardware**. *IEEE Transactions on Computers, Special Issue-Embedded Systems, Microarchitecture, and Compilation Techniques in Memory of B. Ramakrishna (Bob) Rau*, 54(10), pp. 1203-1215. [pdf](#)
Describes extensive studies resulting in lean profiler hardware that effectively finds addresses corresponding to frequent loops in an executing software binary.
- Cotterell, S. and Vahid, F., 2005. **Usability of State Based Boolean eBlocks**. *HCI*, July. [pdf](#)
Four basic state-based blocks -- prolonger, tripper, toggle, and pulse generator -- are understandable by novice users and can be connected to define a good range of desired sensor-system behavior.
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Describes an FPGA routing approach that is lean in terms of runtime and memory, running three times faster while using over 15 times less memory than a popular router, yet creating a critical path that is only 30% longer on average and about equal for very large circuits compared to that other router. Our approach, ROCR (Riverside On-Chip Router), can be useful for methods requiring just-in-time FPGA compilation, like our warp processing method, and future methods using a standard FPGA binary.
- Cotterell, S. and Vahid, F., 2005, April. **A logic block enabling logic configuration by non-experts in sensor networks**. In *CHI'05 Extended Abstracts on Human Factors in Computing Systems* (pp. 1925-1928). doi: [10.1145/1056808.1057058](https://doi.org/10.1145/1056808.1057058) [pdf](#)
Describes attempts to build a logic block that non-experts could configure to compute particular sensor conditions (e.g., motion and no light). Shows that a truth table based block is too complicating to non-experts, but a sentence based

block exhibits high success, though being less general. A truth table using color and presented in a sentence format also exhibits reasonable success while being more general.

- Zhang, C., Vahid, F., Yang, J. and Najjar, W., 2005. **A way-halting cache for low-energy high-performance systems**. *ACM Transactions on Architecture and Code Optimization (TACO)*, 2(1), pp.34-54. doi: [10.1145/1061267.1061270](https://doi.org/10.1145/1061267.1061270) [pdf](#)
Describes a cache design that separates the four low-order tags bits into its own fully-associative memory (a halt-tag array). Concurrently with address decoding, the halt-tag array determines mismatches in the low-order four tag bits (of all the tags). A mismatch masks out the decode line, halting further tag and data access. A way-halting cache yields 55% memory access energy savings on average, with no performance overhead.
- Gordon-Ross, A., Vahid, F. and Dutt, N., 2005, April. **A first look at the interplay of code reordering and configurable caches**. In *Proceedings of the 15th ACM Great Lakes symposium on VLSI* (pp. 416-421). doi: [10.1145/1057661.1057760](https://doi.org/10.1145/1057661.1057760) [pdf](#)
Shows that a configurable cache dominates over compiler-based code reordering with respect to tuning an application to a cache for power and performance improvements. Yet, combining the two methods does result in a smaller overall cache size, 13% on average and up to 89%.
- Cotterell, S., Mannion, R., Vahid, F. and Hsieh, H., 2005, April. **eBlocks-an enabling technology for basic sensor based systems**. In *IPSN 2005. Fourth International Symposium on Information Processing in Sensor Networks, 2005*. (pp. 422-427). IEEE. doi: [10.1109/IPSN.2005.1440960](https://doi.org/10.1109/IPSN.2005.1440960) [pdf](#)
Describes how physical eBlock prototypes and a graphical eBlock simulation tool were used by hundreds of users during the development and refinement of eBlock sensor network nodes
- Zhang, C., Vahid, F. and Najjar, W., 2005. **A highly configurable cache for low energy embedded systems**. *ACM Transactions on Embedded Computing Systems (TECS)*, 4(2), pp.363-387. doi: [10.1145/1067915.1067921](https://doi.org/10.1145/1067915.1067921) [pdf](#)
Describes a cache whose total size, associativity, and line size can be configured just by setting a few bits in a configuration register. Provides experimental results demonstrating that tuning the configuration to a particular software application's needs reduces memory access energy by over 40% on average across a large set of benchmarks.
- Lysecky, R. and Vahid, F., 2005, March. **A study of the speedups and competitiveness of FPGA soft processor cores using dynamic hardware/software partitioning**. In *Design, Automation and Test in Europe* (pp. 18-23). IEEE. doi: [10.1109/DATE.2005.38](https://doi.org/10.1109/DATE.2005.38) [pdf](#)

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Highlights speedup and energy results of implementing warp processing, which dynamically and transparently remaps software kernels to FPGA using on-chip synthesis tools, for software running on a Xilinx MicroBlaze soft-core processor. Results show competitive performance and energy compared to software on regular "hard core" embedded microprocessors, thus making soft-cores on FPGA even more attractive beyond just their flexibility of putting different numbers of cores and custom circuitry on a single chip.

- Stitt, G. and Vahid, F., 2005, March. **A decompilation approach to partitioning software for microprocessor/FPGA platforms**. In *Design, Automation and Test in Europe* (pp. 396-397). IEEE. doi: 10.1109/DATE.2005.9 [pdf](#)

Utilizing advanced decompilation techniques enables synthesis of hardware from binaries to recover nearly all high-level constructs that existed in the source code, even for different compiler optimization levels.

- Mannion, R., Hsieh, H., Cotterell, S. and Vahid, F., 2005, March. **System synthesis for networks of programmable blocks**. In *Design, Automation and Test in Europe* (pp. 888-893). IEEE. doi: 10.1109/DATE.2005.289 [pdf](#) [ppt](#)

Describes techniques to automatically convert a network of pre-defined eBlocks into a minimal number of programmable eBlocks, while also generating code for those blocks.

- Stitt, G., Guo, Z., Najjar, W. and Vahid, F., 2005, February. **Techniques for synthesizing binaries to an advanced register/memory structure**. In *Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays* (pp. 118-124). doi: 10.1145/1046192.1046208 [pdf](#)

Advanced decompilation methods can make synthesizing FPGA hardware from software binaries competitive with synthesizing directly from C-level source code, even when utilizing an advanced memory structure (smart buffer) requiring knowledge of loops and arrays. Synthesis from binaries provides numerous advantages of language independence, tool independence, portability, and support of legacy code.

- Cotterell, S., Downey, K. and Vahid, F., 2004, October. **Applications and experiments with eBlocks-electronic blocks for basic sensor-based systems**. In *2004 First Annual IEEE Communications Society Conference on Sensor and Ad Hoc Communications and Networks, 2004. IEEE SECON 2004*. (pp. 7-15). IEEE. doi: 10.1109/SAHCN.2004.1381897 [pdf](#) [ppt](#)

Describes common applications that can be built just by connecting eBlocks together, enabling people without programming experience to build useful sensor-based systems. Summarizes experiences with hundreds of users,

showing success rates even when utilizing logic and state based blocks.

- Zhang, C., Vahid, F., Yang, J. and Najjar, W., 2004, August. **A Way-Halting Cache for Low-Energy High-Performance Systems**. International Symposium on Low-Power Electronics and Design (ISLPED), pp. 126-131. [pdf](#)
Describes a cache whose tag comparison logic includes a small and fast fully-associative memory that quickly detects a mismatch in a particular cache way, and then halts further tag and data access of that way, thus saving power.
- Lysecky, R., Vahid, F. and Tan, S.X.D., 2004, June. **Dynamic FPGA routing for just-in-time FPGA compilation**. In *Proceedings of the 41st annual design automation conference*(pp. 954-959). doi: [10.1145/996566.996819](#) [pdf](#) [ppt](#)
Describes an FPGA routing heuristic suitable for execution on-chip, to support Just-in-Time compilation for FPGAs.
- Gordon-Ross, A., Zhang, C., Vahid, F. and Dutt, N., 2004. **Tuning caches to applications for low-energy embedded systems**. *Ultra Low-Power Electronics and Design*, pp.103-122. doi: [10.1007/1-4020-8076-X_6](#) [pdf](#)
- Zhang, C., Vahid, F. and Lysecky, R., 2004. **A self-tuning cache architecture for embedded systems**. *ACM Transactions on Embedded Computing Systems (TECS)*, 3(2), pp.407-425. doi: [10.1145/993396.993405](#) [pdf](#)
Describes a configurable cache that monitors its own hit rate, and automatically reconfigures the cache's number of ways (associativity), line size and total size to reduce power and/or improve performance, using an efficient heuristic that not only prunes the configuration search space but also avoids cache flushes during the search.
- Guo, Z., Najjar, W., Vahid, F. and Vissers, K., 2004, February. **A quantitative analysis of the speedup factors of FPGAs over processors**. In *Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays*(pp. 162-170). doi: [10.1145/968280.968304](#) [pdf](#)
- Lysecky, R. and Vahid, F., 2004, February. **A configurable logic architecture for dynamic hardware/software partitioning**. In *Proceedings Design, Automation and Test in Europe Conference and Exhibition* (Vol. 1, pp. 480-485). IEEE. doi: [10.1109/DATE.2004.1268892](#) [pdf](#) [ppt](#)
Describes a simple configurable logic (FPGA) fabric and surrounding architecture specifically intended to support dynamic hardware/software partitioning -- meaning on-chip CAD tools must be able to quickly map a netlist to the fabric.
- Gordon-Ross, A., Vahid, F. and Dutt, N., 2004, February. **Automatic tuning of two-level caches to embedded applications**. In *Proceedings Design, Automation and Test in Europe Conference and Exhibition* (Vol. 1, pp. 208-213).

IEEE. doi: 10.1109/DATE.2004.1268850 [pdf](#) [ppt](#)

Describes efficient heuristics for tuning a two-level cache to a particular application, obtaining near-optimal memory-access energy savings of 53%-55% through such tuning, while exploring a mere 6% of the total configuration space.

- Zhang, C. and Vahid, F., 2004, February. **Using a victim buffer in an application-specific memory hierarchy.** In *Proceedings Design, Automation and Test in Europe Conference and Exhibition* (Vol. 1, pp. 220-225). IEEE. doi: 10.1109/DATE.2004.1268852 [pdf](#) [ppt](#)
Adding to a cache a configurable victim buffer, which can be turned on or off, improves memory-access energy of an application by up to 43%. Such savings occur even if the cache itself is configurable. Making the buffer configurable enables us to shut off the buffer for some applications that otherwise would suffer increased energy and performance penalties of up to 4%.
- Zhang, C., Vahid, F. and Lysecky, R., 2004, February. **A Self-Tuning Cache Architecture for Embedded Systems.** Design Automation and Test in Europe Conference (DATE), pp. 142-147. [pdf](#) [ppt](#)
Describes a configurable cache that can tune its total size, associativity, and line size to an executing application. The search heuristic is carefully designed to avoid flushing. The cache transparently reduces memory-access related energy by 45%-55% on average, and by as much as 97% for particular applications.
- Zhang, C., Yang, J. and Vahid, F., 2004, February. **Low static-power frequent-value data caches.** In *Proceedings Design, Automation and Test in Europe Conference and Exhibition* (Vol. 1, pp. 214-219). IEEE. doi: 10.1109/DATE.2004.1268851 [pdf](#) [ppt](#)
Improves upon Yang/Gupta's previous frequent value cache, by eliminating performance overhead, and saving static power in addition to dynamic power, using circuit level design improvements. A frequent value cache encodes commonly-occurring data values into just a few bits, shutting down the remaining bit storage cells. 33% static energy savings are obtained.
- Stitt, G., Vahid, F. and Nematbakhsh, S., 2004. **Energy savings and speedups from partitioning critical software loops to hardware in embedded systems.** *ACM Transactions on Embedded Computing Systems (TECS)*, 3(1), pp.218-232. doi: 10.1145/972627.972637 [pdf](#)
Partitioning a program's kernels to FPGA hardware can reduce overall system energy.
- Zhang, C., Vahid, F., Yang, J. and Walid, W., 2003. **A way-halting cache for low-energy high-performance systems.** *IEEE Computer Architecture Letters*, 2(1), pp.5-5. doi: 10.1109/L-CA.2003.2 [pdf](#)
The first four bits of a cache's tags are stored in a fast efficient CAM and

accessed concurrently with set decoding -- if those four bits mismatch for the decoded set, the full tag comparisons and data array accesses are "halted," thus saving power, with no performance overhead (unlike other power-saving caches).

- Gordon-Ross, A. and Vahid, F., 2003, October. **Frequent loop detection using efficient non-intrusive on-chip hardware**. In *Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems*(pp. 117-124). doi: [10.1145/951710.951728](https://doi.org/10.1145/951710.951728) [pdf](#)
Describes efficient non-intrusive hardware for detecting the most frequent loops in an executing binary, and the relative frequencies of those loops.
- Cotterell, S., Vahid, F., Najjar, W. and Hsieh, H., 2003, October. **First results with eBlocks: embedded systems building blocks**. In *Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis* (pp. 168-175). doi: [10.1145/944645.944690](https://doi.org/10.1145/944645.944690) [pdf](#)
Describes embedded system building blocks that people with no training can connect together to build simple but useful systems.
- Lysecky, R. and Vahid, F., 2003, October. **A codesigned on-chip logic minimizer**. In *Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis* (pp. 109-113). doi: [10.1145/944645.944677](https://doi.org/10.1145/944645.944677) [pdf](#)
Hardware/software partitioning of an on-chip logic minimizer results in 8x speedup and 60% energy savings, improving the usefulness of on-chip logic minimization in a variety of applications.
- Gordon-Ross, A., Cotterell, S. and Vahid, F., 2003. **Tiny instruction caches for low power embedded systems**. *ACM Transactions on Embedded Computing Systems (TECS)*, 2(4), pp.449-481. doi: [10.1145/950162.950163](https://doi.org/10.1145/950162.950163) [pdf](#)
Putting a very small (e.g., 128 word) loop cache in front of L1 instruction cache can greatly reduce power, with no performance overhead.
- Suresh, D.C., Najjar, W.A., Vahid, F., Villarreal, J.R. and Stitt, G., 2003, June. **Profiling tools for hardware/software partitioning of embedded applications**. In *Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems* (pp. 189-198). doi: [10.1145/780732.780759](https://doi.org/10.1145/780732.780759) [pdf](#)
- Zhang, C., Vahid, F. and Najjar, W., 2003, May. **A highly configurable cache architecture for embedded systems**. In *Proceedings of the 30th annual international symposium on Computer architecture* (pp. 136-146). doi: [10.1145/859618.859635](https://doi.org/10.1145/859618.859635) [pdf](#)
A cache with whose number of ways and total size can be tuned to a particular program yields big energy savings with almost no performance overhead.

- Zhang, C. and Vahid, F., 2003, June. **Cache configuration exploration on prototyping platforms**. In *14th IEEE International Workshop on Rapid Systems Prototyping, 2003. Proceedings*. (pp. 164-170). IEEE. doi: 10.1109/IWRSP.2003.1207044 [pdf](#)
 Methods to automatically tune a configurable cache to a particular software application.
- Stitt, G., Lysecky, R. and Vahid, F., 2003, June. **Dynamic hardware/software partitioning: A first approach**. In *Proceedings of the 40th annual Design Automation Conference* (pp. 250-255). doi: 10.1145/775832.775896 [pdf](#)
 Dynamically partitioning an executing software application onto on-chip FPGA is not only possible, but quite effective.
- Lysecky, R. and Vahid, F., 2003, June. **On-chip logic minimization**. In *Proceedings of the 40th annual Design Automation Conference* (pp. 334-337). doi: 10.1145/775832.775918 [pdf](#)
 Executing a lean form of logic minimization on-chip is feasible and has several immediate applications in networking.
- Vahid, F., 2003, June. **Embedded system design: UCR's undergraduate three-course sequence**. In *Proceedings 2003 IEEE International Conference on Microelectronic Systems Education. MSE'03* (pp. 72-73). IEEE. doi: 10.1109/MSE.2003.1205260 [paper link](#)
 Summarizes UCR's successful 3-course sequence on embedded system design, based on the new ESD book (see above) that emphasizes a unified view of hardware and software.
- Vahid, F., 2003. **The softening of hardware**. *Computer*, 36(4), pp.27-34. doi: 10.1109/MC.2003.1193225 [pdf](#)
 A new perspective on hardware becoming much more like software, due in part to configurable logic, and in part to hardware being created today by compiling high-level languages.
- Vahid, F., Lysecky, R., Zhang, C. and Stitt, G., 2003. **Highly configurable platforms for embedded computing systems**. *Microelectronics journal*, 34(11), pp.1025-1029. DOI: 10.1016/S0026-2692(03)00171-X [pdf](#)
 The case for creating platform chips with much configurability, including on-chip FPGA, configurable cache, etc.
[Online version](#)
- Vahid, F., 2003. **Making the best of those extra transistors**. *IEEE Design & Test of Computers*, 20(1), p.96. doi: 10.1109/MDT.2003.1189241 [pdf](#)
 An argument for new uses of the abundant transistors on modern chips.

- Zhang, C., Vahid, F. and Najjar, W., 2003, February. **Energy benefits of a configurable line size cache for embedded systems.** In *IEEE Computer Society Annual Symposium on VLSI, 2003. Proceedings.* (pp. 87-91). IEEE. doi: 10.1109/ISVLSI.2003.1183357 [pdf](#)
 Creating a cache with a line size that can be configured to 16, 32 or 64 bytes results in suprisingly large energy savings.
- Givargis, T. and Vahid, F., 2002. **Platune: A tuning framework for system-on-a-chip platforms.** *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 21(11), pp.1317-1327. doi: 10.1109/TCAD.2002.804107 [pdf](#)
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Selected for special issue from earlier version of paper in Compilers and Operating Systems for Low Power (COLP'01).
Describes the size and power advantages of recognizing that software-configurable control registers in peripherals may never change after being initialized, if the software itself never changes (as is common in embedded systems).
- Givargis, T., Vahid, F. and Henkel, J., 2001, November. **System-level exploration for pareto-optimal configurations in parameterized systems-on-a-chip.** In *IEEE/ACM International Conference on Computer Aided Design. ICCAD 2001. IEEE/ACM Digest of Technical Papers (Cat. No. 01CH37281)*(pp. 25-30). IEEE. doi: 10.1109/ICCAD.2001.968593 [pdf](#) [html slides](#)
Provides a technique for efficiently exploring the configuration space of a parameterized system-on-a-chip (SOC) architecture to find all Pareto-optimal configurations. These configurations represent the range of meaningful power and performance tradeoffs that are obtainable by adjusting parameter values for a fixed application mapped onto the SOC architecture. Our approach extensively prunes the potentially large configuration space by taking advantage of parameter dependencies. We have successfully incorporated our technique into the parameterized SOC tuning environment (Platune) and applied it to a number of applications.
- Givargis, T.D., Vahid, F. and Henkel, J., 2001. **Evaluating power consumption of parameterized cache and bus architectures in system-on-a-chip designs.** *IEEE transactions on very large scale integration (VLSI) systems*, 9(4), pp.500-508.
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Architectures with parameterizable cache and bus can support large tradeoffs between performance and power. We provide simulation data showing the large

tradeoffs by such an architecture for several applications, and demonstrating that the cache and bus should be configured simultaneously to find the optimal solutions. Furthermore, we describe analytical techniques for speeding up the cache/bus power and performance evaluation by several orders of magnitude over simulation, while maintaining sufficient accuracy with respect to simulation-based approaches.

- Vahid, F. and Gordon-Ross, A., 2001, August. **A self-optimizing embedded microprocessor using a loop table for low power**. In *Proceedings of the 2001 international symposium on low power electronics and design* (pp. 219-224). doi: 10.1145/383082.383138 [pdf](#) [html](#) [slides](#)
Describes the architecture and methodology of an embedded microprocessor that can automatically tune itself to the particular application that will run. The particular tunable component described is a loop table, similar to a loop cache except that its contents never change after the most frequent loops are detected.
- Vahid, F. and Givargis, T., 2001. **Platform tuning for embedded systems design**. *Computer*, 34(2), pp.112-114. doi: 10.1109/2.901171 [pdf](#)
Provides an overview of the philosophy of our UCR Dalton Project, in particular, the idea of tuning a programmable system-on-a-chip architecture to the one application that it will eventually run forever.
- Givargis, T.D., Vahid, F. and Henkel, J., 2001, January. **Trace-driven system-level power evaluation of system-on-a-chip peripheral cores**. In *Proceedings of the 2001 Asia and South Pacific Design Automation Conference* (pp. 306-312). doi: 10.1145/370155.370363 [pdf](#) [html](#)
Our earlier work for fast evaluation of power consumption of general cores in a system-on-a-chip described techniques that involved isolating high-level instructions of a core, measuring gate-level power consumption per instruction, and then annotating a system-level simulation model with the obtained data. In this work, we describe a method for speeding up the evaluation further, through the use of instruction traces and trace simulators for every core, not just microprocessor cores. Our method shows noticeable speedups at an acceptable loss of accuracy. We show that reducing trace sizes can speed up the method even further. The speedups allow for more extensive system-level power exploration and hence better optimization.
- Stitt, G., Vahid, F., Givargis, T. and Lysecky, R., 2000, November. **A first-step towards an architecture tuning methodology for low power**. In *Proceedings of the 2000 international conference on Compilers, architecture, and synthesis for embedded systems* (pp. 187-192). doi: 10.1145/354880.354906 [pdf](#) [html](#) [slides](#)
We describe an automated environment to assist a system-on-a-chip designer to

tune a microprocessor core to a particular application program that will run on the microprocessor, and vice-versa, with the goal of reducing embedded system power consumption. We limit such tuning to modifications that do not change the microprocessor instruction set, thus avoiding the large costs that would come with such a change. Our tuning environment for the 8051 microcontroller is freely-available on the web.

- Givargis, T., Vahid, F. and Henkel, J., 2000, September. **Instruction-based System-level Power Evaluation of System-on-a-chip Peripheral Cores.** IEEE/ACM International Symposium on System Synthesis (ISSS), pp. 163-169. [pdf](#) [slides](#)

We propose a new technique, suitable for a variety of cores like peripheral cores, that is the first to combine gate-level power data with a system-level simulation model written in C++ or Java. For that purpose, we investigated peripheral cores and decomposed their functionality into so-called instructions. Our technique addresses a core-based system design paradigm. We show that our technique is sufficiently accurate for making power-related system-level design decisions, and that its computation time is orders of magnitude smaller than lower-level simulation approaches.

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The Peripheral Virtual Component Interface, or PVCI, is a standard intended to simplify the interfacing of peripheral cores to on-chip buses in a system-on-a-chip, by standardizing the interface between a core's internals and its bus wrapper. We provide results of experiments intended to determine the power, performance, and size overhead associated with using a PVCI bus wrapper versus using a non-PVCI bus wrapper, and versus using no bus wrapper at all. The results demonstrate that using a bus wrapper may result in only small performance, power and size overhead versus using no wrapper, though even that performance overhead can be reduced or eliminated using pre-fetching. The results also demonstrate that using a PVCI bus wrapper yields no significant additional power, performance or size overhead compared with a non-PVCI bus wrapper.

- Givargis, T. and Vahid, F., 2000, May. **Parameterized System Design.** IEEE/ACM International Workshop on Hardware/Software Codesign (CODES), pp. 98-102. [pdf](#) [html](#)

Continued growth in chip capacity has led to new methodologies stressing reuse, not only of pre-designed processing components, but even of entire pre-designed

architectures. To be used across a variety of applications, such architectures must be heavily parameterized, so they can adapt to those applications' differing constraints by trading off power, performance and size. We describe several parameterized system design issues, and provide results showing how a single architecture with easily configurable parameters can support a wide range of tradeoffs.

- Givargis, T.D., Vahid, F. and Henkel, J., 2000, January. **Fast cache and bus power estimation for parameterized system-on-a-chip design.** In *Proceedings of the conference on Design, automation and test in Europe* (pp. 333-339). doi: 10.1145/343647.343791 [pdf](#) [html](#) [slides](#)
We present a technique for fast estimation of the power consumed by the cache and bus sub-system of a parameterized system-on-a-chip design for a given application. The technique uses a two-step approach of first collecting intermediate data about an application using simulation, and then using equations to rapidly predict the performance and power consumption for each of thousands of possible configurations of system parameters, such as cache size and associativity and bus size and encoding. The estimations display good absolute as well as relative accuracy for various examples, and are obtained in dramatically less time than other techniques, making possible the future use of powerful search heuristics.
- Lysecky, R.L., Vahid, F. and Givargis, T.D., 2000, January. **Techniques for reducing read latency of core bus wrappers.** In *Proceedings of the conference on Design, automation and test in Europe* (pp. 84-91). doi: 10.1145/343647.343710 Best Paper Award. [pdf](#) [html](#) [slides](#)
Today's system-on-a-chip designs consist of many cores. To enable cores to be easily integrated into different systems, many propose creating cores with their internal logic separated from their bus wrapper. This separation may introduce extra read latency. Pre-fetching register data into register copies in the bus wrapper can reduce or eliminate this extra latency. In this paper, we introduce a technique for automatically designing a pre-fetch unit that satisfies user-imposed register-access constraints. The technique benefits from mapping the pre-fetching problem to the well-known real-time process scheduling problem. We then extend the technique to allow user-specified register interdependencies, using a Petri Net model, resulting in even more efficient pre-fetch schedules.
- Givargis, T., Vahid, F. and Henkel, J., 2000, January. **A hybrid approach for core-based system-level power modeling.** In *Proceedings of the 2000 Asia and South Pacific Design Automation Conference* (pp. 141-146). doi: 10.1145/368434.368593 [pdf](#) [html](#)
Describes a technique for obtaining fast yet accurate power estimations of

core-based systems. The main idea is to use an object-oriented language (C++ or Java) to create a system-level model, modeling each core as an object, and extending each object with power-estimation methods based on statistics from low-level power data of a synthesized version of the core. By executing the system-level model, which runs about 1000x faster than gate-level simulation, we obtain very accurate power estimates.

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Demonstrates, through experiments on four applications, the large power, performance and size tradeoffs possible just by varying architectural parameters relating to cache and bus for a given reference architecture. Illustrates that these parameters must be tuned to one another for each application, and thus argues for the need for a parameter exploration environment in a configure-and-execute design paradigm.
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Introduces a method to reduce or eliminate the extra latency that may arise when reading from a core designed with a bus wrappers for ease of retargeting to different system buses. The method involves pre-fetching registers from the core's internals to registers added in the bus wrapper, akin to caching.
- Vahid, F. and Givargis, T., 1999, March. **The case for a configure-and-execute paradigm**. In *Proceedings of the seventh international workshop on Hardware/software codesign* (pp. 59-63). doi: 10.1145/301177.301211 [pdf](#) [html](#)
Provides an argument, supported by data obtained by various researchers, in favor of building systems-on-a-chip by configuring a pre-designed reference design already in silicon, rather than building systems by connecting large numbers of cores.
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Describes a method for describing a system built from pre-designed system components (cores) at the system level, using an object-oriented language, resulting in dramatically faster simulations than approaches based on HDL's.
- Givargis, T. and Vahid, F., 1998, December. **Interface exploration for reduced power in core-based systems.** In *Proceedings. 11th International Symposium on System Synthesis (Cat. No. 98EX210)* (pp. 117-122). IEEE. doi: 10.1109/ISSS.1998.730611 [pdf](#) [html](#)
Provides equations developed to enable one to explore various bus configurations in a parameterized architecture very rapidly. One simulates an application once, from which bus traffic data is accumulated, and then fed into a tool that analyzes each bus configuration in constant-time using the equations. The power or performance optimal bus can thus be quickly selected for a given application.
- Gajski, D.D., Vahid, F., Narayan, S. and Gong, J., 1998, May. **System-level exploration with SpecSyn.** In *Proceedings of the 35th Annual Design Automation Conference* (pp. 812-817). doi: [10.1145/277044.277252](https://doi.org/10.1145/277044.277252) [pdf](#)
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Patents

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F. Vahid, R. Lysecky, G. Stitt. Warp Processor for Dynamic Hardware/Software Partitioning. US Patent 7,356,672, May 28, 2004.
J. Henkel, T. Givargis, F. Vahid, Method for core-based system-level power modeling using object-oriented techniques. U.S. Patent #6,865,526, June 24, 2000.

Talks (not associated with conference papers above)

[Getting Students to Earnestly Do Reading, Studying, and Homework in an Introductory Programming Class](#), SIGCSE Technical Symposium, Seattle, March 2017.

[Effectiveness of Interactive Web-Native Content vs. Online Textbooks](#) [static vs interactive 061514 925pm FV.pptx](#), ASEE Annual Conference, Indianapolis, June 2014 (**Best paper award**).

[Zyante's zyBooks](#), SJSU's NSF Workshop on MOOCs and Online Technologies, June 2014 (also UCR Innovation Day, May 2014).

[Building Fake Body Parts: Digital Mockups](#), Texas A&M, Feb 2013 (also U Arkansas, Oct 2013).

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[Portable FPGA Applications: Warp Processing and SystemC Bytecode](#) -- Keynote talk, Reconfigurable Architectures Workshop (RAW), 2009, Rome, Italy

[Warp Processing](#) -- Univ. of California, San Diego, Dept. of CS&E, Nov 2008

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[Warp Processor: A Dynamically Reconfigurable Coprocessor](#) -- Talk at Intel's System Design Symposium (San Jose), Nov. 2005

[Supercomputing in a Pencil Tip](#) -- Talk at UCR's Engineering Industry Day, Oct 2005

[Silicon prototyping issues](#) -- Panel talk at Intel, May 2005

[eBlocks](#) -- Talk at UCSD, April 2005

[eBlocks](#) -- Talk at Intel, September 2004

[Warp Processors](#) -- Distinguished Lecture at ASU, April 2004

[Warp Processors](#) -- Talk at IBM Research, Yorktown Heights, Apr 2004

[Warp Processors](#) -- SRC annual review talk, March 2004

[Self-Improving Configurable IC Platforms](#) -- SRC annual review talk, February 2003

[Improving Embedded System Software Speed and Energy using](#)

[Microprocessor/FPGA Platform ICs](#) -- UCR colloquium talk, October 2002

[New Opportunities with Platform-Based Design](#) -- Keynote talk at ESCODES'02

[System-on-a-Chip Platform Tuning for Embedded Systems](#) -- given at 2002

Southern California Embedded Systems Seminar

[Recent Results at UCR with Configurable Cache and Hw/Sw Partitioning](#) -- given at Triscend Corp., September 2002. For publications supported by NSF awards:

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