Frank Vahid Publications

Textbooks

zyBooks on C++, C, Java, Digital Design, Quantitative Reasoning, Statistics, Computer Organization, Coral, Technical Communication, others. (2012-2023) Highly-interactive learning material written natively for the web, replacing textbooks and homework systems. Use animation, learning questions, tools, and some text; shown to improve student learning outcomes, participation, and motivation. Used by 1000+ universities, 1,000,000+ students, and 3,000+ instructors to date. Supported by several NSF grants and Google.

Digital Design By Frank Vahid, John Wiley and Sons publishers, 2nd ed, 2011. Emphasizes RTL design, optimization/tradeoffs at multiple levels of abstraction, and practical applications; includes extensive examples and explains concepts intuitively and constructively for students. Used in dozens of universities including Univ of Michigan, Texas A&M, Notre Dame, Princeton, UC Irvine, Univ of Arizona, and more. Additional books, which may accompany Digital Design or be used standalone, are "VHDL for Digital Design" and "Verilog for Digital Design". See http://www.ddvahid.com for info on all three books, sample slides, online tools, etc.

Programming Embedded Systems: An Introduction to Time-Oriented Programming By Frank Vahid and Tony Givargis, published by UniWorld Publishing, (c) 2011. Teaches disciplined embedded programming involving behavior capture using a synchronous state machine computation model to appropriately deal with time-ordered and time-interval behavior common in embedded applications, and structured implementation of the model in C code on a microcontroller. Includes creating a task scheduler for multiple tasks, as well as bit-level manipulation, introduction to control systems and signal processing, and targeting FPGAs via an HDL.

Embedded System Design -- A Unified Hardware/Software Introduction By Frank Vahid and Tony Givargis, published by J. Wiley and Sons, (c) 2002. Emphasizes top-down design involving tradeoffs between programmable processor and custom digital processors. Describes various memory technologies and approaches to interfacing. Includes a digital camera design

example.

Specification and Design of Embedded Systems By Dan Gajski, Frank Vahid, Sanjiv Narayan, and Jie Gong, published by Prentice Hall, 1994. *Possibly the first book title on embedded systems.*

Journal and Conference Papers

- F. Vahid and A. Pang. Experiences Teaching a CS1 Common Course across 7 Institutions. SIGCSE 2024 (to appear March 2024).
- F. Vahid, A. Pang, B. Denzler. Towards Comprehensive Metrics for Programming Cheat Detection. SIGCSE 2024 (to appear March 2024).
- F. Vahid. CS1 Instructors: Flexibility in Content Approaches is Justified, and can Enable More Cross-University Cooperation. SIGCSE 2024 (to appear March 2024).
- A. Pang and F. Vahid. **Variability-Inducing Requirements for Programs: Increasing Solution Variability for Similarity Checking**. ITiCSE 2023. doi: 10.1145/3587102.3588855 conference paper
- C. Gordon, S. Zhao, F. Vahid. **Ultra-Lightweight Early Prediction of At-Risk Students in CS1**. SIGCSE 2023. doi: 10.1145/3545945.3569764 conference paper
- F. Vahid, K. Downey, L. Areizaga, A. Pang. **Experiences Teaching Coral Before C++ in CS1**. SIGCSE 2023. doi: 10.1145/3545945.3569732 conference paper
- F. Vahid, K. Downey, A. Pang, C. Gordon. **Impact of Several Low-Effort Cheating-Reduction Methods in a CS1 Class**. SIGCSE 2023. doi: 10.1145/3545945.3569731 conference paper
- Gordon, C.L., Lysecky, R. and Vahid, F., 2022. **Less Is More: Students Skim Lengthy Online Textbooks**. *IEEE Transactions on Education*. doi: 10.1109/TE.2022.3199651. paper link
- Gordon, C., Lysecky, R. and Vahid, F., 2022, August. **Programming learners struggle as much in Python as in C++ or Java**. In *2022 ASEE Annual Conference & Exposition*. paper
- Gordon, C., Vahid, F. and Lysecky, R., 2022, August. **Understanding and Promoting Earnest Completion in Online Textbooks**. In *2022 ASEE Annual Conference & Exposition*. paper

- Vahid, F. and May, D., 2022, August. **Auto-Awarding Points for Incremental Development in Programming Courses**. In *2022 ASEE Annual Conference & Exposition*. paper
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- Vahid, F., Givargis, T. and Miller, B., 2022, August. **RIOS: A Task Scheduler in Source Code for Teaching and Implementing Concurrent or Real-Time Software**. In *2022 ASEE Annual Conference & Exposition*. paper
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- Gordon, C., Lysecky, R. and Vahid, F., 2021, October. **The shift from static college textbooks to customizable content: A case study at zyBooks**. In *2021 IEEE Frontiers in Education Conference (FIE)* (pp. 1-7). IEEE. doi: 10.1109/FIE49875.2021.9637289. paper link
- Vahid, F., Lysecky, R., Miller, B.A. and Vanderbeek, L., 2021, July. **Coding Trails: Concise Representations of Student Behavior on Programming Tasks**. In *2021 ASEE Virtual Annual Conference Content Access*. doi: 10.18260/1-2--36802. paper
- Alzahrani, N. and Vahid, F., 2021, July. **Common Logic Errors for Programming Learners: A Three-Decade Literature Survey**. In *2021 ASEE Virtual Annual Conference Content Access*. doi: 10.18260/1-2--36814. paper
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- Zhang, C. and Vahid, F., 2003, June. **Cache configuration exploration on prototyping platforms**. In *14th IEEE International Workshop on Rapid Systems Prototyping, 2003. Proceedings.* (pp. 164-170). IEEE. doi: 10.1109/IWRSP.2003.1207044 pdf
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- Lysecky, R. and Vahid, F., 2003, June. **On-chip logic minimization**. In *Proceedings of the 40th annual Design Automation Conference* (pp. 334-337). doi: 10.1145/775832.775918 pdf
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  Summarizes UCR's successful 3-course sequence on embedded system design, based on the new ESD book (see above) that emphasizes a unified view of hardware and software.
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  Provides a technique for efficiently exploring the configuration space of a parameterized system-on-a-chip (SOC) architecture to find all Pareto-optimal configurations. These configurations represent the range of meaningful power and performance tradeoffs that are obtainable by adjusting parameter values for a fixed application mapped onto the SOC architecture. Our approach extensively prunes the potentially large configuration space by taking advantage of parameter dependencies. We have successfully incorporated our technique into the parameterized SOC tuning environment (Platune) and applied it to a number of applications.
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  Architectures with parameterizable cache and bus can support large tradeoffs

between performance and power. We provide simulation data showing the large tradeoffs by such an architecture for several applications, and demonstrating that the cache and bus should be configured simultaneously to find the optimal solutions. Furthermore, we describe analytical techniques for speeding up the cache/bus power and performance evaluation by several orders of magnitude over simulation, while maintaining sufficient accuracy with respect to simulation-based approaches.

- Vahid, F. and Gordon-Ross, A., 2001, August. **A self-optimizing embedded microprocessor using a loop table for low power**. In *Proceedings of the 2001 international symposium on low power electronics and design* (pp. 219-224). doi: 10.1145/383082.383138 pdf html slides
  Describes the architecture and methodology of an embedded microprocessor that can automatically tune itself to the particular application that will run. The particular tunable component described is a loop table, similar to a loop cache except that its contents never change after the most frequent loops are detected.
- Vahid, F. and Givargis, T., 2001. **Platform tuning for embedded systems design**. *Computer*, *34*(2), pp.112-114. doi: 10.1109/2.901171 pdf
  Provides an overview of the philosophy of our UCR Dalton Project, in particular, the idea of tuning a programmable system-on-a-chip architecture to the one application that it will eventually run forever.
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  Our earlier work for fast evaluation of power consumption of general cores in a system-on-a-chip described techniques that involved isolating high-level instructions of a core, measuring gate-level power consumption per instruction, and then annotating a system-level simulation model with the obtained data. In this work, we describe a method for speeding up the evaluation further, through the use of instruction traces and trace simulators for every core, not just microprocessor cores. Our method shows noticeable speedups at an acceptable loss of accuracy. We show that reducing trace sizes can speed up the method even further. The speedups allow for more extensive system-level power exploration and hence better optimization.
- Stitt, G., Vahid, F., Givargis, T. and Lysecky, R., 2000, November. **A first-step towards an architecture tuning methodology for low power**. In *Proceedings of the 2000 international conference on Compilers, architecture, and synthesis for embedded systems* (pp. 187-192). doi: 10.1145/354880.354906 pdf html slides

We describe an automated environment to assist a system-on-a-chip designer to tune a microprocessor core to a particular application program that will run on the microprocessor, and vice-versa, with the goal of reducing embedded system power consumption. We limit such tuning to modifications that do not change the microprocessor instruction set, thus avoiding the large costs that would come with such a change. Our tuning environment for the 8051 microcontroller is freely-available on the web.

- Givargis, T., Vahid, F. and Henkel, J., 2000, September. **Instruction-based System-level Power Evaluation of System-on-a-chip Peripheral Cores**. IEEE/ACM International Symposium on System Synthesis (ISSS), pp. 163-169. pdf slides
  We propose a new technique, suitable for a variety of cores like peripheral cores, that is the first to combine gate-level power data with a system-level simulation model written in C++ or Java. For that purpose, we investigated peripheral cores and decomposed their functionality into so-called instructions. Our technique addresses a core-based system design paradigm. We show that our technique is sufficiently accurate for making power-related system-level design decisions, and that its computation time is orders of magnitude smaller than lower-level simulation approaches.

- Lysecky, R.L., Vahid, F. and Givargis, T.D., 2000, September. **Experiments with the peripheral virtual component interface**. In *Proceedings 13th International Symposium on System Synthesis* (pp. 221-224). IEEE. doi: 10.1109/ISSS.2000.874053 pdf html slides
  The Peripheral Virtual Component Interface, or PVCI, is a standard intended to simplify the interfacing of peripheral cores to on-chip buses in a system-on-a-chip, by standardizing the interface between a core's internals and its bus wrapper. We provide results of experiments intended to determine the power, performance, and size overhead associated with using a PVCI bus wrapper versus using a non-PVCI bus wrapper, and versus using no bus wrapper at all. The results demonstrate that using a bus wrapper may result in only small performance, power and size overhead versus using no wrapper, though even that performance overhead can be reduced or eliminated using pre-fetching. The results also demonstrate that using a PVCI bus wrapper yields no significant additional power, performance or size overhead compared with a non-PVCI bus wrapper.

- Givargis, T. and Vahid, F., 2000, May. **Parameterized System Design.** IEEE/ACM International Workshop on Hardware/Software Codesign (CODES), pp. 98-102. pdf html
  Continued growth in chip capacity has led to new methodologies stressing reuse,

not only of pre-designed processing components, but even of entire pre-designed architectures. To be used across a variety of applications, such architectures must be heavily parameterized, so they can adapt to those applications' differing constraints by trading off power, performance and size. We describe several parameterized system design issues, and provide results showing how a single architecture with easily configurable parameters can support a wide range of tradeoffs.

- Givargis, T.D., Vahid, F. and Henkel, J., 2000, January. **Fast cache and bus power estimation for parameterized system-on-a-chip design**. In *Proceedings of the conference on Design, automation and test in Europe* (pp. 333-339). doi: 10.1145/343647.343791 pdf html slides
  We present a technique for fast estimation of the power consumed by the cache and bus sub-system of a parameterized system-on-a-chip design for a given application. The technique uses a two-step approach of first collecting intermediate data about an application using simulation, and then using equations to rapidly predict the performance and power consumption for each of thousands of possible configurations of system parameters, such as cache size and associativity and bus size and encoding. The estimations display good absolute as well as relative accuracy for various examples, and are obtained in dramatically less time than other techniques, making possible the future use of powerful search heuristics.
- Lysecky, R.L., Vahid, F. and Givargis, T.D., 2000, January. **Techniques for reducing read latency of core bus wrappers**. In *Proceedings of the conference on Design, automation and test in Europe* (pp. 84-91). doi: 10.1145/343647.343710 Best Paper Award. pdf html slides
  Today's system-on-a-chip designs consist of many cores. To enable cores to be easily integrated into different systems, many propose creating cores with their internal logic separated from their bus wrapper. This separation may introduce extra read latency. Pre-fetching register data into register copies in the bus wrapper can reduce or eliminate this extra latency. In this paper, we introduce a technique for automatically designing a pre-fetch unit that satisfies user-imposed register-access constraints. The technique benefits from mapping the pre-fetching problem to the well-known real-time process scheduling problem. We then extend the technique to allow user-specified register interdependencies, using a Petri Net model, resulting in even more efficient pre-fetch schedules.
- Givargis, T., Vahid, F. and Henkel, J., 2000, January. **A hybrid approach for core-based system-level power modeling**. In *Proceedings of the 2000 Asia and South Pacific Design Automation Conference* (pp. 141-146). doi: 10.1145/368434.368593 pdf html

Describes a technique for obtaining fast yet accurate power estimations of core-based systems. The main idea is to use an object-oriented language (C++ or Java) to create a system-level model , modeling each core as an object, and extending each object with power-estimation methods based on statistics from low-level power data of a synthesized version of the core. By executing the system-level model, which runs about 1000x faster than gate-level simulation, we obtain very accurate power estimates.

- Givargis, T.D., Henkel, J. and Vahid, F., 1999, November. **Interface and cache power exploration for core-based embedded system design**. In *1999 IEEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers (Cat. No. 99CH37051)* (pp. 270-273). IEEE. doi: 10.1109/ICCAD.1999.810660 pdf html
  Demonstrates, through experiments on four applications, the large power, performance and size tradeoffs possible just by varying architectural parameters relating to cache and bus for a given reference architecture. Illustrates that these parameters must be tuned to one another for each application, and thus argues for the need for a parameter exploration environment in a configure-and-execute design paradigm.
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  Introduces a method to reduce or eliminate the extra latency that may arise when reading from a core designed with a bus wrappers for ease of retargeting to different system buses. The method involves pre-fetching registers from the core's internals to registers added in the bus wrapper, akin to caching.
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  Provides an argument, supported by data obtained by various researchers, in favor of building systems-on-a-chip by configuring a pre-designed reference design already in silicon, rather than building systems by connecting large numbers of cores.
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Recent Results at UCR with Configurable Cache and Hw/Sw Partitioning -- given at Triscend Corp., September 2002.For publications supported by NSF awards: Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation. Back to Frank Vahid's home page