Geethanjali College of Engineering and Technology

Department of Electronics and Communication Engineering

Center of Excellence in VLSI

Events Conducted

S.No	Title	Category	Date and Time	Place
1.	Tech Pic	An Online Poster Presentation	August 6, 2021 - August 11, 2021	online
2.	Design and Verification Using Verilog	Workshop	September 13 to October 27 2021	online
3.	Latest Trends in ECE and the job opportunities in core area	Guest lecture	2nd November 2021 9:30 AM – 12:00 PM	online
4.	ARM MICROCONTROLLER	Guest lecture	3rd November 2021 11:00 AM – 12:30 PM	online
5.	Paper Pro	Paper presentation	23rd November 2021- 30th November 2021	online
6.	VLSI Design Flow	Guest lecture	29th November 2021 9:00 AM – 10:00 AM	online
7.	Open Source Tools in VLSI	Workshop	29th November 2021 10:00 AM – 3:30 PM	online
8.	Satvara Think-Quick 5.0	Online quiz competition	5 th December 2021 7:00 PM – 7:30 Pm	online
9.	How to select your final year project	Peer training	10th December 2021 6:30 PM – 7:30 PM	online
10.	Session by Alumni on “Benefits of IEEE Membership”	Webinar	11th December 2021 6:30 PM – 7:15 PM	online

11.	Session by Alumni on “Benefits of IEEE CAS Membership”	Webinar	11th December 2021 7:30 PM – 8:30 PM	online

Ms.G.SreeLakshmi
Co-cordinatorCoE-VLSI Design

Prof.O.V.P.R.Siva Kumar
Cordinator CoE-VLSI Design

Dr.S.Suryanarayana
Prof & HoD-ECE

Report of

“TECHPIC an online Poster Presentation competition”

Organized by IEEE CAS Student Branch Chapter-GCET

Dates: 6th August 2021 to 13th August 2022. Reopened from 15th September 2021 to 22nd september 2022

- No. of Student Registrations: 8
- No. of Student participants: 8
- Target Students: B.Tech II, III Yr and IV Yr Students
- No. of IEEE Student Member participants: 3
- No. of Non-IEEE Student Member participants: 5
- Registration Fee: Nil

Agenda: To promote a thorough conceptual understanding of Recent trends in circuits/systems/VLSI devices and its related areas

About Event:

IEEE Circuits and Systems Society Student Branch Chapter GCET organized "TECHPIC" an online Poster Presentation competition on circuits/systems/VLSI devices and its related areas. This was the online Poster Presentation competition conducted by IEEE CAS SBC GCET and the motto behind conducting this event is to promote a thorough conceptual understanding of Recent trends in circuits/systems/VLSI devices.

IEEE

CAB

IEEE Circuits ancf Systems *Society* Stczcfenr *Branch Chapter*
Geethozt,jo/i Co//ege of'Engineering ancf Techno/ogy

Presents

TECHPIC

-Poster presentation competition

Theme

ReCent trends in

- Circuits
- Systems
- VLSI devices

Open contest

6th August 2OZI tol3th August 2OZI

Register at: http: bt ly/Techpic

Deadline : \3th August2O21 O6:OO PM IST

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Participate Incl winexciting prizes

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IEEE

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/?e-opening

TECHPIC

-Poster presentation competition

Theme

Recent trends in

- Circuits
- Systems
- VLSI devices

Re-open contest

15th September 2DZI to 22nd September 20ZI

Register at: http: bt ly echpic

Deadline : 22nd September 2O21 O6:OO PM IST

§„g /ieee gcetsb

Participate Incl winexciting prizes

___ /IEEE-GCETSB

The winners of "TECHPIC" an online Poster Presentation competition are:

s.no	Name	College	Cash prize	poster
1	Kandula Vineela	Geetanjali College of Engineering and Technology	1500	K Vineela Poster - Vineela Reddy.pdf
2	S Guna Sindhuja	Geetanjali College of Engineering and Technology	1000	3DIC - Sindhuja Sharma.jpg
3	Tejaswi kilaru	Geetanjali College of Engineering and Technology	500	poster-18R11A0428 - Tejaswi Kilaru.pdf

Event Coordinators:

1. M. Keerthana (18R11A0432 : ECE-3A)
2. Y. Saketh (18R11A0446 : ECE-3A)
3. G.Akhila (18R11A0463 : ECE-3B)
4. G.Haasya (18R11A04A8 : ECE-3C)

Report prepared and drafted by:

M. Keerthana

Chair, IEEE SB GCET

Report of

“Entuple Technologies On-line Training Program”

Organized by IEEE CAS Student Branch Chapter-GCET

Dates: 13th September 2021 - 27th October (6-Week Training Program 4 hours per week)

- No. of Student Registrations: 120
- No. of Student participants: 49
- Target Students: B.Tech II and III Yr Students
- No. of IEEE Student Member participants: 17
- No. of Non-IEEE Student Member participants: 32
- Registration Fee: Nil

Agenda: To promote a thorough conceptual and practical understanding of VLSI Domain, Verilog HDL, and its related areas.

About Event:

IEEE Circuits and Systems Society Student Branch Chapter GCET organized "ENTUPLE TECHNOLGIES" an online training program on VLSI Domain, Verilog HDL, and its related areas. This was the online training about Digital Fundamentals conducted by IEEE CAS SBC GCET and the motto behind conducting this event is to promote a thorough conceptual and practical understanding of VLSI Domain, Verilog HDL. It was planned for 6 weeks from 18th September 2021 as 4 hours per week.

Finally, this traning course has ended successfully with a lot of informative and enlightening points.

Some Topics Covered in the Training Program:

- Verilog and design verification (part 1)
- Verilog and design verification (part 2)

 Operator precedence
 Ports in Verilog

- Digital Fundaments
- Gate level primitives
- Structural, data and Gate flow Model in Verilog HDL
- VLSI Ecosystem and Employment Opportunities
- VLSI Industry Segments
- VLSI Types (FPGA, ASIC, Analog)

Tentative Schedule for Entuple technologies:

Date	Time	Theory Session	Lab Session	Outcome
13th September	6:30 PM to 8:30 PM	Introduction to VLSI, ASIC and FPGA flow	Digital Fundamentals	Complete understanding of ASCI flow and FPGA flow
20th September	6:30 PM to 8:30 PM	Digital design stages, Verilog program structure, Verilog constructs	Verilog Syntax	Learning Verilog constructs
27th September	6:30 PM to 8:30 PM	Design of combinational circuits using Verilog	Assignment on combinational circuit design	combinational circuit design using Verilog
7th October	6:30 PM to 8:30 PM	Design of sequential circuits using Verilog, timing	Assignment on sequential circuit design	Sequential circuit design using Verilog
18th September	6:30 PM to 8:30 PM	Design of state machine, Introduction to Verification, Verification using Verilog, AMBA APB protocol, Low power techniques	APB based Memory design and verification, Designing finite state machine	Understanding modeling of a protocol state machine, Writing Test bench for a given design

27th October	6:30 PM to 8:30 PM	Description of the project	Development and Review	Final Project result

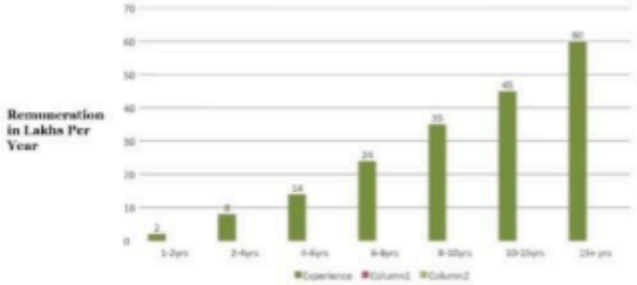
Please find the Certificates provided by the Entuple Technologies Pvt Ltd from the attached Google Drive Link: Click here

***Photos of the Session*:**

VLSI Career

- Good Semiconductor ecosystem in India – Significant no. of job opportunities here in India with good salaries

Experience vs Remuneration



NOTE:
Figures shown are only indicative. The industry is performance based and salaries can vary significantly from individual to individual.

Even Positions in organization is also can vary over years.

- Since most of the end customers are MNCs, Abroad opportunities are presented quite often.
- One can travel through H1 and L1 VISAs after acquiring minimum of 3 years experience.
- Onsite salaries could range from USD 70k-80k.
- Presents opportunity to become entrepreneurs

Share content

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What matters in VLSI?

Core	Cores/threads	Speed	Power
i9	10/20	3.7GHz	65/125W
i7	8/16	3.8GHz	65/125W
i5	6/12 (Cache 12MB)	4.1GHz	65/125W
i3	4/8 (Cache 6/8MB)	3.8GHz	65W

11

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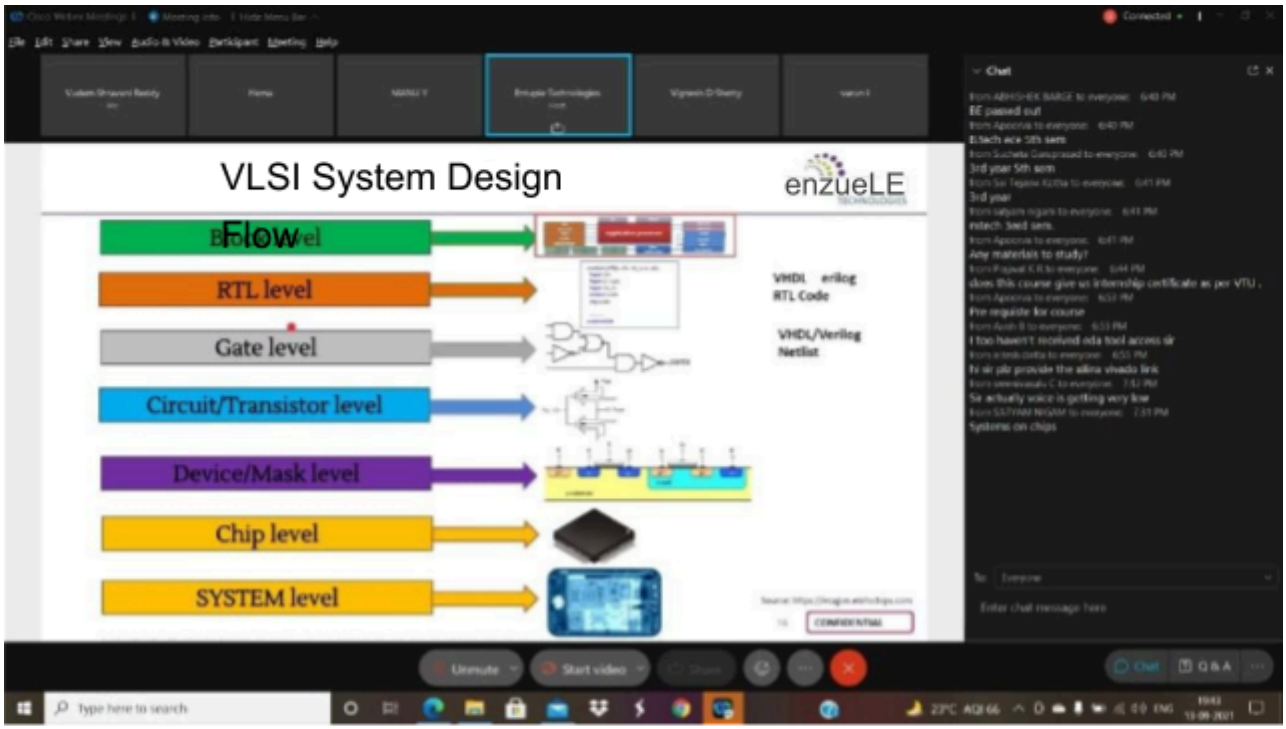
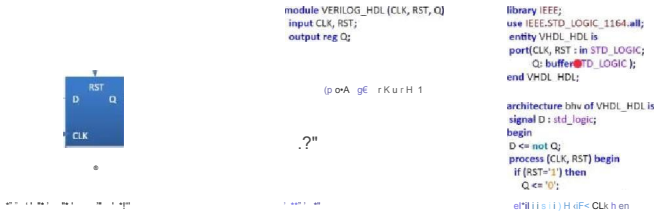


RTL Coding

en upLE

- Design is abouL mod eling a synchronous digit aI circuit is using Register Transfer Logic (RTL).
- Represents Flow of digital signals between hardware registers with certain logical operation
- Consists of two kind oh elemen Ls: registers (sequential) ano gates (comoinational)
- Languages used to implement RT—L VHDL and Verilog
- Tools for RTL simulations - IES (C ’°° °/„“^” ’” °‘/s) and "° °ı°°ı "’° ’°° Gra ohics)



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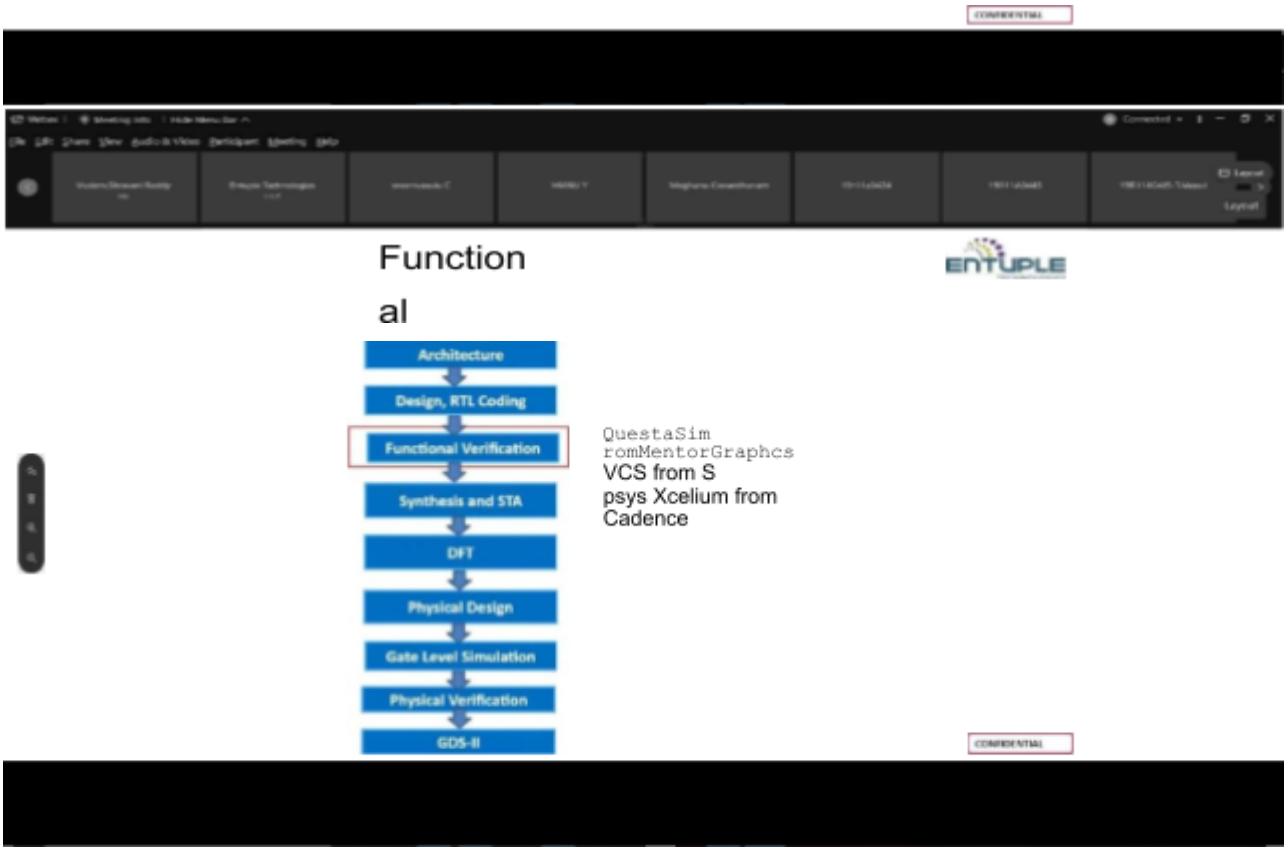
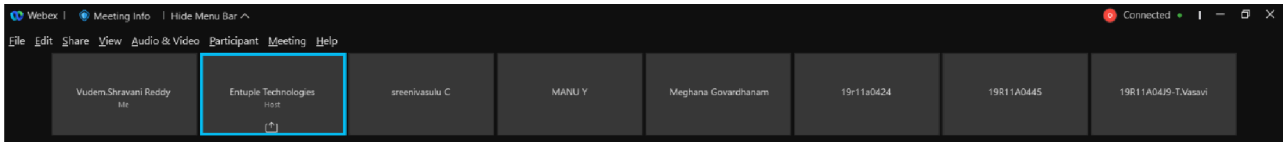
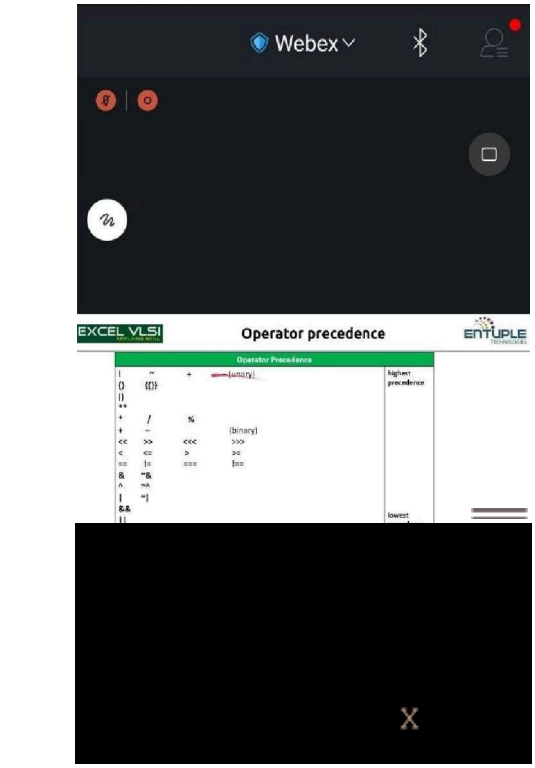
ASIC FLOW - FUNCTIONAL VERIFICATION

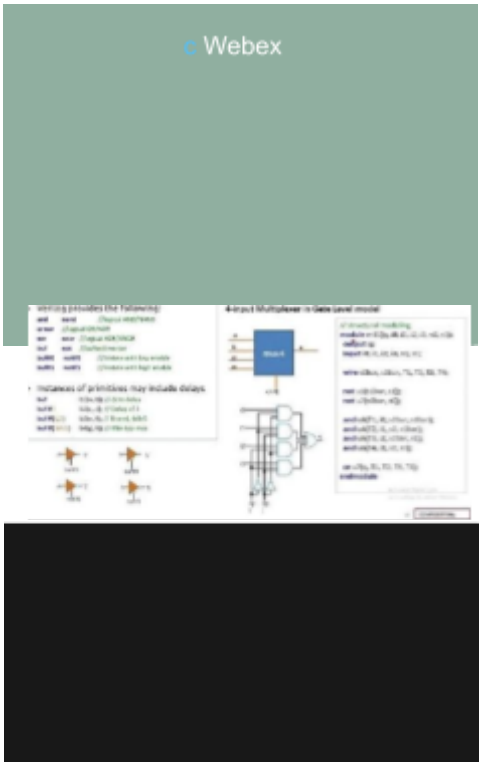


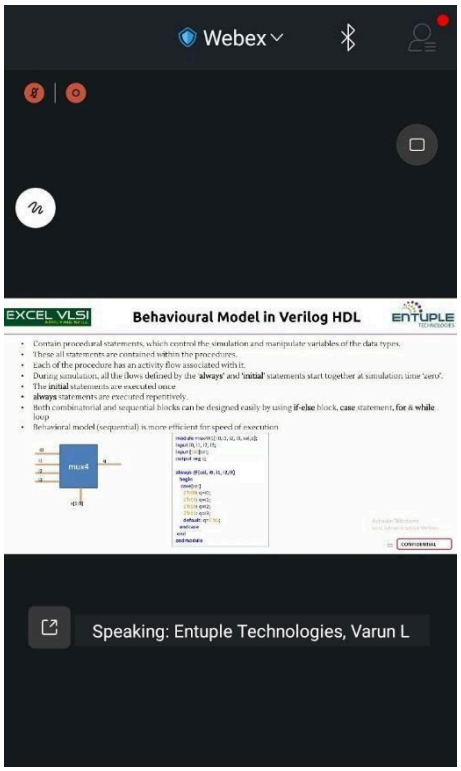


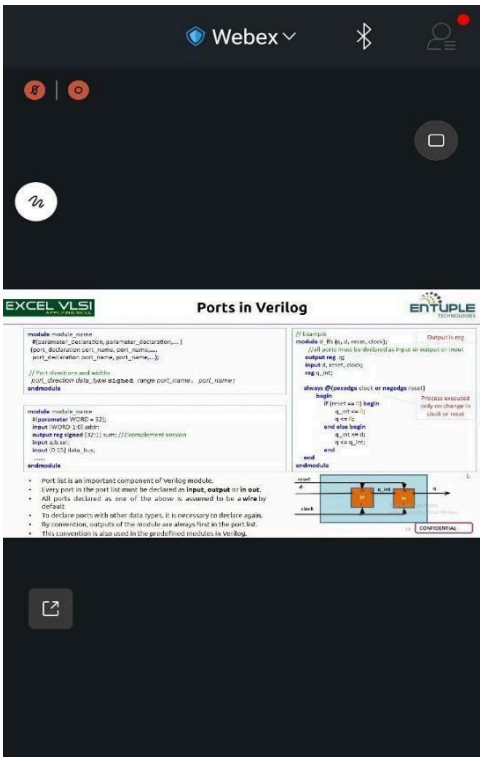
Verification

- Goal is to check the Design For the Correct FuncCionaliLy.
- Verification Process:
  - Test bench is to verify the Functionality oF a design
    A test bench is at the highest level in the hierarchy of the desig n.
    the test bench encapsulates the stimulus driver, known good resulLs, and DUT, and contains internal signals to make the proper connections.
    The stimulus ger§rator and driver drives inputs into the oUT.









Event Coordinators:

1. M. Keerthana (18R11A0432: ECE-4A)
2. Y. Saketh (18R11A0446: ECE-4A)
3. G.Akhila (18R11A0463: ECE-4B)
4. G.Haasya (18R11A04A8: ECE-4C)

Report prepared and drafted by:

M. Keerthana

Chair, IEEE SB GCET

Report on
Guest Lecture on
"LATEST TRENDS IN ECE AND THE JOB OPPURTUNITIES IN CORE AREA"

Organized under Under IEEE CAS GCET SBC

Date: 2nd November, 2021

Faculty Coordinator:

Mrs. G.Sreelakshmi, Associate Professor, Faculty Advisor,IEEE CAS GCET SBC,

Resource person:

Mr. Damodara Sambasiva, Business Head, Entuple Technologies Private Limited, Bangalore

Participants: III year I sem ECE students of all sections

Objectives:

- To highlight the opportunities available in core areas like VLSI, Embedded and IoT streams.
- Skills required for industry to grab opportunities.

Need of the Guest Lecture

- To bridge the gap between industry and academics, and at the same time to encourage students about the latest technologies and skills required by students to get into industry.
- To know about EDA tools used by industry.
- To motivate students to pursue their internships in various courses related to VLSI area and to take out mini and major projects in same area.
- To help students understand the flow of VLSI Design from scratch to tape off
- To encourage students to apply the concepts in writing programs and in building projects.
- To enlighten the students regarding the present day scenario and how to choose bright future.

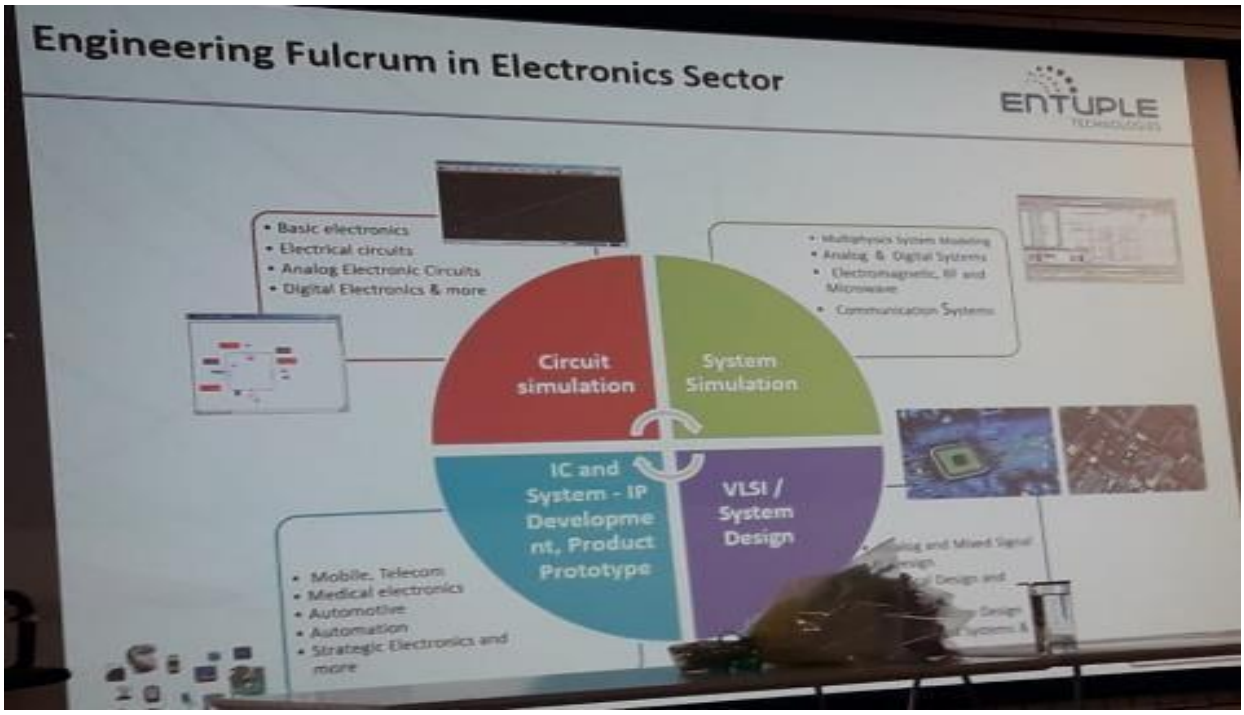
Report:

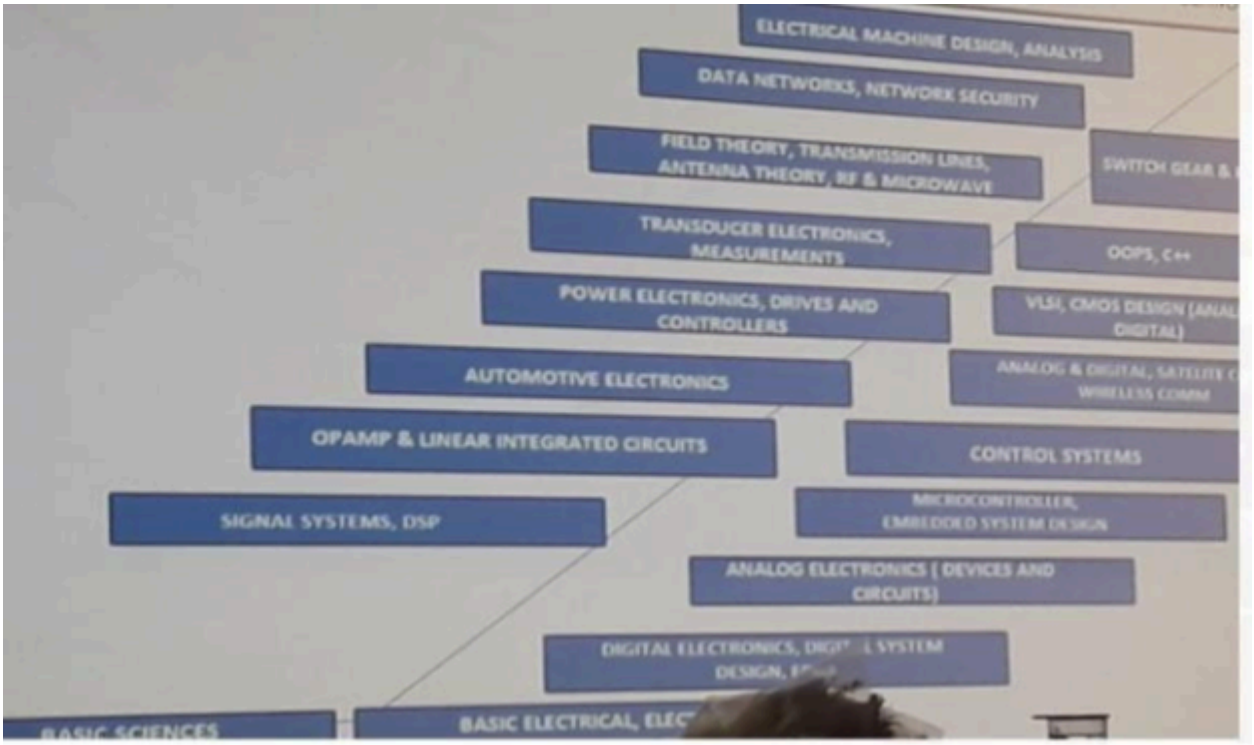
The session started at 11:00 AM by coordinator Ms. G.Sreelakshmi by welcoming the participants. Mrs. M.Laxmi, Associate Professor, invited guest speaker and Professor O.V.P.R.Sivakumar on to the dais with a bouquet. Professor Siva kumar addressed students about event in a few words. Later Ms. G.Sreelakshmi briefly introduced guest speaker Mr. Damodara Sambasiva, Business Head, Entuple Technologies Private Limited, Bangalore

Around 190 students participated in guest lecture from all sections of 3rd year and got benefited. Mr.Damodara clearly explained what industry is looking for and how to achieve those goals before completing final year B.Tech. He also explained various streams in VLSI domain and job

opportunities based on software, hardware and testing. He also suggested thinking on themselves

where they are strong and where they are weak and suggested to focus on strong side. As an example he quoted on that who are interested in coding they can choose career as “Verification Engineer” and if they are interested in circuits “Physical Design Engineers”, etc.,




ELECTRICAL MACHINE DESIGN, ANALYSIS
DATA NETWORKS, NETWORK SECURITY
FIELD THEORY, TRANSMISSION LINES, ANTENNA THEORY, RF & MICROWAVE
SWITCH GEAR &
TRANSDUCER ELECTRONICS, MEASUREMENTS
OOPS, C++
POWER ELECTRONICS, DRIVES AND CONTROLLERS
VLSI, CMOS DESIGN (ANAL
DIGITAL)
AUTOMOTIVE ELECTRONICS
ANALOG & DIGITAL, SATELLITE
WIRELESS COMM
OPAMP & LINEAR INTEGRATED CIRCUITS
CONTROL SYSTEMS
SIGNAL SYSTEMS, DSP
MICROCONTROLLER, EMBEDDED SYSTEM DESIGN
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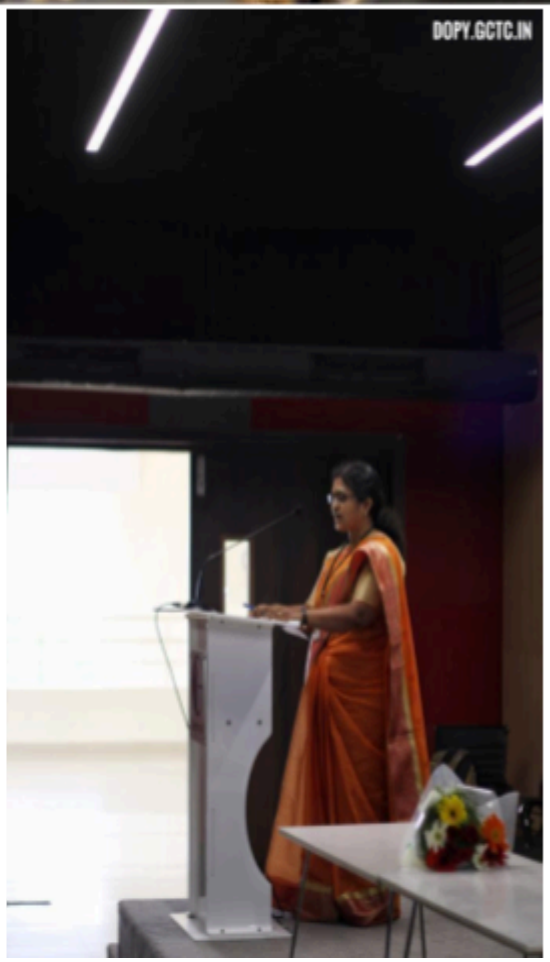
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ACADEMIC YEAR t021-22

ATTEA /Q&NCE SHEET Date:-18/11/2021

B.No.

	ROLL No.	NAME	SECTION SIGNATURE
1	19R11A0418	E. Thanuja	
2	19R11A0A16	D. Akhila	
3	19R11A04K8	B. Mani chandrika	
4	19R11A04J6	S. Jyothi	
5	19R11A04L5	D. Bhavya	
6	19R11A04L7	Ch. Tulasi	
7	19R11A04R2	V Sambitha	
8	19R11A0459	CH. Vineesha	
9	19R11A0456	C. Hemalatha	
	19R11A0465	G. Kusuma Clayton	
	19R11A0465	K. Abhinav	
	19R11A04H5	N. Pranay	
	19R11A04F9	G. Spandhan Reddy	
	19R11A04H6	P. Abhishek ex-CR	
15	19R11A04F1	C. Saya Vinshi	
	19R11A0409	C. Naga ranga Swamy	
	19R11A0415	K. Sravan Sravi	
18	1 435	P. Kameswara Bartham	
19	19R11A0436	P. Sai teja	
20	19R11A044J	ASIb Shaik Threy AL	
	19R11A04M8	K. Anil Kumar	
	19R11A04P3	S. Siddhartha	
	19R11A04N0	L. Lokesh Goud	
	19R11A04L9	G.S mohit	
	19R11A04N2	Deepak	
26	19R11A04P8	Vivek Naik	
	19R11A04E4	D. Rajesh Reddy	
	19R11A04J6	S.B. Prasad	
	20R15A0424	G. Vivek	
	19R11A04N6	M. Tousif	
	19R11A04J3	R. Uday Kiran	
	19R11A04J8	T. Rajesh	
	20R15A04A9	MD Adhil	
34	19R11A04K4	A. Sai Keerthana	
	20R15A04A8	K. Vinay kumar	
36	19R11A04H8	G. Vardhan	
	19R11A04F6	D. Naveen	
	19R11A04G2	K. Uday Reddy	
	19R11A04G4	S. Vamshi	
	19R11A04H9	Harsha KVK	
41	19R11A04G2	K. Harsha Vardhan	
42	19R11A04G0	G. Siva Krishna	
	19R11A04F2	Ch. Phaneendra	
43	19R11A04H3	M. Vasu Deva Raju	
44	19R11A04J0	P. Praneeth Kumar	

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SECTION

S.No.	ROLL No.	NAME		SIGNATURE
1	19R11A0476	M. Amulya	B	Amu
2	19R11A0460	Ch. Swetha Sree	B	Swe
3	19R11A0479	K. Jyoshna	B	Jyoshna
4	19 479	M. Kavya	B	Kavya
5	19R11A0405	R. Vani	C	Vani
6	19R11A04B1	G. Shirisha	C	Shirisha
7	20R11A0423	Y. Nivetha	C	Nivetha
8	20R11A0406	M. Sravani	C	Sravani
9	20R1 421	A. Sravani	C	Sravani
10	19R11A04A0	B. Harshini	C	Harshini
	19R11A04A5	Ch. Archana Roy	C	Archanaroy
11	19R11A04A7	Vasavi chetty	C	Vasavi
12	19R11A04H2	M. Shivani	D	Shivani
13	19R11A04J1	P. Kathyayani	D	Kathyayani
14	19R11A04H9	P. Sruthi	D	Sruthi
1	19R11A04H8	P. Poojasree	D	Pooja
16	19R11A04H7	P. Sreeharsha	D	Sreeharsha
17	19R11A04J2	R. Prerna	D	Prerna
18	19R11A04K2	Y. Praneetha	D	Praneetha
19	19R11A04G6	K. Divya	D	Divya
20	19R11A04G1	G. Tejovani	D	Tejovani
	19R11A04J9	T. Vasavi Sree Lakshmi	D	Vasavi
22	20R15A0416	Navya Sree	D	Navya
23	19R11A04J7	Sravani	D	Sravani
24	19R11A04E6	Harini	D	Harini
25	19R11A04E9	Ramya Sree	D	Ramya
26	19R11A04H4	Srija	D	Srija
27	19R11A04G3	Ashritha	D	Ashritha
20	19R11A04A2	Niharika	C	Niharika
28	19R11A04D4	Shashanka	C	Shashanka
30	19R11A04M7	K. B. Priyanka	E	Priya
31	19R11A04E9	Ramya Sree	D	Ramya
32	19R11A04H4	Srija Reddy	D	Sriya
33	19R11A04E6	B. Harini	D	Harini
34	19R11A04H0	M. Samhitha	D	Samhitha
35	19R11A04E5	B.R. Madhavi	D	B.R. Madhavi
36	20R15A0417	R. Vaishnavi	D	R. Vaishnavi
	19R11A04F7	E. Anitha	D	Anitha
38	19R11A04F0	Ch. Akshitha	D	
39				
40				

ACADEMIC YEAR 2021-22
ATTEANDAXICE SHEET
Date:-18/11/2021

S. No.	ROLL No.	NAME	SECTION	SIGNATURE
1	19R11A04C3	M. Sathwik Sai	C	
2	19R11A04B6	K. Sri Varun	C	
3	19R11A04C6	M. Sai Kiran	C	
4	19R11A0498	A. Karthikeya	C	
5	19R11A04	M. Vamshi	C	
6	19R11A04A8	D. Ajay	C	
7	1 B2	G. Nithin	C	
8	19R1 A04B7	K. Goverdhan	C	
9	19R11A04C2	Aditya	C	
10	19R1A04C1	Sarath	C	
-1	20R15A0412	Nanda Kishore	C	
12	20R15A0411	Nikhil	C	
13	20R15A0413	Chaitanya	C	
	20R15A0414	Samarth Raj	C	
t5	20R15A0415	Vinay Kumar	C	
1	19R11A04D9	Siddharth	C	
6	19R11A04C8	Arun Raj	C	
	19R11A04D3	Ganesh	C	
	20R15A0405	T. S V V. SRIRAM	A	
	20R15A04[illegible]	N. VISHNU	D	
19	19R11A0497	Sangoju Sriram chary	B	
20	19R11A0482	Noorbasha Salman Vali	B	
	19R11A04Z1	K. Pavan [illegible]	B	
22	19R11A0417	K. Salman raj 4	A	
23	19R11A0401	A. manikanta	A	
24	19R11A0404	B. kalyan Varma	A	
2S	19R11A0443	S. ajay kumar	A	
26	19R11A0444	S. visu9 tej 9	A	
27	19R11A04D0	Nishanth. P	C	
28	19R11A04C7	Tahalakheel	C	
	19R11A04C6	Dheraj	C	
30	19R11A04B4	Wilson. P	C	
31	19R11A04E3	Divya Rakesh Reddy	C	
32	19R11A04C4	Sathwik	C	
33	19R11A0489	Supriya	B	
34	19R11A0496	Anusha	B	
3S	19R11A04B3	Akshaya	B	
36	19R11A0453	Rachana	B	
37	19R11A0486	Hemanth	B	
38	19R11	Rakesh	B	
38	19R11A04K0	Naveen	B	
39			B	
42	1 11A0 1	Anish	B	
43	19R11A04E8	Manichandan	D	
44	19R11A04G7	Praneeth	B	
45	19R11A0493	Tanush	B	
46	19R11A0485	Deepak	A	
47	19R11A0409 15353640		E	
4NO	19R11A04N5.4E9.4N2.4M8.4P3.4P8			

S NO.	ROLL No.	NAME	SECTION	SIGNATURE
1	19R11A0427	Mukkamalla Srilatha	A	
2		Vaishnavi Yadav	A	
3	19R11A0419		A	
4				
5	19R11A0444	Y. Venkata Sravya	A	
6	19R11A0447	M. Bhavana	B	
7		K. Naithika Sree	B	
8	19R11A04A3	B. Sharmila	C	
9	19R11A0407	K. Sai Tejasvi	C	
10	9R11A04N8	R. Shailaja	C	
11	} qg\	P. Harika	E	
up q R S		S. Anusha	E	S. Anusha
13	19R11A04P0	S. Likhitha Reddy	E	
14	19R11A04P7	V. Sree Harsha	E	
15		Reddy	E	
16	19R11A04K6	A. Sai Keerthana	E	
17	20R15A0401	G Lampamalika	A	
18	20R15A0402	G. Sadhana	A	
19	20R15A0404	P Pavithra	A	
20	*##"°°	X.	A	
21	19R11A0414	[illegible]	A	
22	19R11A0429		A	
23	19R11A0403	B. Navya	A	
24	19R11A0418	K. Pavani	A	
25	19R11A0422	M. Rakesh	A	
26	19R11A0434	P. Bhavya Sai	A	
27	19R11A0404		A	
29	19R11A0481	M. Sai Sruthi	B	
30	19R11A04K5	A. Sathvika	E	
31	19R11A04M1	G. Anusree	E	
32	19R11A04B6	K Lahari	C	
33	19R11A04B8	G. Lahari	C	
34	19R11A04C9	Meghana	C	
35	19R11A0408	Shrutvi Singh	C	
36	19R11A04A8	Chandana	C	
37	19R11A04K2	A. Saanvari	E	
	>ee>iru•			
3	Nsh/»-o	b ilotn '	C	
40	19R11A04E3	V. Tanuja Sri	C	
s..	srn·i	F. [illegible]	C	
		a	C	Sandhya
			B	
42	11 04	Y. Janani	B	
43	19R11A0466	Harini	C	

ATTEANDANCE SHEET

Date:-18/11/ 202i

S. No	ROLL No.	NAIVIE	SECTION	SIGNATURE
1	19R11A04P5	S. Ranjith	E	
2	19R11A04N5	M. Srinivas	E	
3	19P11A04L1		E	
	19R11A04N3	M. Rupa	E	
6	19R11A04M4	K [illegible]	E	
7	19R11A0450	A. Sai Ishwar		
8	19R11A04A4	V. [illegible]		
9		V kaushik	B	
10	19R11A0487	Hemanth		
11	19R11A0458	Ramu		
12	19R11A0486	Srinivas	B	
13	19R11A0481		B	
	19E11A04G4	Aruntha Sai		
15	20R11A0410	Dinesh	eg	
16	20R15A0409	Akhil		
17	19K11A04B6	[illegible] Madhavi		
18	20R15A0417	R. vaishnavi		
19	19R11A0435	Bandeep		
20	19R11A0477	[illegible]	B	
21	19R11A0461	Pradeep		
22	19R11A0469	Akash		
23	19R11A04L7	D. Ramesh	B	
24	19R11A04L3		E	
25	19R11A04P4	S. Srikanth	E	
26	19R11A04N9	R Shiva	E	
27	19R11A04B5	K. [illegible]	E	
28	19R11A04A6	K-CH		
29	19R11A04B9	K. Manohar	C	
30	19R11A04A9	A. Sureesh		
31	19R11A04D2	P. Suman		
32	19R11A04K6	A. Sai Harsha	C	
	19R11A0408	C. Sai Trisha		
3	19R11A0445	T. Rohith Chandra	A	
35	19R11A0420	[illegible]		
36	19R11A0437	P. Karan Kalyan	A	
37	19R11A0413	G. Venu Madhav		
38	19R11A0407	B. Karan	A	
39	19R11A0441	S. Rohith	A	
40	19R11A0438	Varun Varma	A	

Phone : 9182058187
Website: www.geethanjaliinstitutions.com
info@gcet.edu.in

Geethanjali

Geethanjali College of Engineering and Technology

AUTONOMOUS

(Accredited by NAAC "A" Grade; ECE, CSE, EEE & ME, B.Tech Programs Accredited by NBA;
Approved by AICTE, New Delhi; Permanently Affiliated to JNTUH)
Sy. No. 33 & 34, Cheeryal (V), Keesara (M), Medchal District. - 501 301.

18th November, 2021

To

Mr. Damodara Sambasiva,
Business Head,
Entuple Technologies Private Limited,
Bengaluru.

LETTER OF APPRECIATION

Dear Sir,

Thank you very much for delivering an informative and thought provoking lecture as guest speaker on **"Latest Trends in ECE and job opportunities in Core Areas"**, to III year B.Tech ECE students at Geethanjali College of Engineering and Technology, Hyderabad on 18th November, 2021.

It was really a splendid session which exposed students to actively think of pursuing a career in ECE core areas. Your motivating views on becoming members of IEEE and contributing towards societal development are indeed very valuable to the student community. All the students got immensely benefited by your lecture.

On behalf of Department of ECE, Geethanjali College of Engineering and Technology, we thank you earnestly for spending your valuable time to motivate our students through your expert talk and we look forward to continued association with you for the benefit of faculty members and the students.

Prof. OVPR Siva Kumar,

Professor & Head Group-V

S. Suryanarayana

Dr.S.Suryanarayana,

Professor & HOD, ECE

HEAD
Dept. of Electronics & Communication Engg.
Geetanjali College of Engg. and Tech.
Cheeryal (V)., Keesara (M)., M.M Dist-501 301.

Feedback Analysis:

67 responses

Not accepting responses

Message for respondents

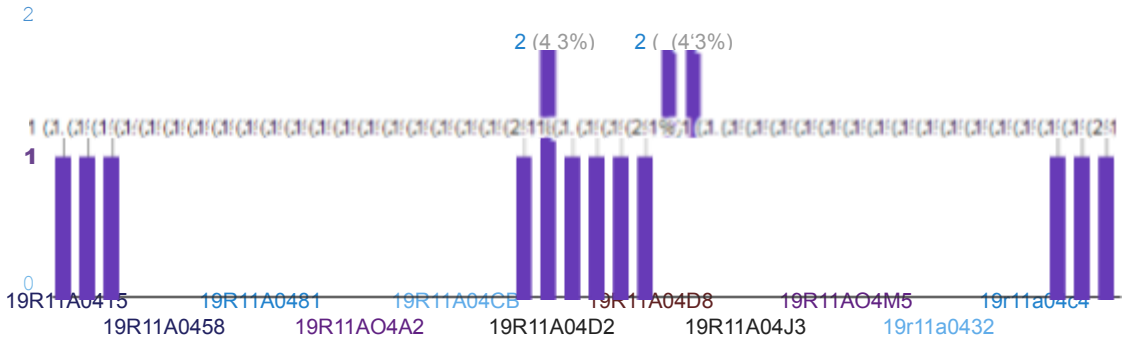
This form is no longer accepting responses

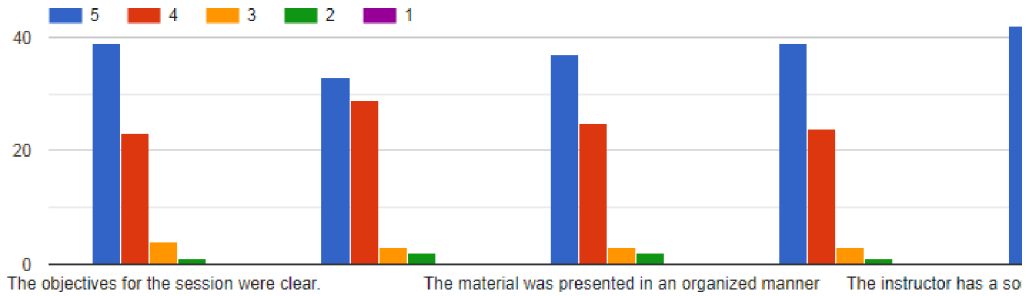
Summary Ouestion Individual

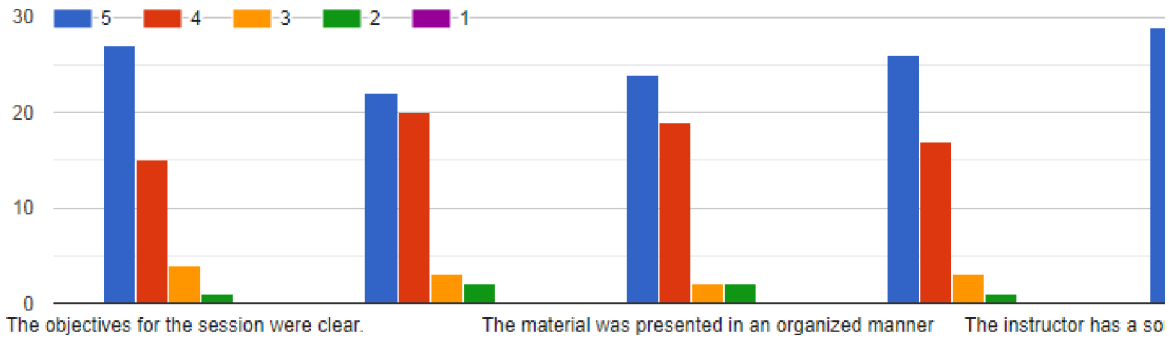
Session : 18th November, 2O21 (1O:OOAM to 12:3OPM), Topic Title: “Latest Trends in EC E and the opportunities in Core Area" , Resource Person: Mr. Damodara Sambasiva, Business Head, Entuple Technologies Private Limited, Bengaluru, India

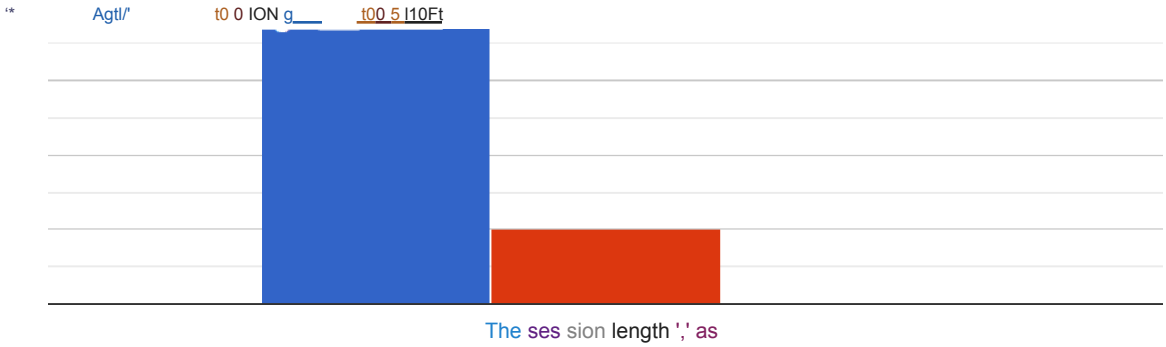
Roll. No.

47responses









What dick you most appreciate/enjoy/think was best about the session?

sv" re sponsee

iu u

Practic ie knowledge and various kinds of jobs available in eve Way

of teachincg

To know that even core area has many i» i»ort unities

The lecture was good

T he c ont ents s ir ha s exp laine d a re very interes1i ng

Topic s relate d gates and cocl ing th em in x il inx Very

interactive and intresting sess ion

Importance of core obs

Any suggestions for improvement?

39 responses

Noo
Clarity in screen presentation
None
Ntg
Nothing
.
Nothing!
nothing
Everything

Ms.G.Sreelakshmi	Prof. O.V.P.R.Sivakumar	Dr. S.Suryanarayana	Prof. B.Harikumar
Coordinator, ECE	Professor and Group V	Professor and HOD	Dean, SE&CE

Report of Guest Lecture on
"ARM MICROCONTROLLERS"

Organized by IEEE CAS Student Branch Chapter-GCET

Date: 3nd November, 2021

- No. of Student Registrations: 120
- No. of Student participants: 120
- Target Students: III year I sem ECE students and IV year I sem EEE students.
- Registration Fee: Nil
- Resource person: Dr. Santanu Chattapadyay, Professor, Department of EEE, IIT Kharagpur.

Objectives:

- Understanding the various concepts of Microcontrollers along with its Architecture. in the importance of 'ARM Microcontroller architecture'
- Knowing the importance of 'ARM Microcontroller architecture, instruction set and concepts of pipeline in the field of embedded systems.

Need of the Guest Lecture:

- To present an over view of theoretical and programming concepts related to ARM Microcontrollers which will be beneficial to students to start writing programs and to take up mini and major projects.
- To motivate students to pursue the course "Microprocessors and Microcontrollers" with a perspective of practical applications.
- To help students understand the importance of microcontrollers To encourage students to apply the concepts in writing programs and in building projects. To enlighten the students regarding the present day scenario and how powerful ARM processors are in industry.

Report:

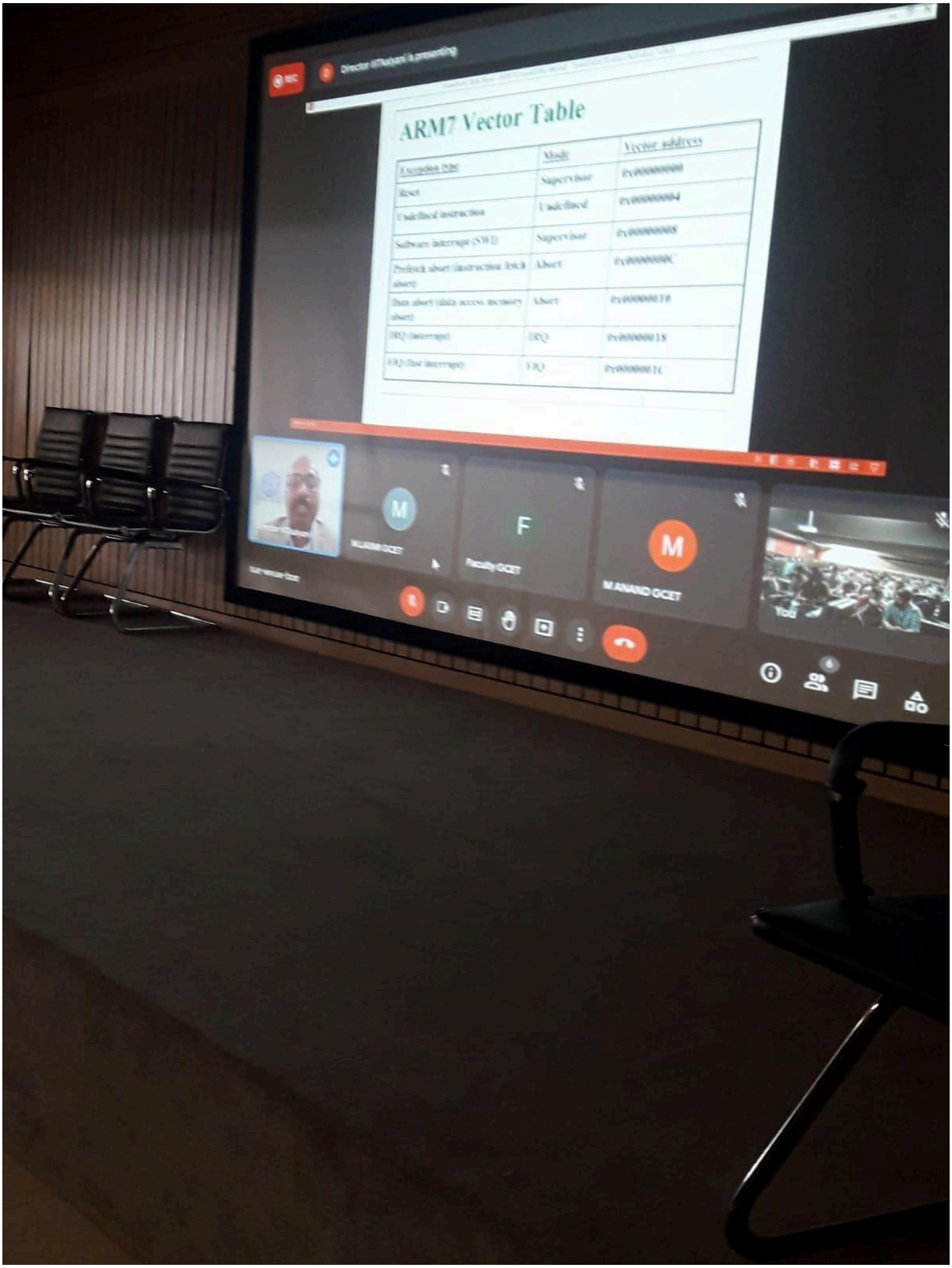
The session started at 11:00 AM by course coordinator Ms. G.Sreelakshmi by welcoming the guest speaker and participants. Later she introduced guest speaker Dr.Santanu Chattapadyay, Professor, IIT Kharagpur. Around 120 students participated in guest lecture from all sections of 3 year and got benefited. The resource person clearly explained about importance of microcontrollers and role of ARM microcontrollers and how it is different from other microcontrollers.

In his talk he highlighted few points about ARM Architecture.

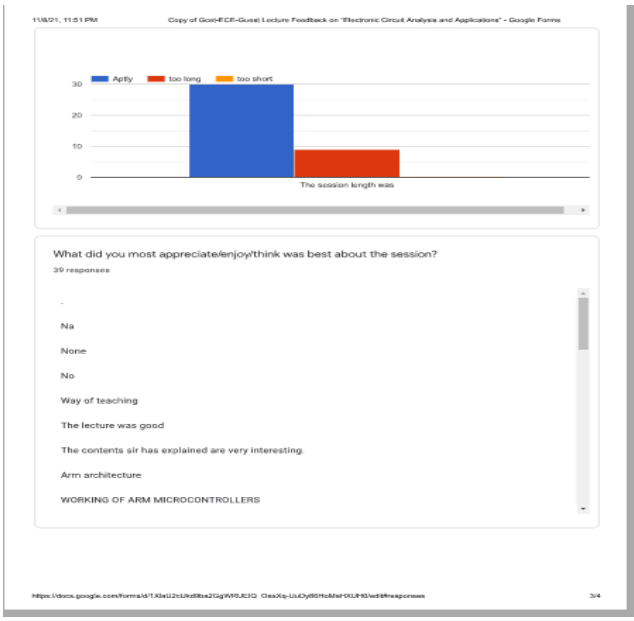
- . Register dominated Architecture
- ARM consists of Barrel shifter
- Which stage pipeline is suggested and structure of ARM pipeline
- ARM pipeline fetch, decode and execution and how Execute stage is split into 3 stages
- JTAG provision
- Instruction Memory and Data memory
- How to avoid data dependencies

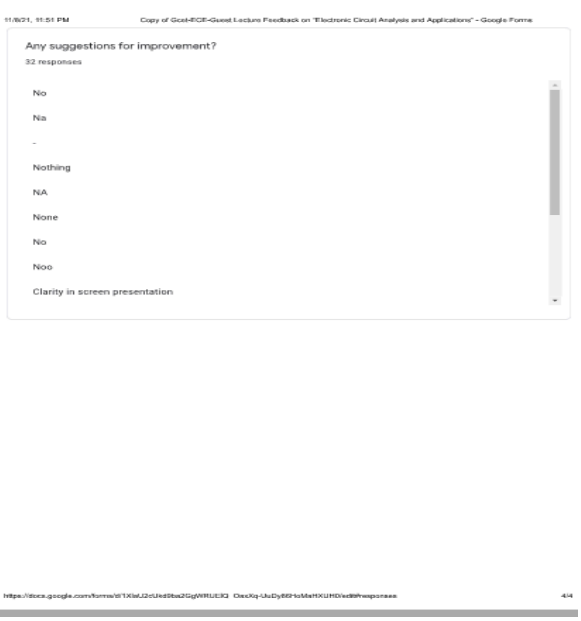
- Multiply Accumulate Instructions help for signal processing applications.
- Multiple load/store instructions
- Current program status registers
- Nested subprogram issue is solved used stack, Link reg.
- Modes of operation: System mode, user mode, irq, Supervisor mode and Fast Interrupt Queue (FIQ).
- THUMB instruction set
- Little Endian and Big-Endian format.
- Auto implement structures
- STMFD stored multiple Full Descending
- MULA

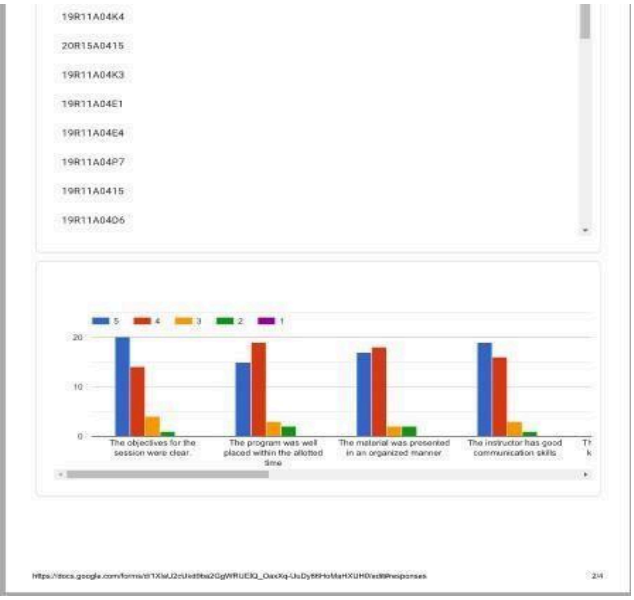
Event Photos:


Director Bhavani is presenting
ARM7 Vector Table
Mode
Vector address
Supervisor
Undefined
Supervisor
Abort
Abort
IRQ
FIQ
M.ANAND GCET
You

Event Feed Back:







Report of

"PAPER PRO an online Paper Presentation competition"

Organized by IEEE CAS Student Branch Chapter-GCET

Dates: 23rd November to 30th November

- *No. of Student Registrations: 7*
- *No. of Student participants: 7*
- *Target Students: B.Tech II, III Yr and IV Yr Students*
- *No. of IEEE Student Member participants: 3*
- *No. of Non-IEEE Student Member participants: 4*
- *Registration Fee: Nil*

Agenda: To promote a thorough conceptual understanding of Recent trends in Electronics

About Event:

IEEE Circuits and Systems Society Student Branch Chapter GCET organized "PAPER PRO" an online Paper Presentation competition on Recent trends in Electronics. This was the online Paper Presentation competition conducted by IEEE CAS SBC GCET and the motto behind conducting this event is to promote a thorough conceptual understanding of Recent trends in electronics .

The winners of "TECHPIC" an online Poster Presentation competition are:

s.no	Name	College	Cash prize	poster
1	Kandula Vineela	Geetanjali College of Engineering and Technology	1500	WIRELESS CHARGING - 18R11A0425 KANDULA VINEELA.docx

Event Coordinators:

1. M. Keerthana (18R11A0432 : ECE-3A)
2. Y. Saketh (18R11A0446 : ECE-3A)
3. G.Akhila (18R11A0463 : ECE-3B)
4. G.Haasya (18R11A04A8 : ECE-3C)

Report prepared and drafted by:

M. Keerthana

Chair, IEEE SB GCET

Report on

Guest lecture on "VLSI Design Flow"

Date: 29/11/2021

Department of ECE IEEE_CAS has organized a guest lecture on **"VLSI Design flow"** on *29th November, 2021* for the students who are interested in the core area of ECE Department.

Faculty Coordinator:

Ms. G. Sree Lakshmi, Faculty Advisor IEEE CAS GCET SBC.

Resource person:

Mr. K.Prashanth (Alumni GCET), Trained in Verilog HDL and System Verilog from industry

The main objective of this guest lecture is to motivate students to get into the core area with the inspiration of their senior students.

Session started by introducing K. Prashanth to students. He started the session with differences between combinational and sequential circuits, importance of latch, flip-flops, how to build concepts from small design to large design. As an example D-FF, 4-bit counter, counting a given sequence, mod N counters, designing of seconds, minutes and Hrs in a clock. During his session he also explained about Blocking and Non-Blocking Assign statements.

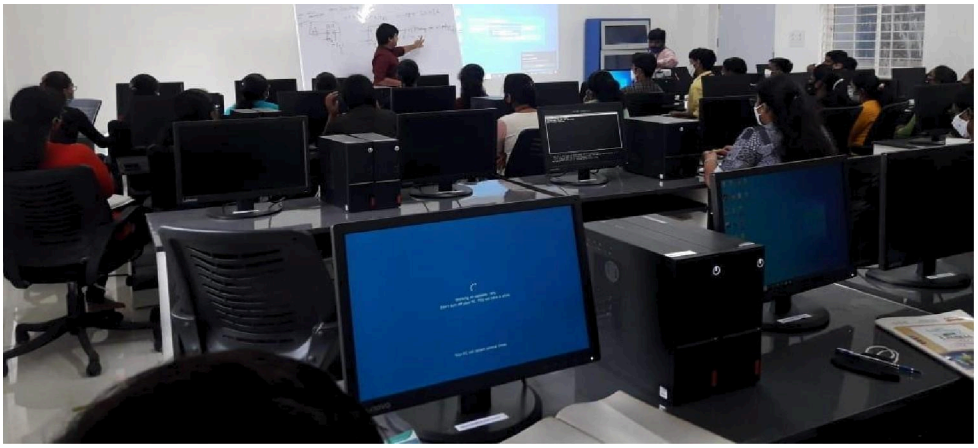
He also explained the concept how to generate numbers based on place value and how to start analyzing a given statement. He stressed that most important combinational blocks are Vectored mux, Vectored Adder and Vectored Comparator where any combinational circuit can be designed using only these three basic circuits.

Geethanjali college of
En$gi see rinjg ancl Tech nolojg

Theme VLSI DESIGN FLOW

$t„,tg /ieee_g cetslo

/IEEE-GCETSB



Report on

One day workshop on “Open Source Tools in VLSI”

Date: 29/11/2021

Department of ECE under IEEE CAS GCET SBC has organized a one day workshop on **“Sequential circuits ”** on *29th November, 2021* for the students who are interested in the core area of ECE Department.

Faculty Coordinator:

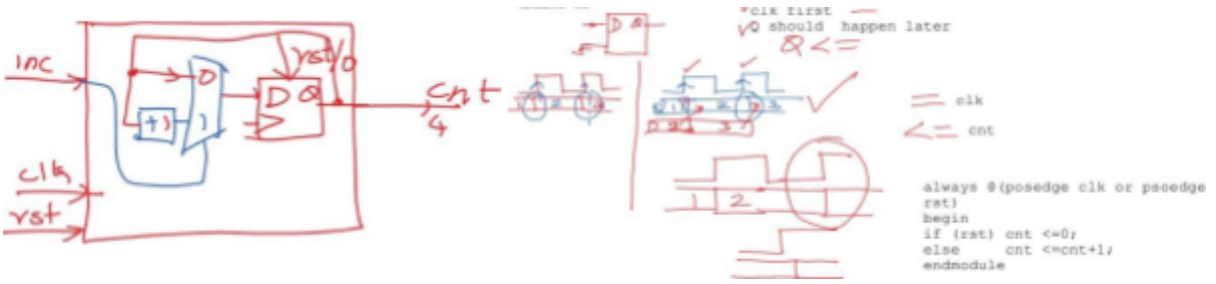
Ms. G. Sree Lakshmi, Faculty Advisor IEEE CAS GCET SBC

Resource person:

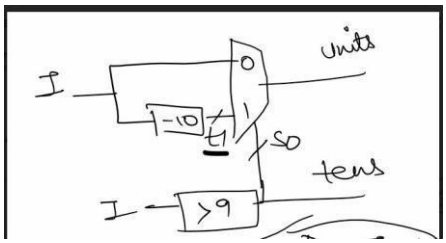
Mr. K.Prashanth (Alumni GCET), Trained in Verilog HDL and System Verilog from industry

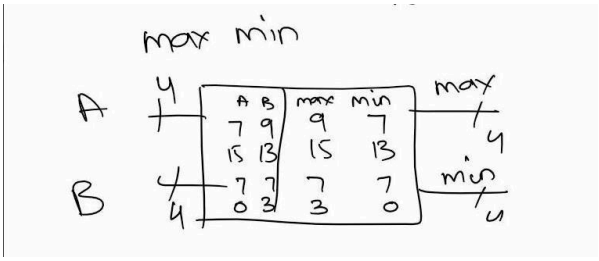
The main objective of this workshop is to motivate students to get into the core area with the inspiration of their senior students.

Session started by introducing K. Prashanth to students. He started the session with differences between combinational and sequential circuits, importance of latch, flip-flops, how to build concepts from small design to large design. As an example D-FF, 4-bit counter, counting a given sequence, mod N counters, designing of seconds, minutes and Hrs in a clock. During his session he also explained about Blocking and Non-Blocking Assign statements. Session went upto 12:30 PM and in the afternoon session they practiced on Modelsim software.

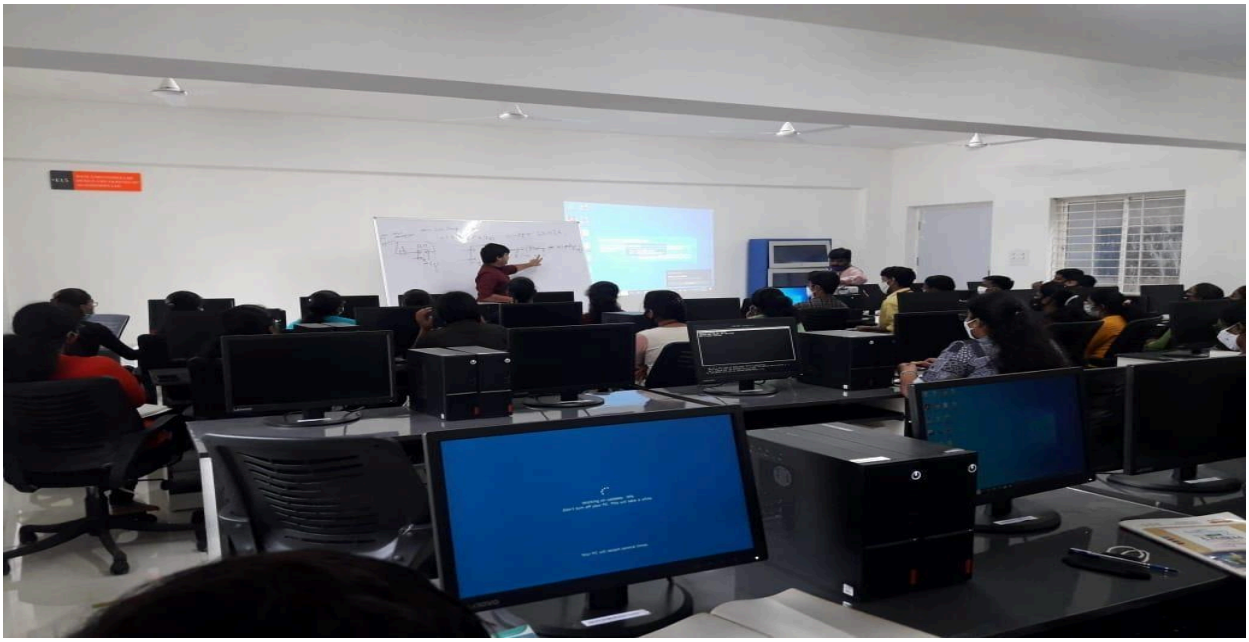


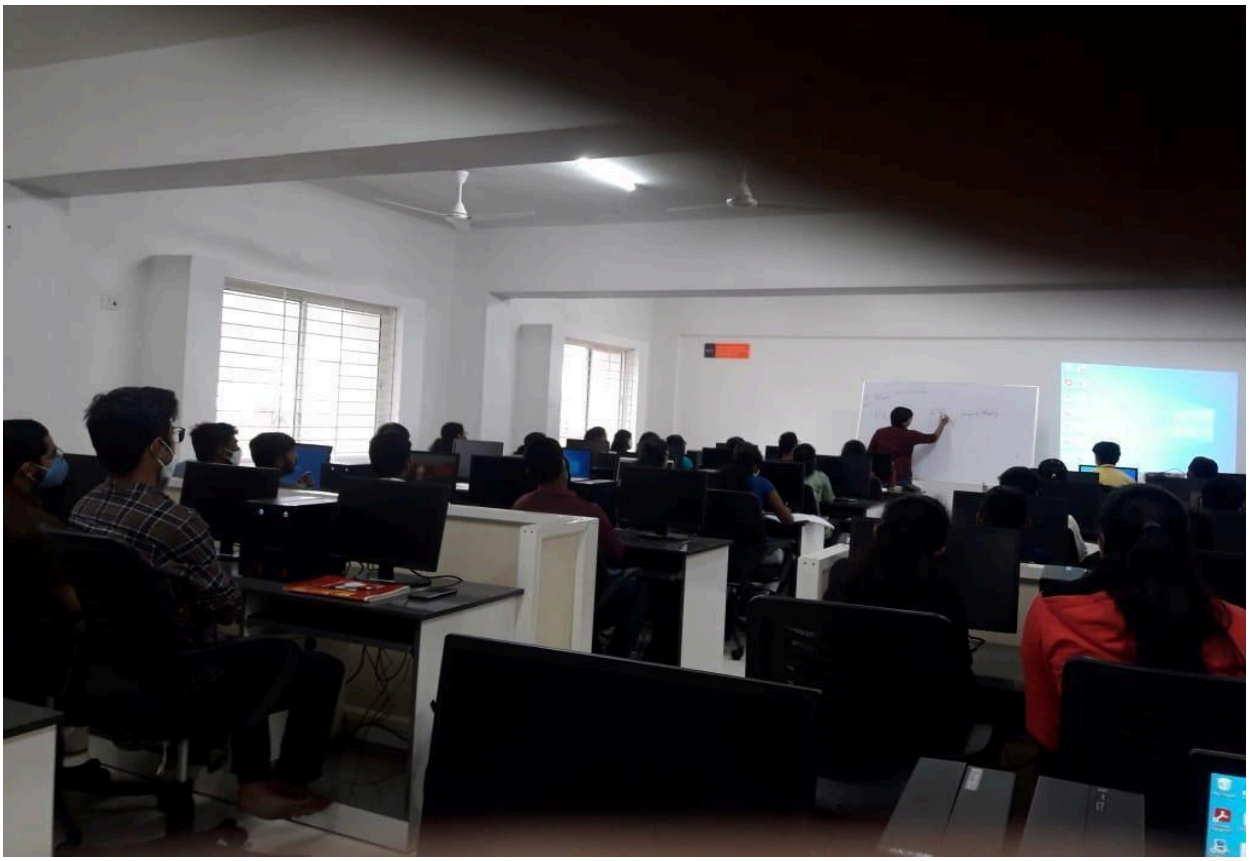
He also explained the concept how to generate numbers based on place value and how to start analyzing a given statement.

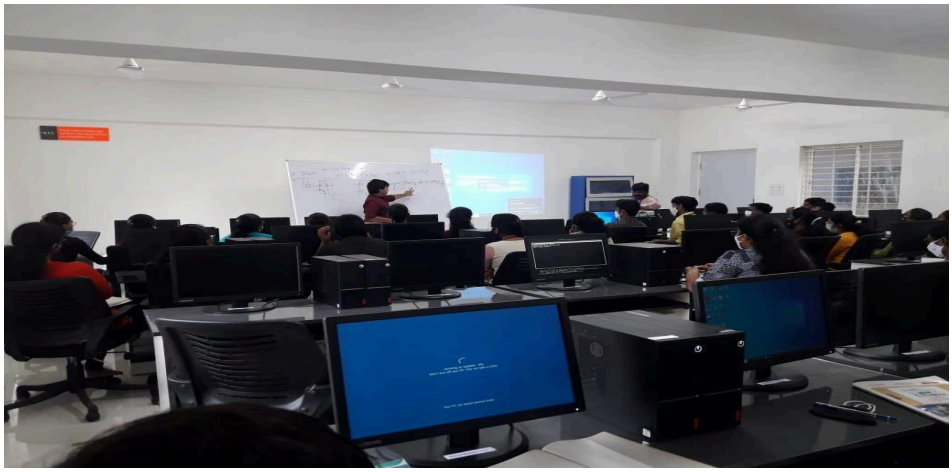




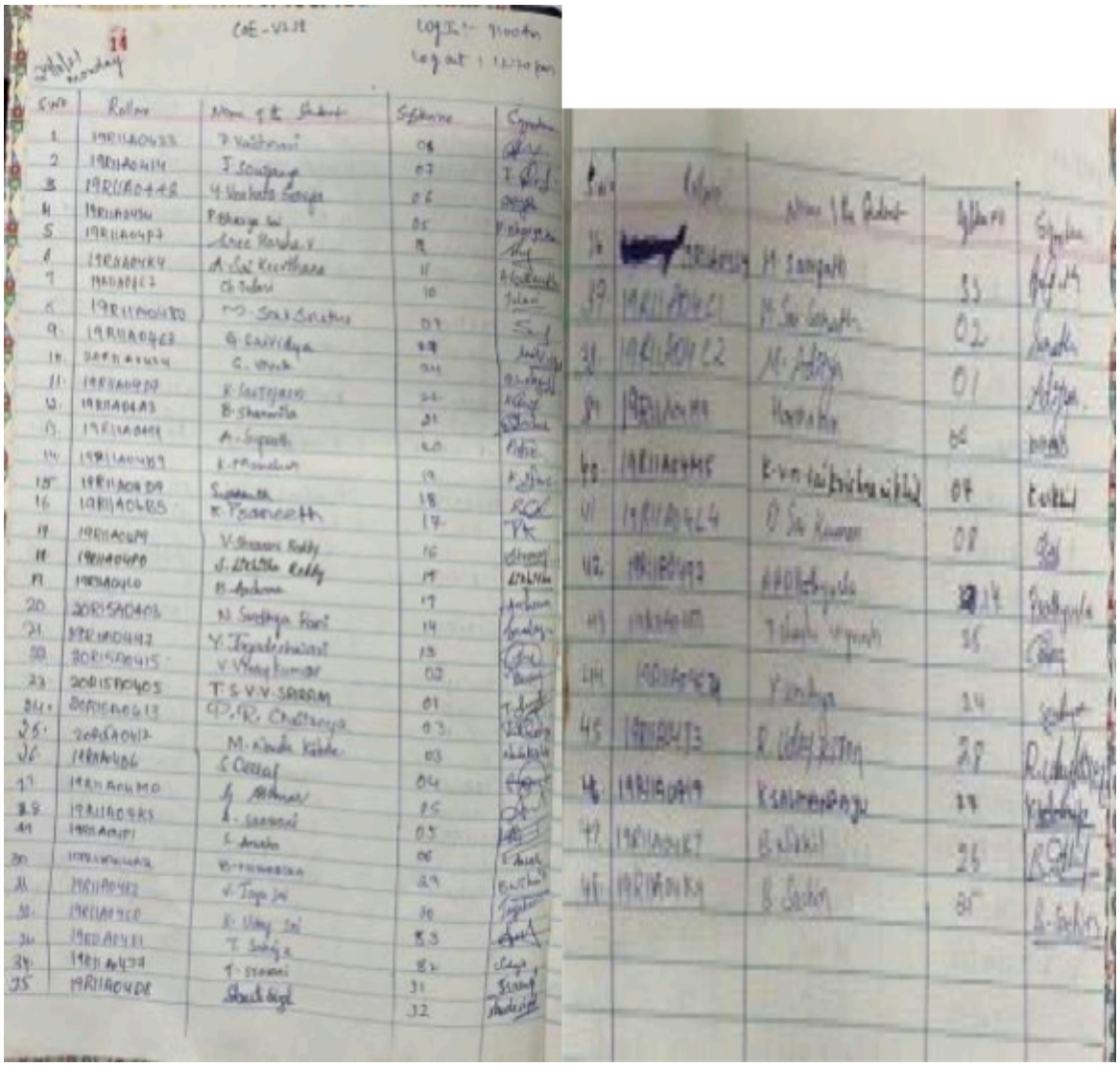
He stressed that most important combinational blocks are Vectored mux, Vectored Adder and Vectored Comparator where any combinational circuit can be designed using only these three basic circuits.







Attendance statement:



Total No. of students Attended :48

Feedback Analysis Report

The feedback was received from the participants and the summary is as follows.

1. The workshop was applicable to my area of interest:
- 80% Strongly Agreed.
- 10% Agreed to large extent
- 10% Agreed

2. The program was well paced within the allotted time
- 70% Strongly Agreed.
- 20% Agreed to large extent
- 10% Agreed

3. The material was presented in an organized manner
- 80% Strongly Agreed.
- 20% Agreed to large extent

4. The instructors were good communicators
- 80% Strongly Agreed.
- 20% Agreed to large extent

5. The instructors were knowledgeable on the topics
- 80% Strongly Agreed.
- 20% Agreed to large extent

6. The workshop improved my understanding of the topics
- 70% Strongly Agreed.
- 30% Agreed to large extent

7. I understood the concepts presented in the workshop
- 70% Strongly Agreed.
- 30% Agreed to large extent

8. The knowledge and skills I learned will be useful to me in my professional career.
- 80% Strongly Agreed.

 20% Agreed to large extent

9. I would attend other workshops offered by these Facilitators in future

 80% Strongly Agreed.

 20% Agreed to large extent

10. What did you most appreciate/enjoy/think best about the course?

✔ Way of building concept from latch, flip-flop, counter to application

✔ Building logic and how to start

✔ Easy to understand and write the code.

11. Any suggestions for improvement?

 More number of days required

48 students benefited from this workshop and most of them strongly decided to do job in VLSI core area.

Ms.G.Sreelakshmi	Prof.OV.P.R.Sivakumar	Dr.S.Suryanarayana	Prof.B.Harikumar
Faculty Advisor, IEEE_CAS	Advisor, IEEE_CAS	Professor & HOD	Professor, Dean SE&CE

Report of

“Satvara Think-Quick 5 .0 On-line Quiz Competition”

Organized by IEEE CAS Student Branch Chapter-GCET

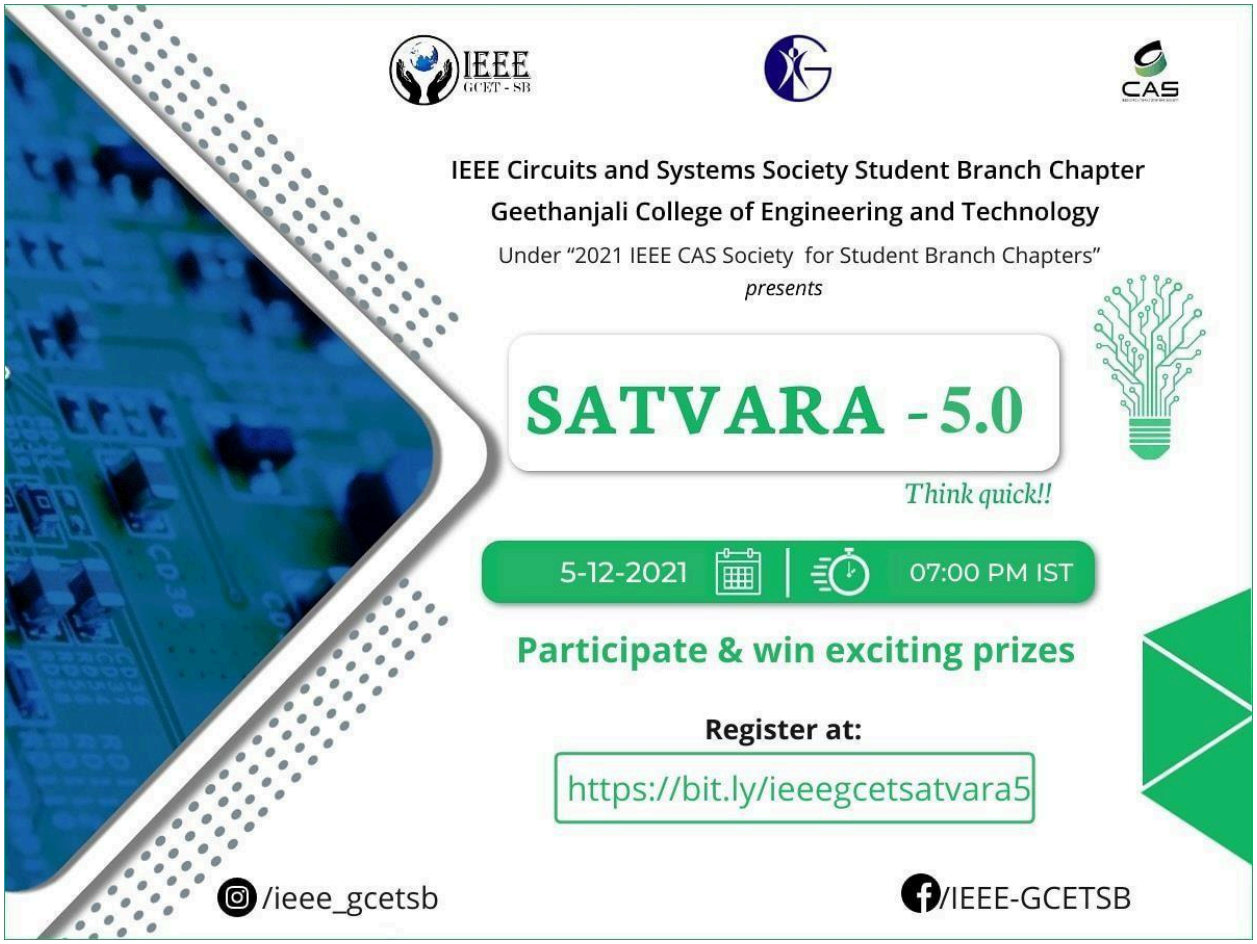
Dates: 5th December 2021. From 07:00 PM To 07:30 PM

- No. of Student Registrations: 116
- No. of Student participants: 93
- Target Students: B.Tech II and III Yr Students of Geethanjali college
- No. of IEEE Student Member participants: 16
- No. of Non-IEEE Student Member participants: 77
- Registration Fee: Nil

Agenda: To promote a thorough conceptual understanding of Digital Electronics and its related areas

About Event:

IEEE Circuits and Systems Society Student Branch Chapter GCET organized "SATVARA-Think quick!! 5.0" an online quiz competition on digital electronics and its related areas. This was the online quiz competition conducted by IEEE CAS SBC GCET and the motto behind conducting this event is to promote a thorough conceptual understanding of digital electronics. It consisted of 20 questions related to digital electronics.



The winners of SATVARA-Think quick!! 4.0 Online Quiz competition are:

s.no	Name	Percentage	College	Prize
1	CHAMAKURA SUSHANT KUMAR	75%	GCET	IEEE CAS MEMBERSHIP

	REDDY			
2	Anusha Samala	70%	GCET	IEEE CAS MEMBERSHIP
3	P.Bhavya Sai	65%	GCET	IEEE CAS MEMBERSHIP
4	Mangolu Vandana devi	65%	GCET	IEEE CAS MEMBERSHIP
5	Boda Niharika	65%	GCET	IEEE CAS MEMBERSHIP

The winners of satvara 5.0 were awarded with IEEE CAS memberships sponsored from our college

Event Coordinators:

1. M. Keerthana (18R11A0432: ECE4A)
2. Y. Saketh (18R11A0446: ECE-4A)
3. G.Akhila (18R11A0463: ECE-4B)
4. G.Haasya (18R11A04A8: ECE-4C)

Report prepared and drafted by:

M. Keerthana

Chair, IEEE SB GCET

Report of Webinar on

“How to select your final year project”

Organized by IEEE CAS Student Branch Chapter-GCET

Dates: 10th December 2021. From 6:30 PM To 7:30 PM

- No. of Student Registrations: 30
- No. of Student participants: 22
- Target Students: B.Tech II and III Yr Students of GCET
- Registration Fee: Nil
- Speakers: Haasya Godavarthy, 4th year ECE, Geethanjali College of Engineering and Technology.

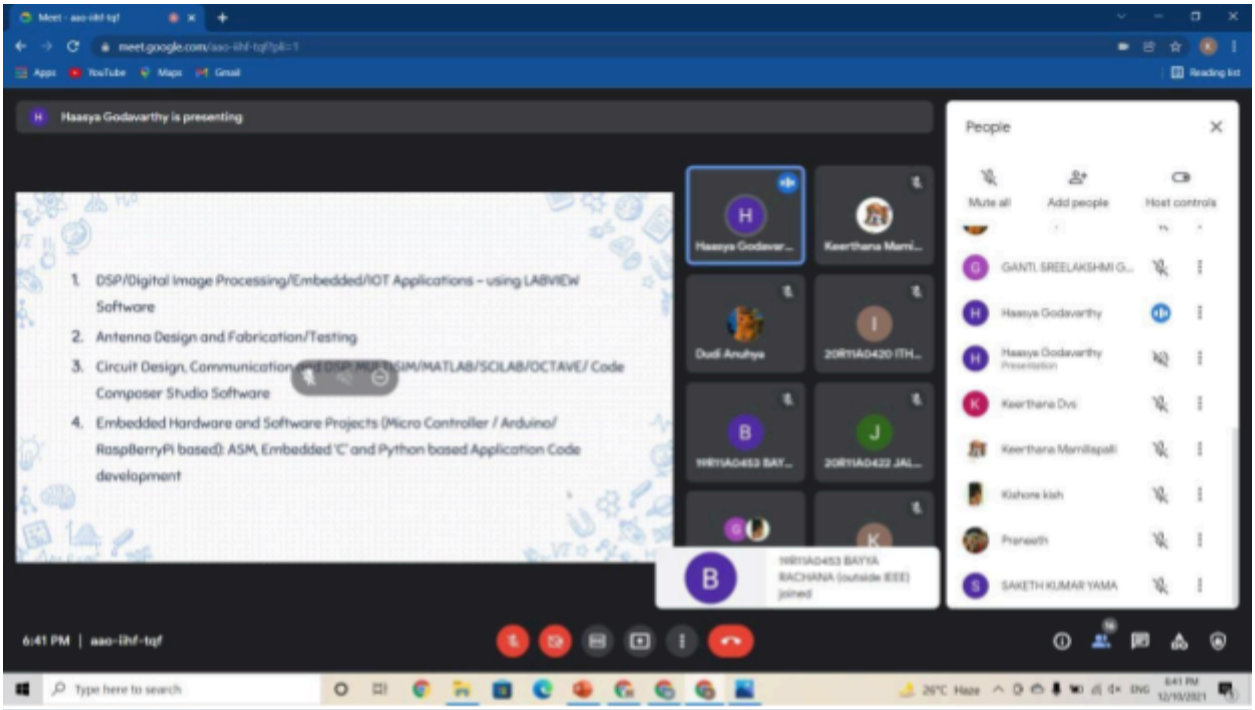
Agenda: To promote a thorough understanding of Selection of final year project in electronics and communications domine

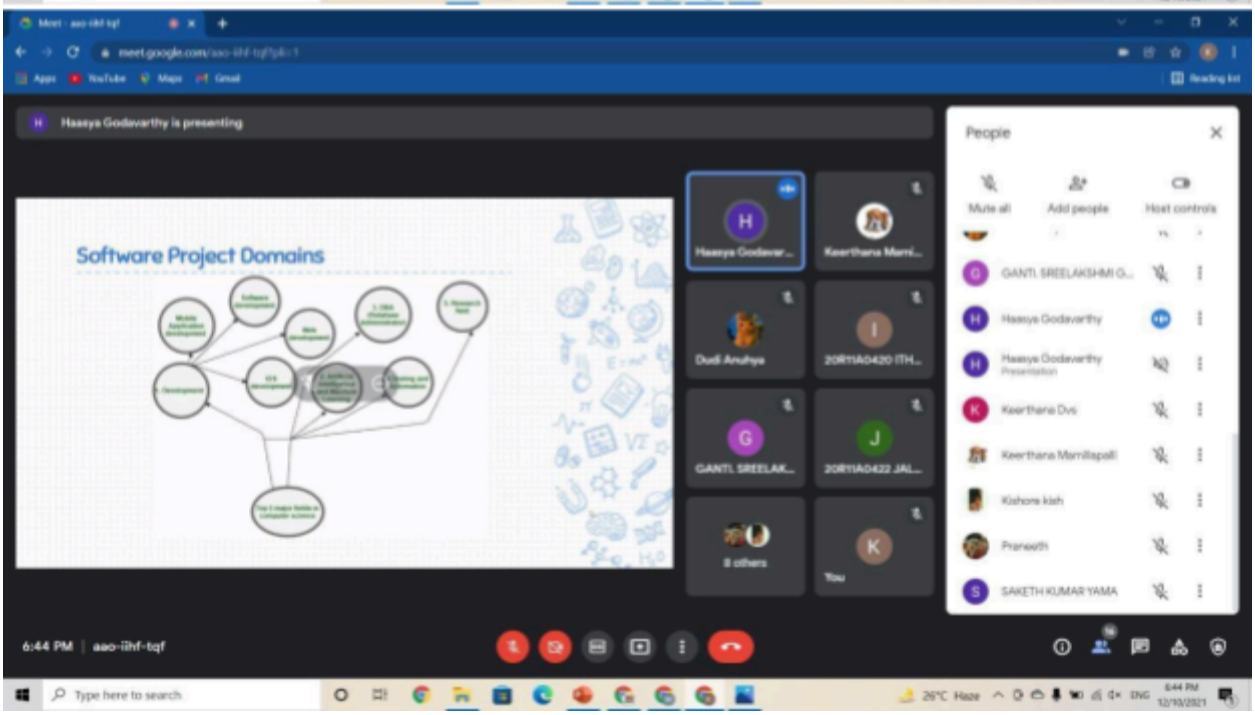
About Event:

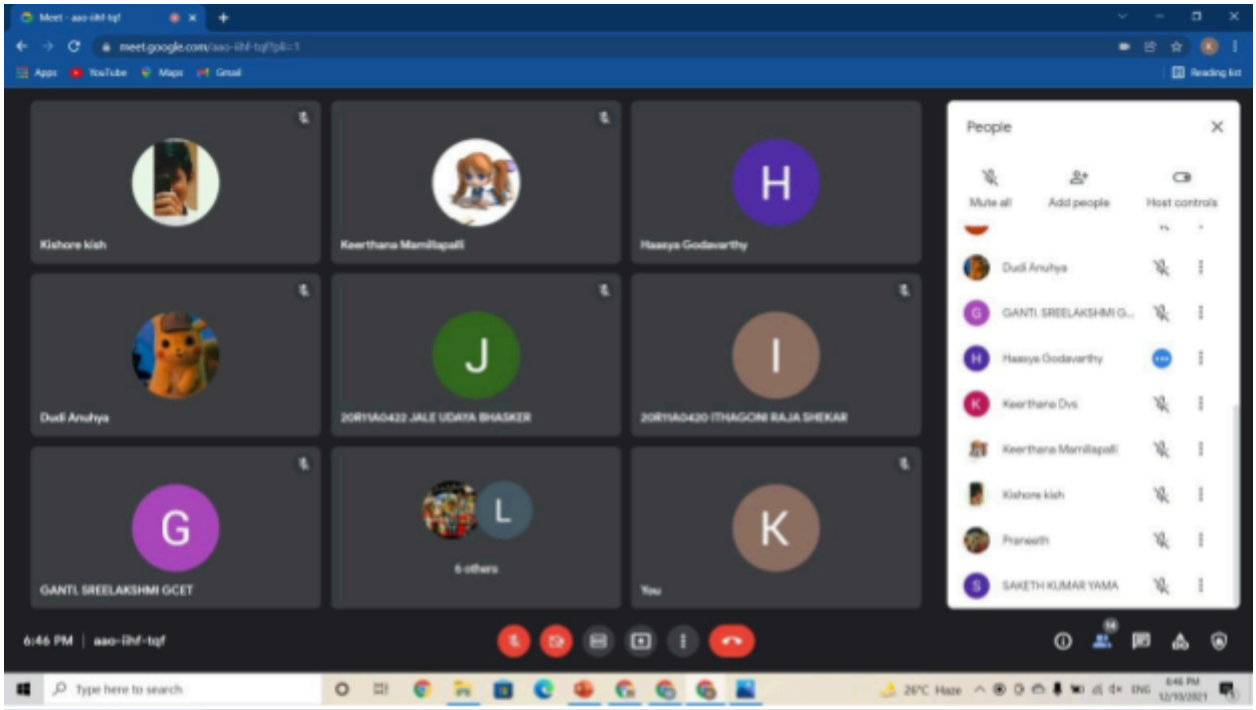
IEEE Circuits and Systems Society Student Branch Chapter GCET organized a Webinar on "How to select your final year project" an online webinar targeting II and III yr students of Geethanjali college of engineering and technology. This was the online webinar competition conducted by IEEE CAS SBC GCET and the motto behind conducting this event is to promote the importance of final year projects and various domains available to select the project in ECE . It consisted of common FAQ, platforms available to do projects, Ideas for projects

Event Poster:

Event images:






Kishore kish
Keerthana Mamillapalli
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Haasya Godavarthy
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J
20R11A0422 JALE UDAYA BHASKER
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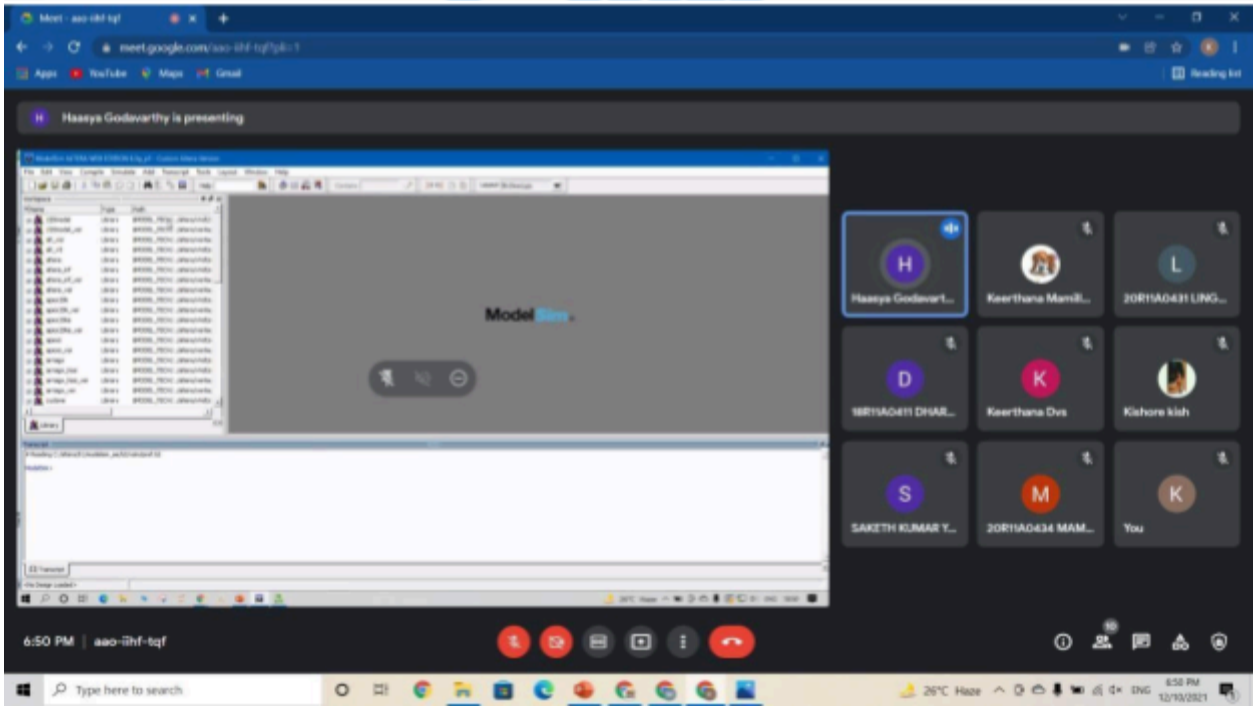
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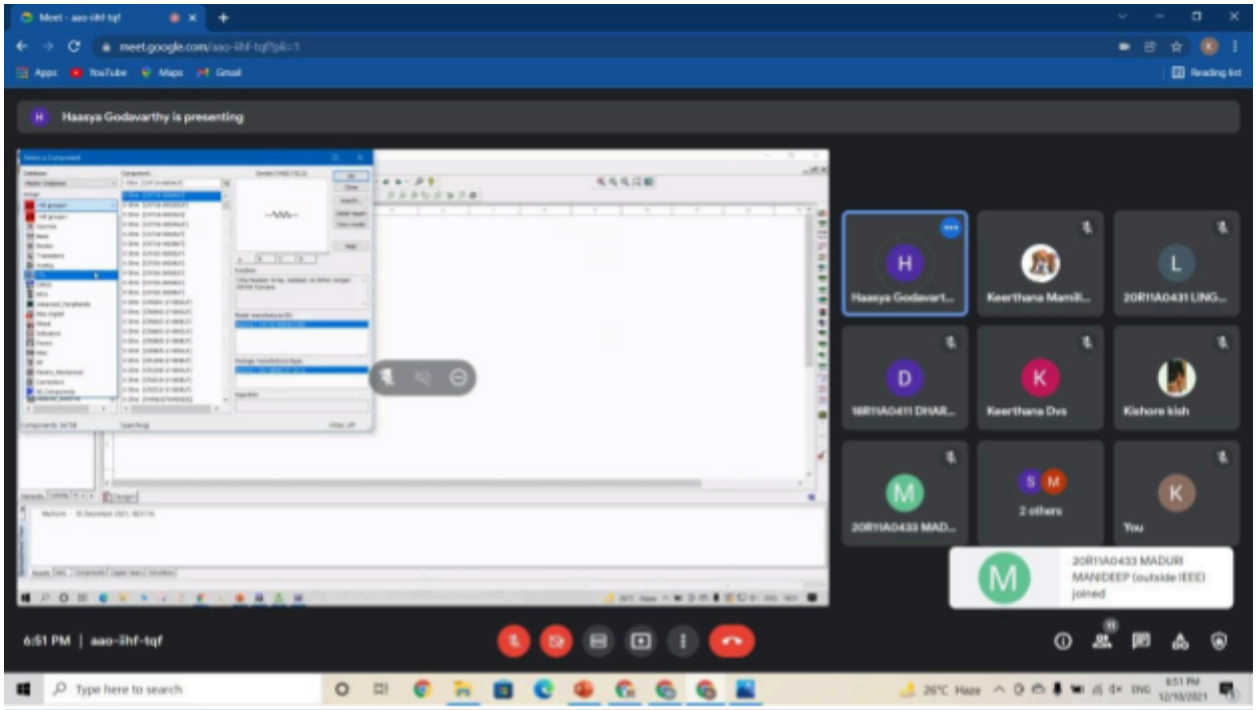
Haasya Godavarthy is presenting
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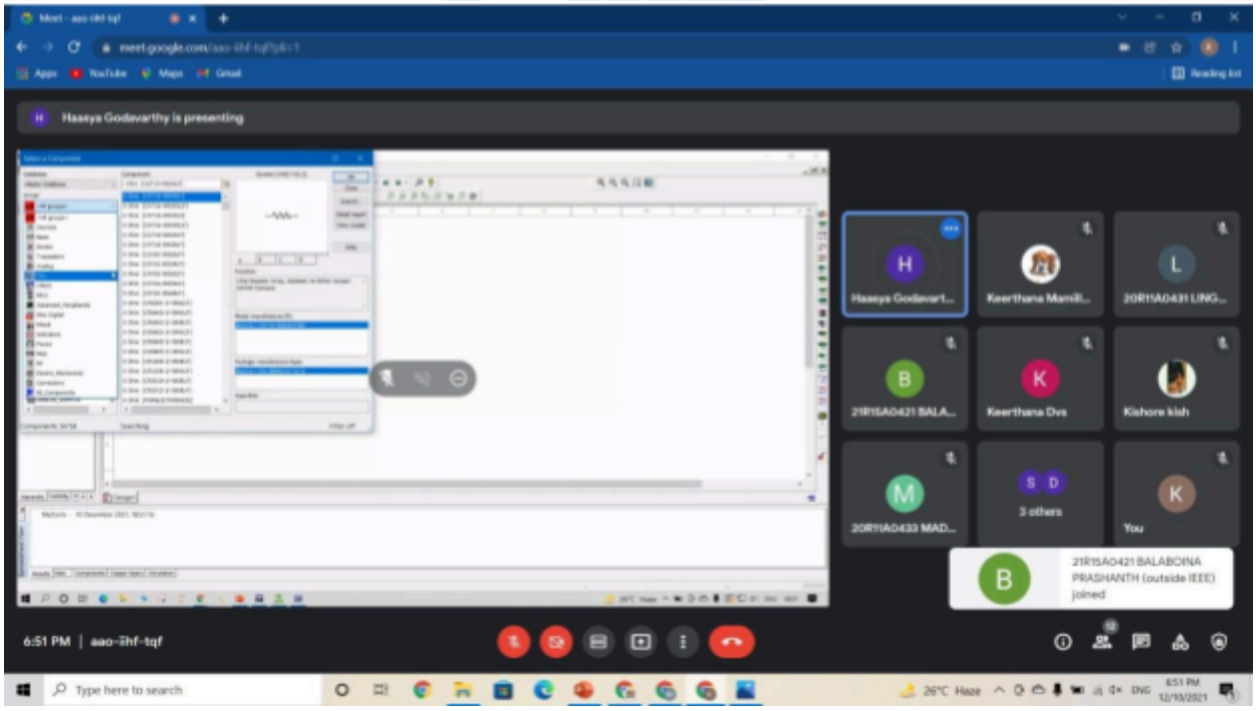
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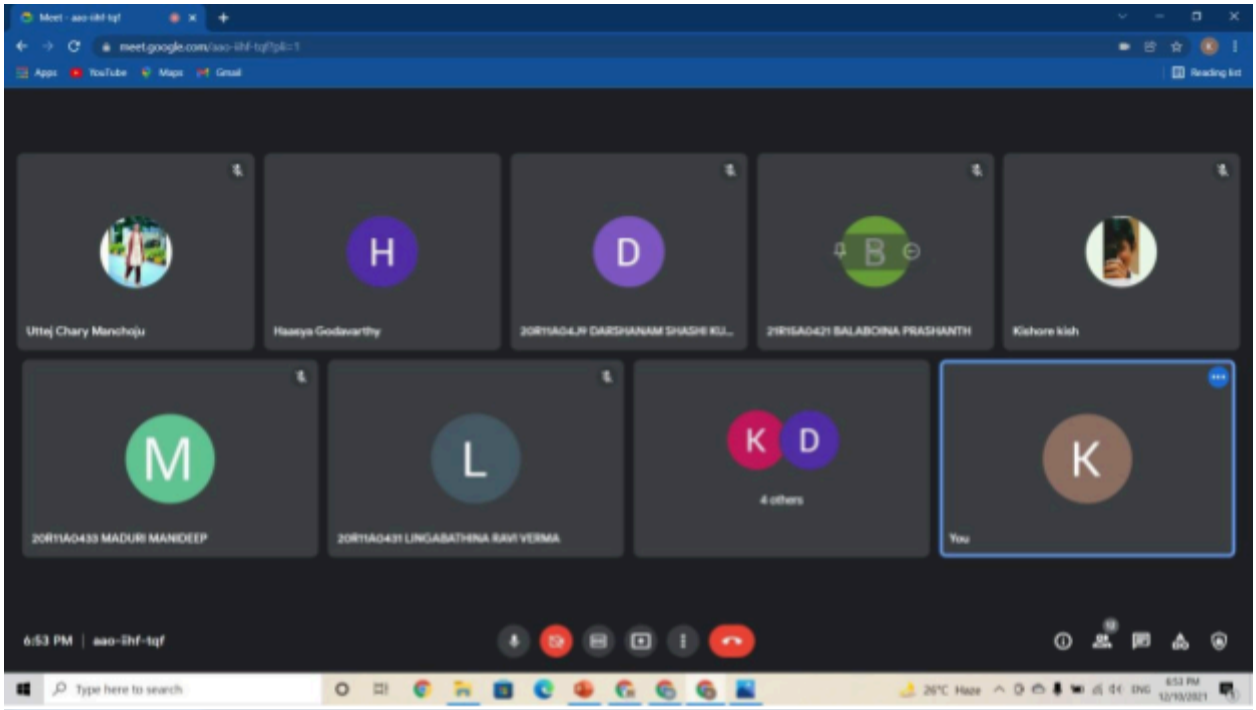
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4 others
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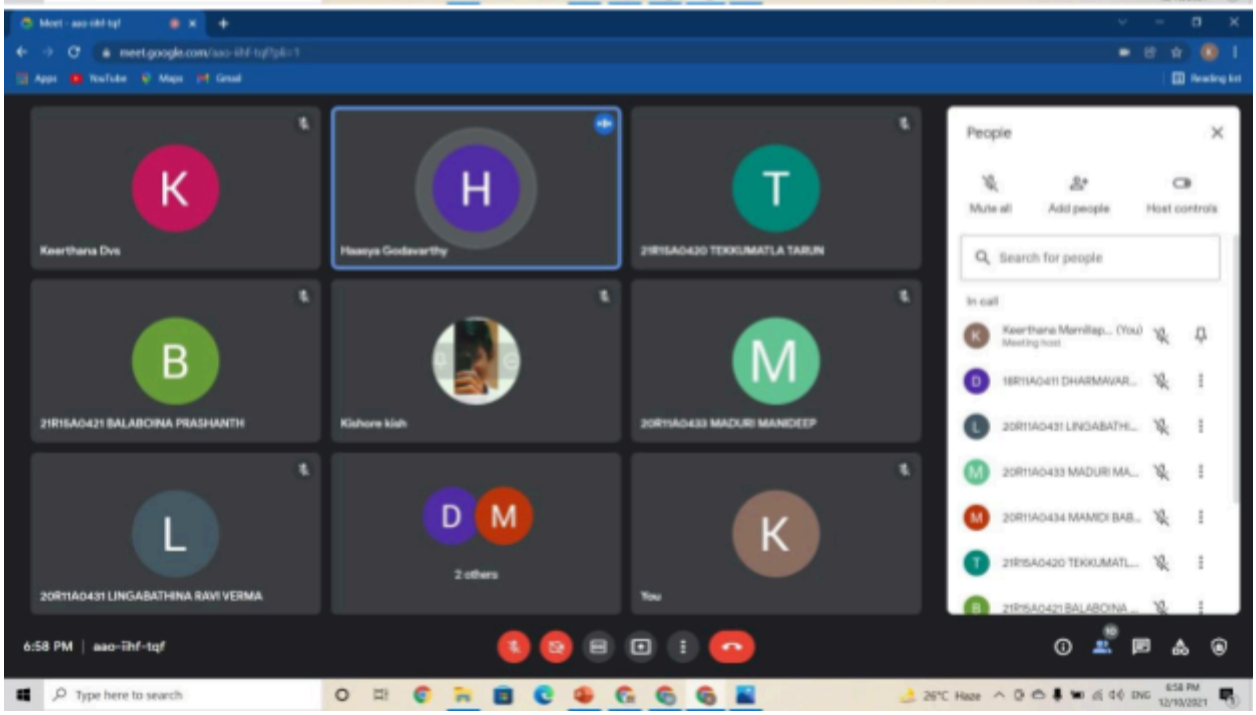
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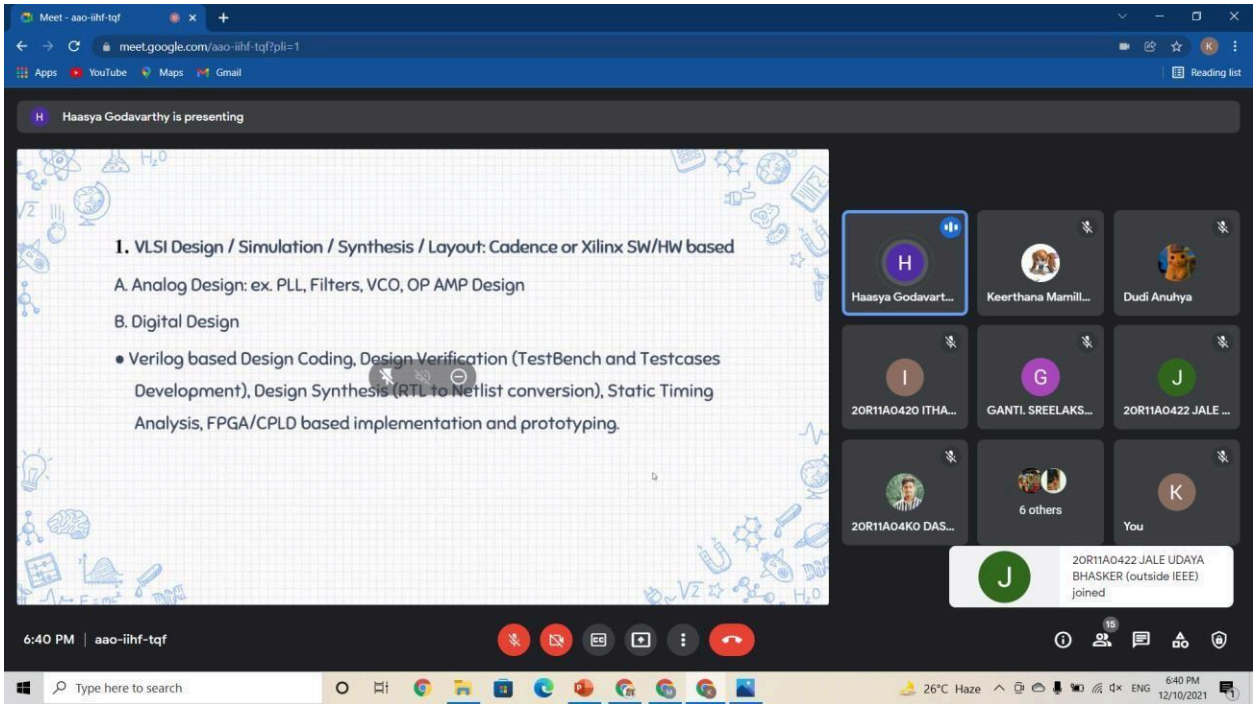

Event Coordinators:

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3. G.Akhila (18R11A0463 : ECE-4B)
4. G.Haasya (18R11A04A8 : ECE-4C)

Report prepared and drafted by:

M. Keerthana

Chair, IEEE SB GCET

Report of Webinar on

“Benefits of IEEE Membership”

Organized by IEEE CAS Student Branch Chapter-GCET

Dates: 11th December 2021. From 06:30 PM To 07:15 PM

- No. of Student Registrations: 40
- No. of Student participants: 24
- Target Students: B.Tech II and III Yr Students of GCET
- Registration Fee: Nill
- Speakers:

    1) Vishwa Prakash chary Vadla (Secretary for IEEE GCET SB (17-18), Chair for IEEE CAS GCET SBC (18-19)

Agenda: To promote a thorough understanding of IEEE membership and its benefits

About Event:

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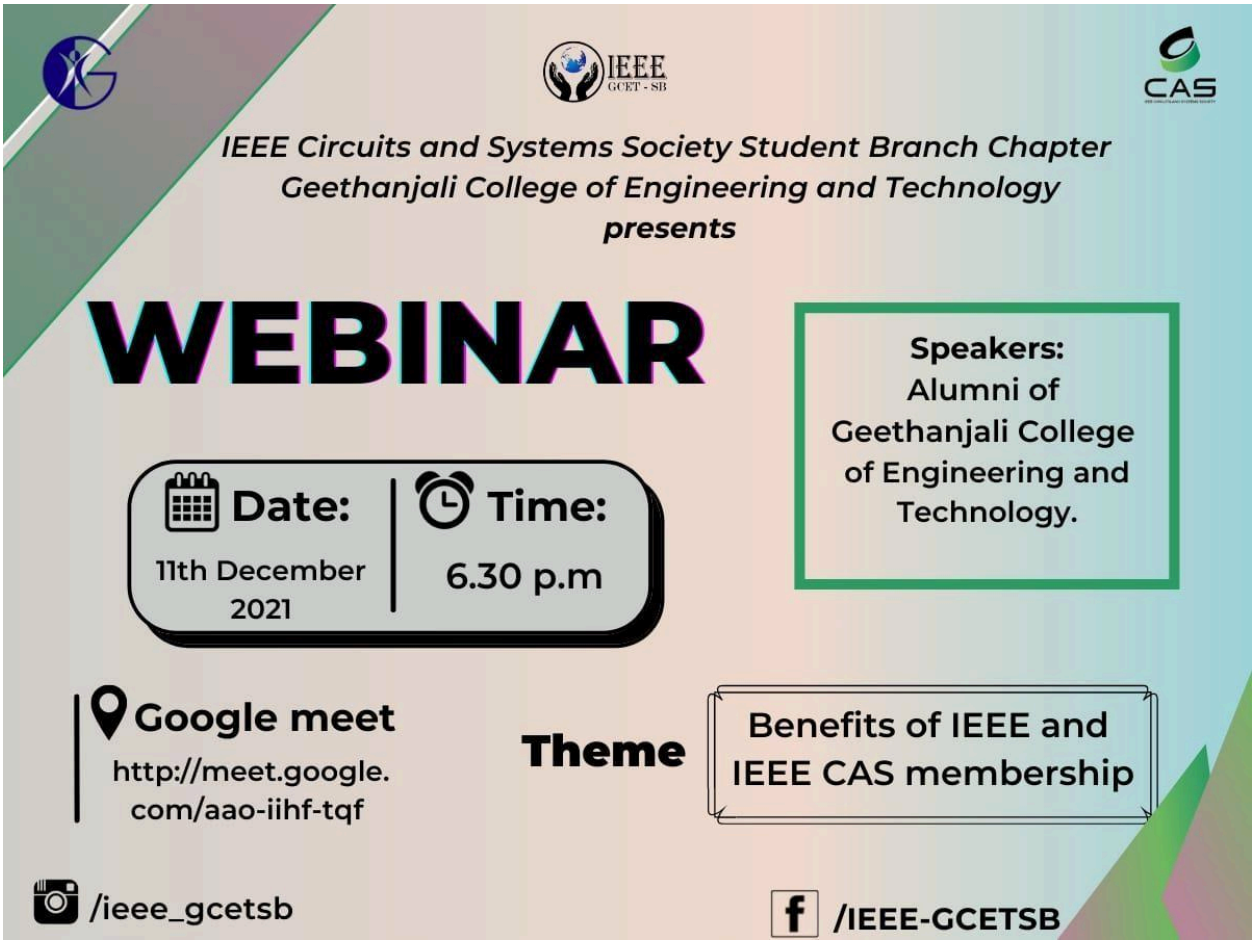

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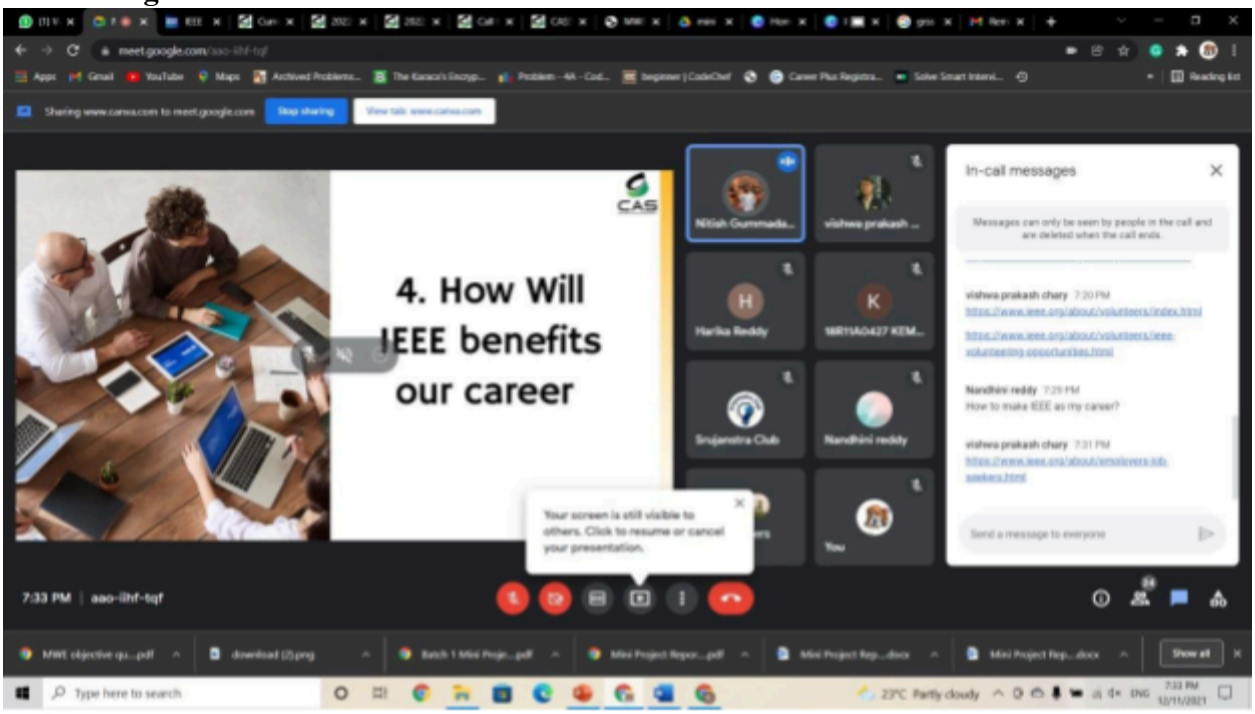

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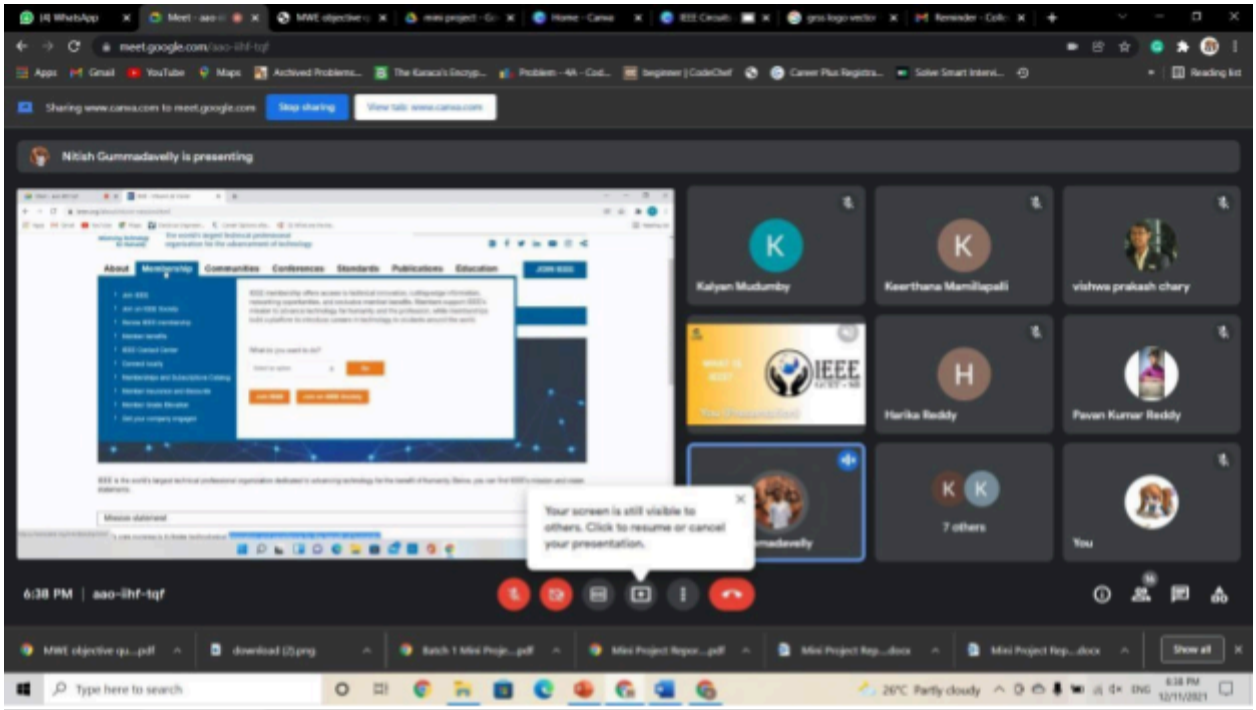
CAS

FUNDING	SOCIETIES	YEAR
$12Q0	CAS	2021
$1200	CAS	2021
$300	SPS	Z021
$500	SSIT	**2021**
6150	CS	2020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Harika Reddy
Pavan Kumar Reddy
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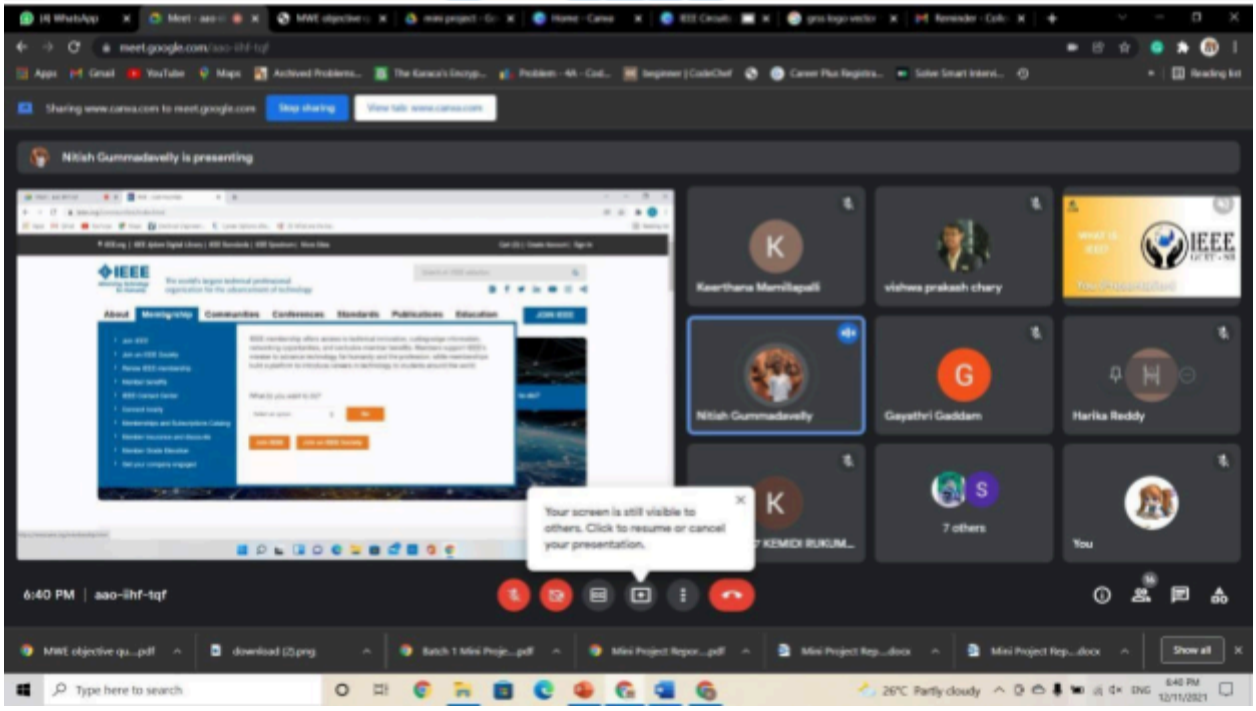
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Keerthana Mamillapalli
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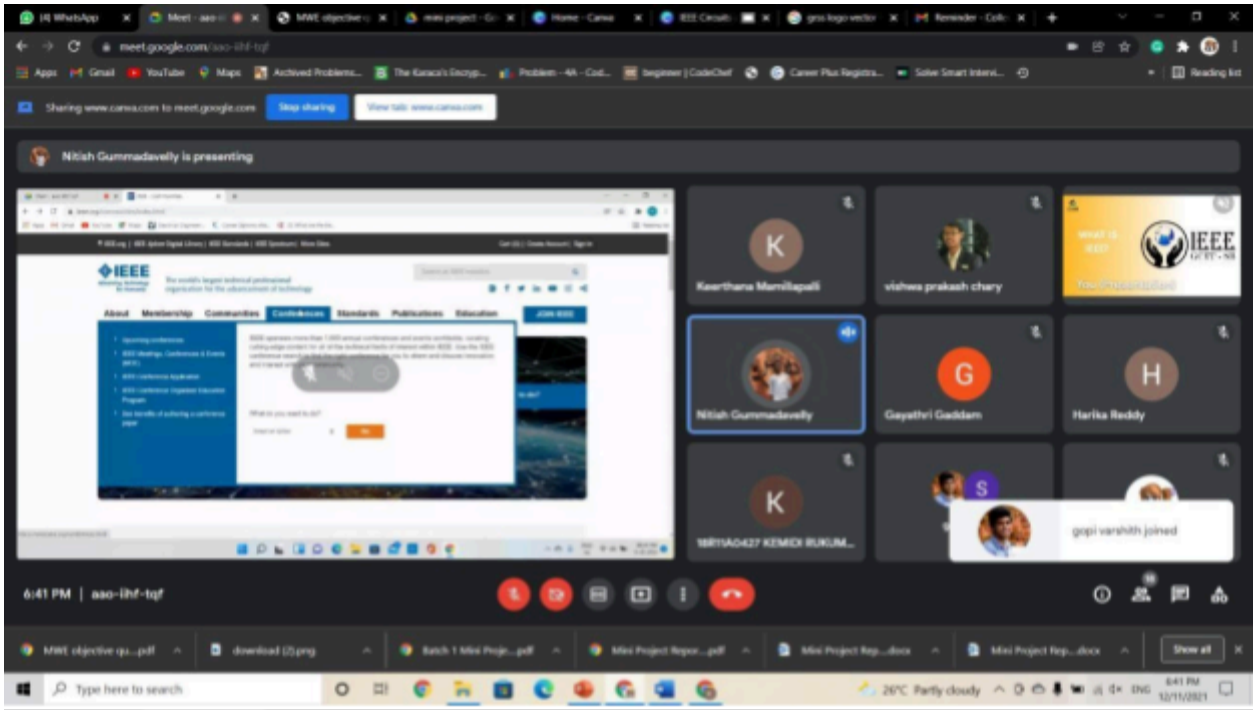

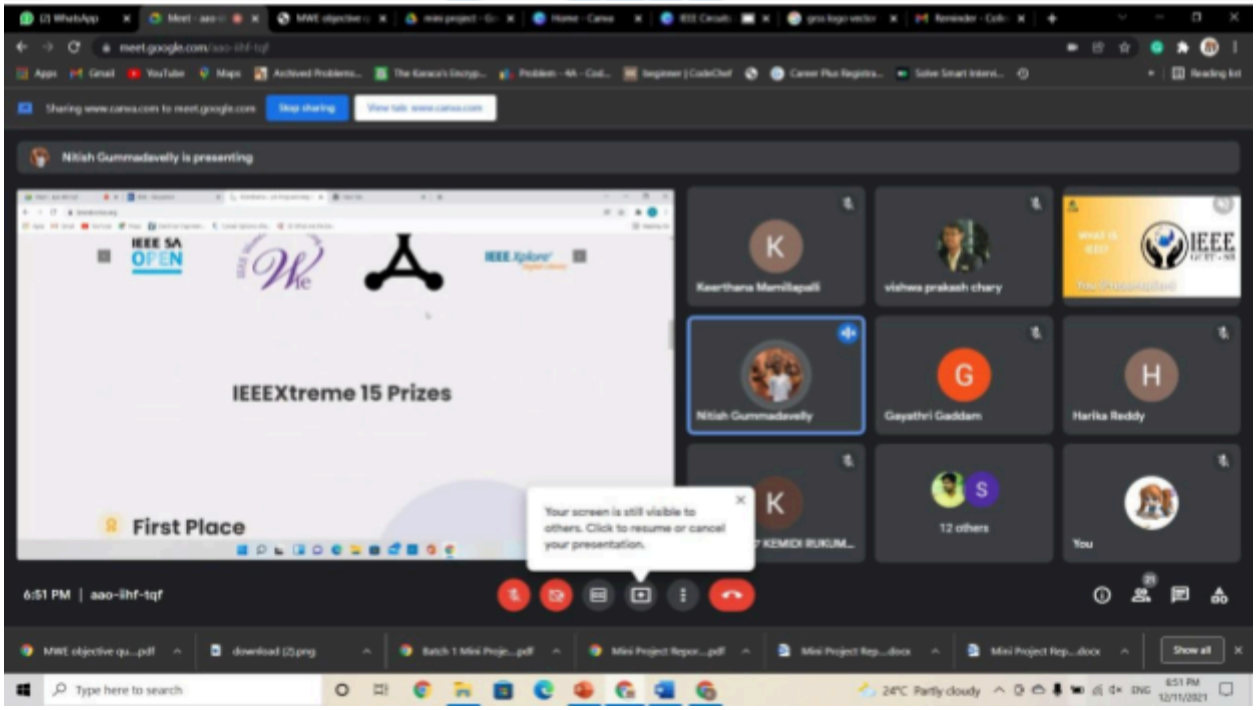

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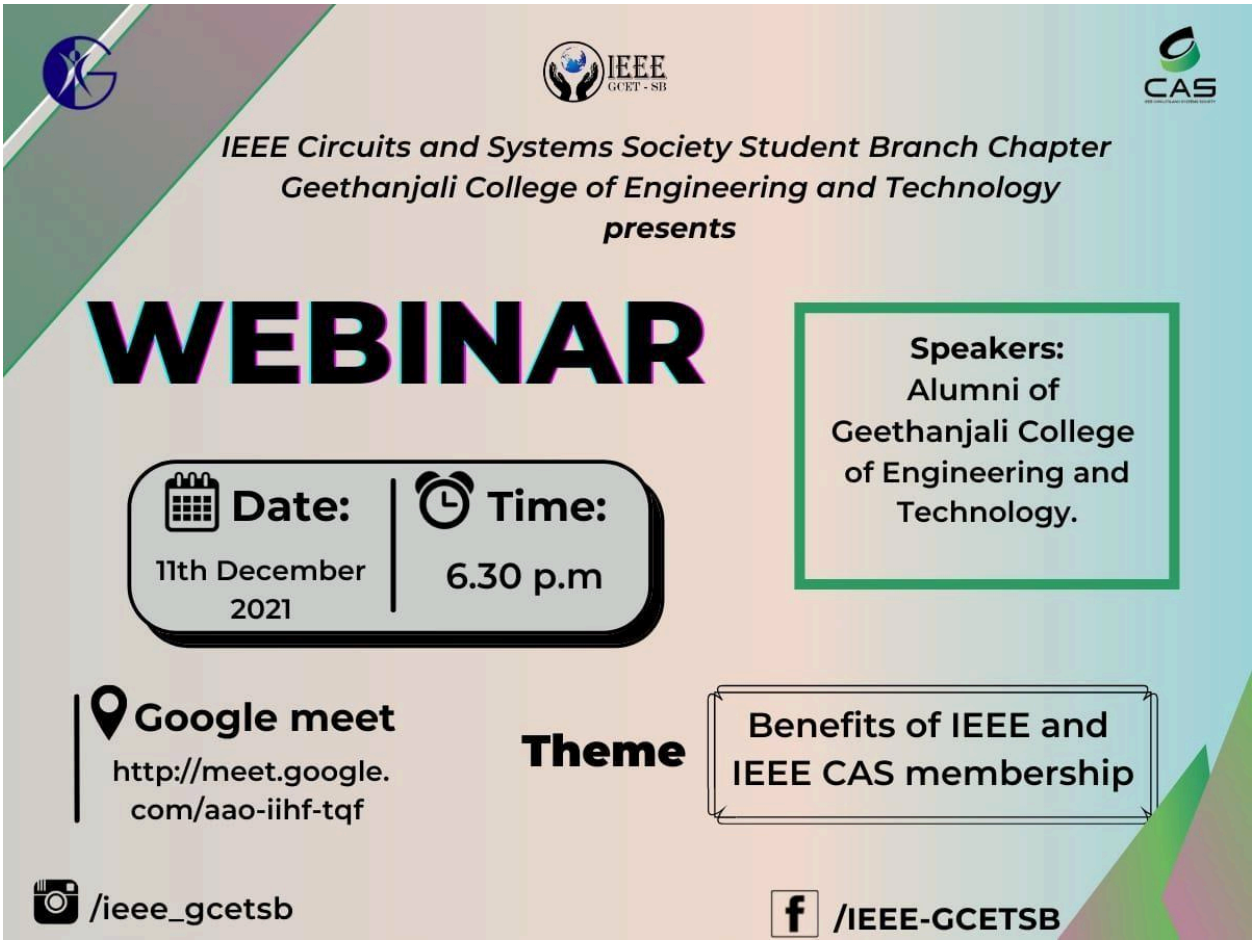

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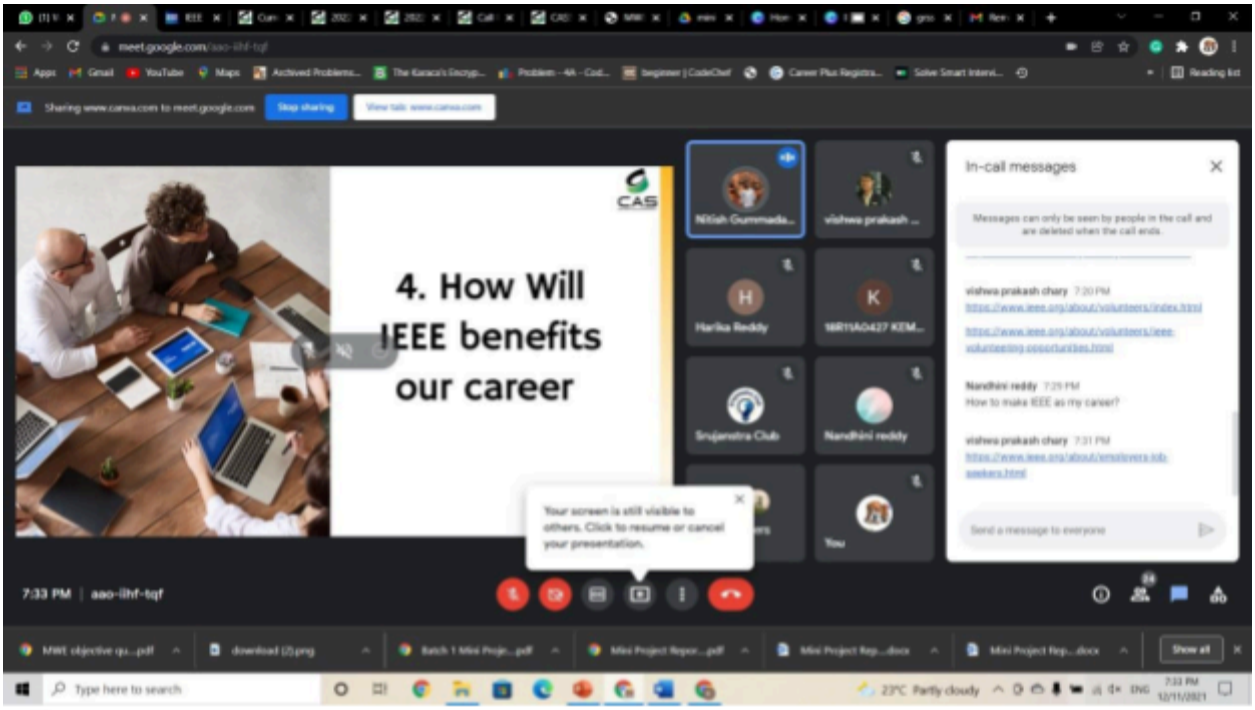

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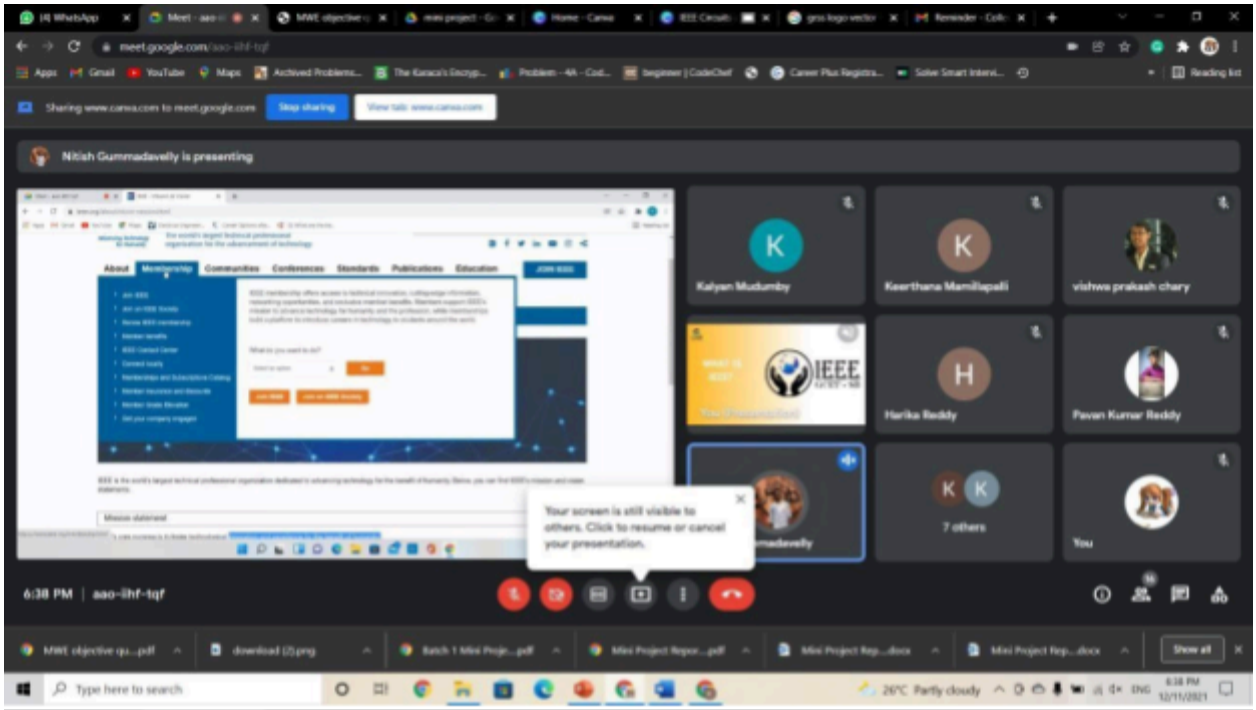
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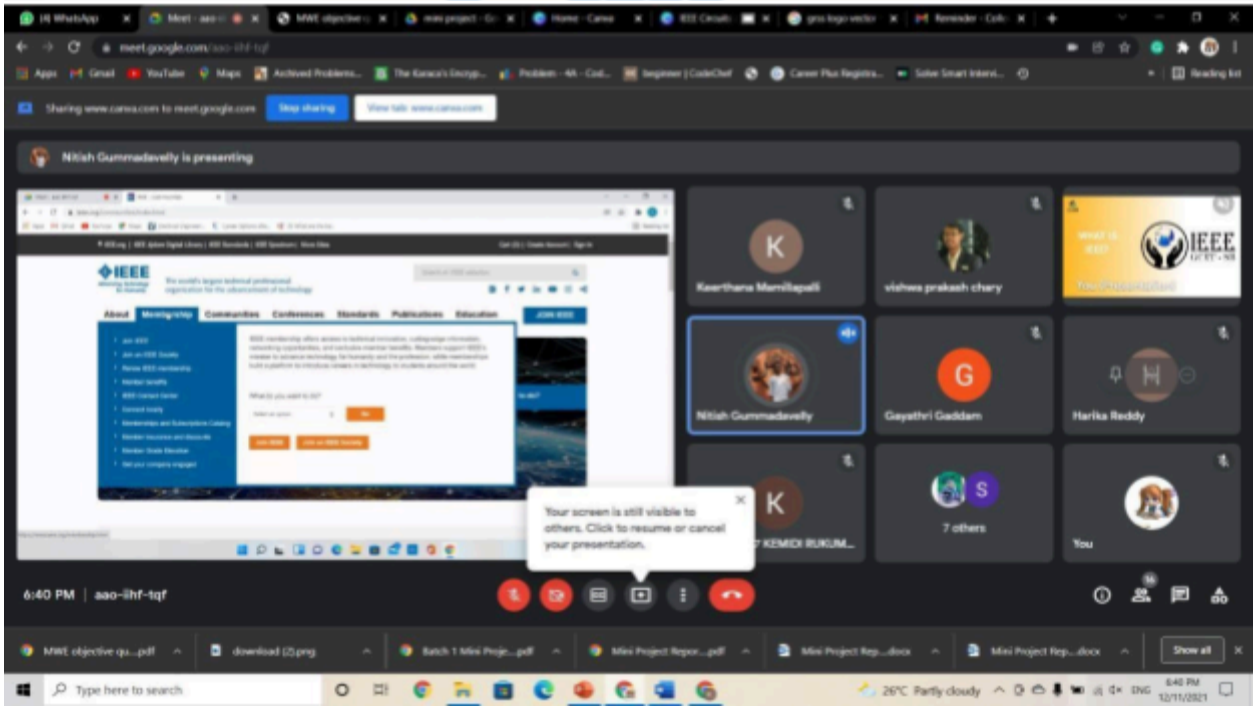
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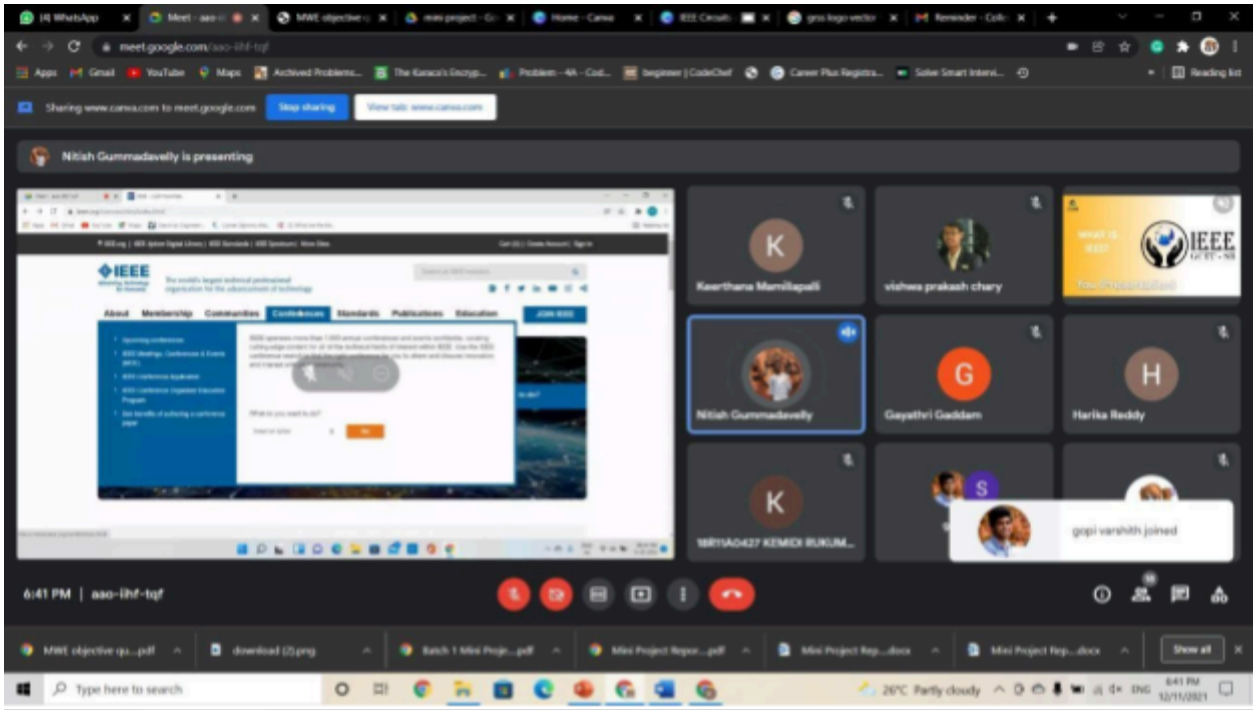

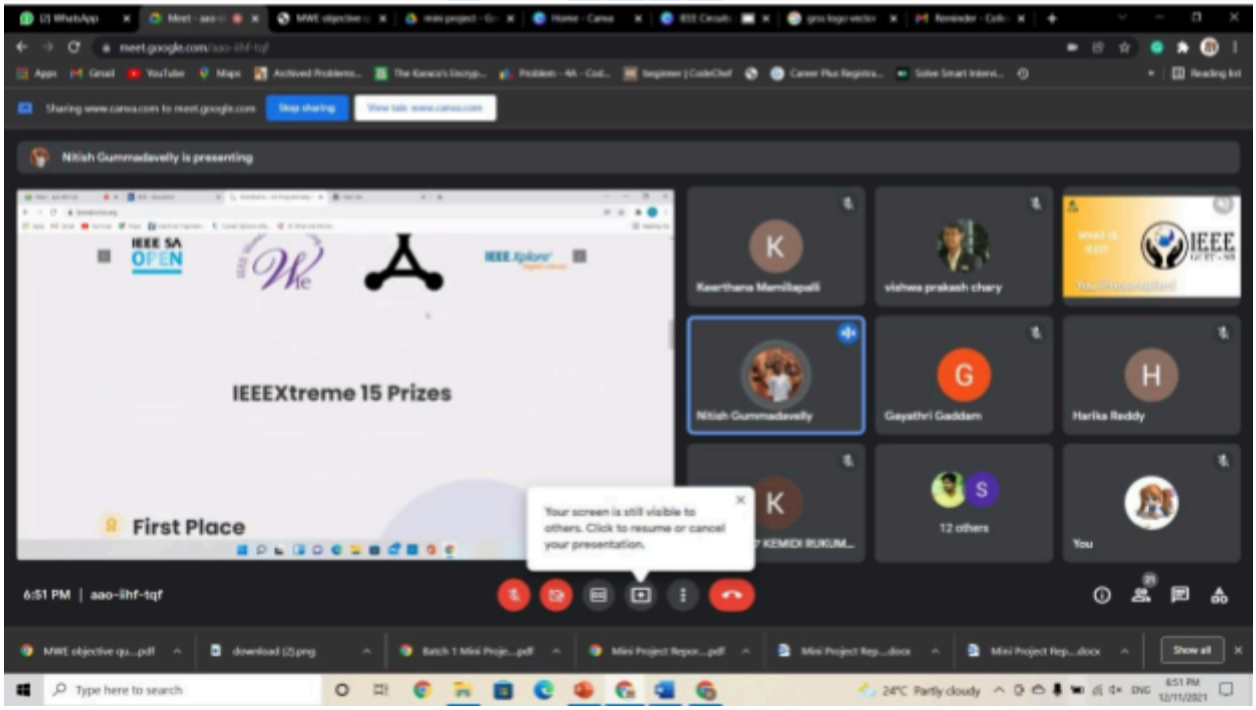

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