Task group name: Code-size-reduction
Extension or extension group name: Zc
Component names: Zc
Group contributor name: CAS/PLCT
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Creation date: 2021-04-12
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Version: 0.1

Requirements (prose describing what has to be done and what the end result is):

1. Implement the Zce specification in LLVM, GCC, QEMU, Spike https://github.com/riscv/riscv-code-size-reduction/releases/tag/V0.70.4-TOOLCHAIN-DEV

Deliverables (bullet list of components and the changes expected):

1. Zce implemented in either the LLVM or GCC assembler, and supported in one simulator (QEMU / Spike) to allow basic test writing to start.
2. Full support in one compiler (LLVM or GCC)
    a. Prototype releases will be useful so we can test them and give feedback
3. Full support in both simulators (QEMU and Spike)
4. Full support in both compilers (LLVM and GCC)

Acceptance criteria (bullet list with measurable results defined):

1. QEMU/Spike pass regression tests
2. Toolchains pass standard GCC/LLVM signoff criteria with Zce enabled

Projected timeframe (best guess):

1. 3 months

Sign off dates (done for every version > 1.0):

- Task group liaison sign-off date:
- Group contributor sign-off date: