N013: Happy send to Liverpool

Summary:
Status:
Problems: VP3-0 with ID 0x0 should be ID 0x785
Electrical tests:

- Communication test air ✓
- Communication?
- PRBS BTC✓
- TFC BTC✓
- Bandgap BTC✓
- Equalisation BTC✓
- IV-curves: BTC✓ATC✓

Band gap: Done before and after TC
IV curves: Done before and after TC
Status DB:

- Add PI after QA at production site
- Check completed

N014: Error problem

Summary: Technical problem with VeloPix CLI/VP0-1
Status: Waiting to further debug CLI/VP0-1
Problems:

1. Technical problem with VeloPix CLI/VP0-1:
    a. VeloPix registers can be read and written, except for matrix_ctrl 0x641. After writing to that register, all other registers start reading back 0xFFFF. These wrong readings disappear again after resetting the VeloPix.
    b. Status reply code from VeloPix is 0x001f, but should be 0x005f (on power-up) or 0x015d (after configure for QA). The missing bit 6 indicates that the VeloPix cannot synchronise itself with the TFC commands from the MiniDAQ.
    c. It is possible that when the module was first powered on, two wire bonds were touching each other. However, no spike in the current was observed. After it was realised the VeloPix was not responding as expected, the wire bonds were inspected and two were separated a bit better. Unknown where the wirebonds were located.
2. No TFC for CLI/VP0-1
   While working on wire bonds on CLI, ASIC 1 got damaged on periphery

3. No TFC for NLO/VP1-2: something is being counted if you ignore the TFC lock on the VeloPix. Not recoverable with high DC/DC and additional PLL reset.
4. Weird equalisation results for CSO/VP3-2: The right half of the matrix does not respond at all, and another 25% does not respond for one of the two scans. In total 51k pixels are masked.

Electrical tests: Not yet done
Band gap: Not yet done
IV curves: Not yet done
Update:

1. Karol saw the same problem on VP2-1 of the CERN electrical sandwich. The problem was triggered because the datapoints for performing the VeloPix hard reset were no longer subscribed to the GbtServer, i.e. the reset wasn't executed. Thus performing a hard reset before manipulating 0x641 prevents the problem from happening. This is already part of the default VeloPix configuration algorithm. Interestingly, the bad 0xFFFF or 0x0000 readings of all registers disappear automatically after about 3.5min
    - This problem is solved by adding the PLL step to the initialisation
    - The signals from the GBTx are there and look fine
2. CLI/VP0 SKT9 interconnect cable replaced by SKT9 from set #23 at 11-06-2021. not yet updated in DB
   Checked TFC 06-08-2021 problem solved with new wire bonds, didn't find a problem yet
3. NLO/VP1 tested with a test interconnect cable
   Original interconnect cable placed back at 22-07-2021
   TFC signals still missing for NLO/VP1-2
4. No update

Question 13/8/2021: TFC of NLO/VP1-2 still missing: did we check that the GBTx on this side is fine? If so, did we ever try with a different interconnect cable? Krista is quite sure that we never replaced the cable. So that could be the next step.

Update 13/8/2021: We replaced the NLO interconnect cable. The TFC is fine, but th N-side frequently go into error.
Update 14/8/2021: This is still the same after the weekend. The ASICs usually go into error mode simultaneously. It doesn't seem to matter which ASIC we turn on or how many. This behaviour is new. Could it be that the GBTx or chips got damaged by ESD in the repair?
Status DB:

- Add Thermal cycles
- Add E2
- Select thermal degradation
- Add PI after QA at production site
- Add PI finished module
- Add checklists

N016: Dead

Summary: Sparking + Communication problem with 2 VeloPix
Status: ??
Problems:

1. HV

Electrical tests: ??
Band gap: ??
IV curves: ??
Status DB: Module died during IV-curves...

- Add cool down
- Add Thermal cycles
- Add E2
- Select thermal degradation
- Add PI after QA at production site
- Add PI finished module
- Add checklists

N017: Happy send to Liverpool

Summary: HV problem for NLO/VP1 + Communication problem with CSO/VP3-2
Status: Waiting to debug further. We can increase the HV further.
Problems:

1. For tile NLO/VP1 the HV breakdown is already happening around 180V
2. CSO/VP3-2 does not respond when the module is warm (cooled at 15C), and on at least 2 occasions when cold (cooled at -27C). This did not show up during the electrical testing.

Electrical tests: All good
Band gap: Grade A
IV curves: ?? missing from DB
Questions: do we not see this chip at all? wirebonds or connector? need to inspect wirebonds.
17/2/2021: VP3-2 still unreachable. have tried if gently pushing on connectors helps, but no success. proposal would be to first inspect wirebonds, then replace interconnect cable.
Update:

1. No update
2. After swapping the interconnect cables to VP3-1 and VP3-2 the response in WinCC is identical. But we cross-checked that we are now talking to VeloPix 0x874 on VP3-1, which is on the outside of the tile. Therefore the problem is not with the VeloPix, but with the interconnect cable or the GBTx hybrid. We have to wait for a jig to replace the cable. (Also glue back the substrate to midplate)
3. Changing the cable did not help. Putting a ‘substitute GBTx’ the problem is fixed. However, in the mean time we also changed the dc/dc converters on the OPB.

4. Looking with the breakout board and the scope at the signals coming from the GBTx, the positive differential signal for the 40MHz main clock is missing (or very bad) and the positive differential signal for the ECS data is constant 1. We take these poor/missing signals as the explanation why we cannot communicate with the VeloPix

Status DB:

- Select thermal degradation
- Add PI after QA at production site
- Add PI finished module

N018: @Manchester

Summary: Communication problem: BH/N-side VeloPix reset
Status: Waiting to debug further.
Problems:

1. All BH/N-side VeloPix reset automatically when the module is cold. This is associated with a burst in the GBTx FEC counter. The time between resets varies from seconds up to 8 minutes. On 1 occasion also the GBTx itself got reset. Everything seems to point to bad signal quality corrupting the GBTx.
2. When the module is cold, a reset of the FH GBTx will put the BH GBTx in Error state. This can be avoided by keeping the watchdogs running, but will still put all six BH VeloPix in an unrecoverable Error state. Starting from this cooked-up scenario, we see the same issues as on N014 and N022: the VeloPix status reply is 0x001f (TFC bit missing) and after interacting with matrix_ctrl 0x641 the VeloPix hangs (always read back 0x0000 or 0xFFFF).
3. NLO/VP1-0 shows different TFC counts compared to the other VeloPix (2 occasions), and on 1 occasion missed FE reset and 50% of Calib A signals
4. With OPB v3, all TFC counters of NSI/VP3-2 remain 0. TFC is fine with the old OPB v2

Electrical tests: Incomplete due to VeloPix resetting
Band gap: Currently Grade F, but was Grade A in December
IV curves: ?? Not graded, but looks all fine to me?
Questions/comments on the reset problem:
* are the resets really simultaneously? (what time resolution do we have? -> 3 sec)
* assuming that they are really simultaneous, can we find evidence that the GBTx input link is off? For instance, a temporary glitch in the time could ‘move’ the reset bits, which are independent for all ASICs. However, this should be visible in the checksum (‘parity bits?’) on the GBTx. Are such errors counted? Do we continuously monitor errors on the GBx?

- Is there a bit-error test for the GBTx?
- how can we explain a temperature/power dependent effect? is there parameters that we can change on the GBTx?
- is the synchronization bit in the TFC okay when the reset happens?

Update:

1. This is solved by using the new OPB v3. This is a temperature dependent effect and can be monitored through the Rx Ready counters in the firmware (i.e. whatever upsets the VeloPix also upsets the outgoing signal from the GBTx). The effect can be influenced

(but not solved) by increasing/decreasing the modulation current of the GBLD. Shorting the Tx DV pin does not have any impact.
2. No update
3. This has disappeared in the latest test using the new OPB v3. Was not investigated in detail
4. The VeloPix cannot lock onto the TFC signal. However, the VeloPix can be configured to ignore the lack of lock (TFC_LAT 0x0534). In that case, the TFC commands are being counted, but they are shifted compared to normal. The BXID reset is counted in counter 2 instead of 1, the FE reset in counter 3 instead of 2, etc.
5. Weird TFC behaviour for VP1-2 and VP3-2. With OPB V4 we get
   VP3-2:
   - QA: no counts
   - QA ignore lock: Every counter is counting "counter-1"
   - QA + reset PLL: counts correctly, no interference from other VeloPix
   - PRBS: Every counter is counting "itself" && "counter+1"
   - Counts correctly in PRBS when VP3-0 and VP3-1 are unconfigured, or shutter remains closed

   VP1-2:
   - QA: Every counter is counting "itself"
   - PRBS: Every counter is counting "itself" && counter-1"
   - PRBS: does not count when only VeloPix in the tile configured. It needs all tiles configured to count, but will then count double.
6. Looking at the TFC signals with the breakout board and a scope, we did not see any obvious problems with the time alignment of the clock and data signals.

- CSO/VP3 SKT10 interconnect cable replaced by SKT10 from set #23 at 17-05-2021. not yet updated in DB

Status DB:

- Add Thermal cycles, no TC done?
- Add PI after QA at production site

N019: Happy send to Liverpool

Summary: Cooling problem with BH/N-side GBTx + Communication problem: FH/C-side VeloPix reset

Status: Waiting to be tested further

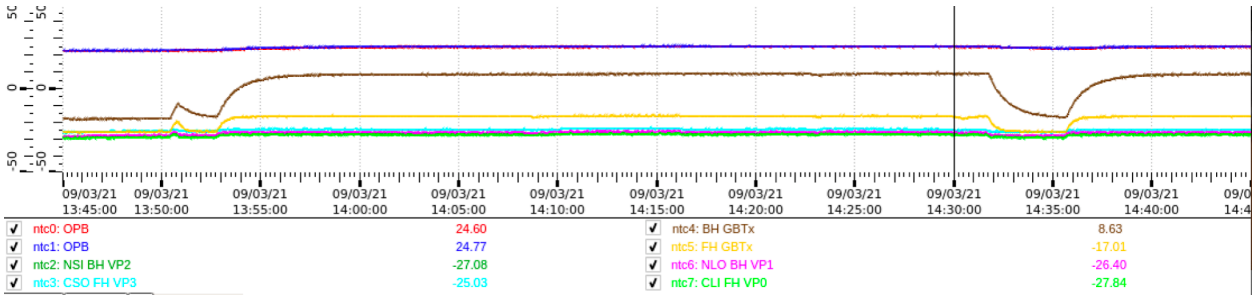
Problems:

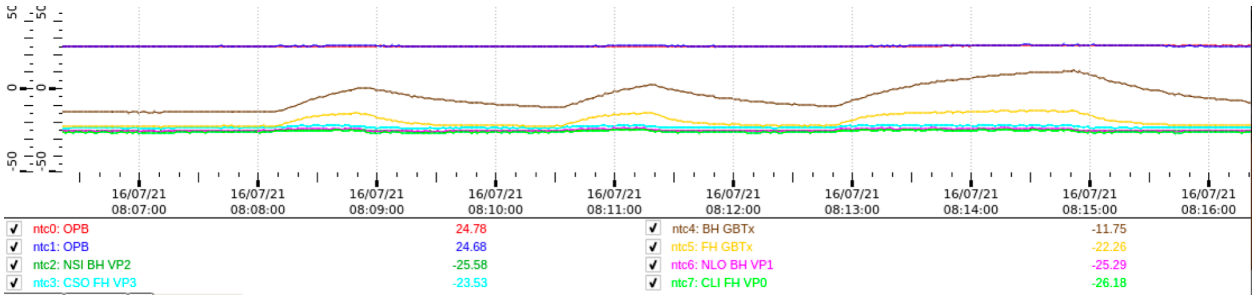
1. Cooling of BH/N-side GBTx: For the situation warm, i.e. 15C, when GBTx is powered, its NTC reaches 40C. This reduces the long-term life expectancy of the GBTx.
2. All FH/C-side VeloPix reset automatically. The time between resets varies with an average around 10 minutes, but in low power mode also saw only a few seconds.
3. Bad PRBS for NSI/VP2 cold (-30C), while PRBS had 0 errors when warm (15C).
   Upon retesting, links 10-16 now all give problems even when warm.

Electrical tests: All good at 15C, reset problems with FH VeloPix when cold. Bad PRBS for NSI/VP2

Band gap: Tested warm
IV curves: Grade A
Update:

1. Still present, needs reworking of the module (n-side GBTx hybrid)
   16/07: Module was cooled at -25C. When unpowered the BH GBTx was at -14C and the FH GBTx -22C. When powered the BH GBTx reached +10C before stopping the test, without reaching equilibrium. The FH GBTx reached -14C, but stable.
   Rework options: There is space on the bottom of the N-side GBTx to add glue, the other option is to completely remove the GBTx and glue again
   C-side GBTx is not inspected yet
2. Most likely solved by using the new OPB v3
3. Solved by replacing the long flex tapes and improving the clamps.





Status DB:

- Add PI after QA at production site

N020: Special needs

Summary: Cooling problem with BH/N-side GBTx
Status: Reworked ready for testing (08-04-2021)
Problems:

1. Cooling of BH/N-side GBTx: For the situation warm, i.e. 15C. When GBTx is powered, its NTC reaches 40C, which we considered unsafe to continue with testing. Situation is worse than N019.
2. After the rework we still have a bad PRBs on link 2 (NLO VP1-0) (not new!)

Electrical tests: Not yet done
Band gap: Not yet done
IV curves: Not yet done
Update:

1. Needs rework n-side GBTx hybrid, almost detached at 10-03-2021, reworked at 08-04-2021
2. During testing at 14-07-2021 link 2 is still bad (NLO VP1-0)
   30-07-2021 replaced data cable (NLO/SKT4) l**ink 2 is good**, link 14 (NSI/VP2-0) is bad and links 17 and 18 (CSO/VP3-0 and -1) aren't the best.
   - Link 14 NSI/VP2-0
   - Link 17 CSO/VP3-0
   - Link 18 CSO/VP3-1
3. 27-10-2021 Found disconnected solder on left bottom pins of the connector on data cable SKT2 to the data flex tape

Question 13/8/2021: link 14 also became bad after the repair. the cable was replaced on 30/7 (as for link 2), but in this case it didn't help. so perhaps the most puzzling is link 14. **Next step**: look at wirebonds and at the connector of the data cable. perhaps remove the data cable and look at the connector on the FE hybrid.

Update 03/11/2021: TFC still bad on VP2-1 in prbs mode. (fine in minimal/QA). The FH GBTx is about 4 degrees warmer than the other ntc when cooling at 15 degrees.

Status DB:

- Add PI after QA at production site
- Add PI finished module
- Add checklists

N022:

Summary: Technical problem with VeloPix CLI/VP0-0
Status: Waiting for thermal cycling
Problems:

1. Technical problem with VeloPix CLI/VP0-0:
    a. VeloPix registers can be read, but not written.
    b. Status reply code from VeloPix is 0x001f, but should be 0x005f (on power-up) or 0x015d (after configure for QA). The missing bit 6 indicates that the VeloPix cannot synchronise itself with the TFC commands from the MiniDAQ.
    c. It is unclear why parts (a) and (b) should be related.
2. Cooling of BH/N-side GBTx: For the situation cold, i.e. -27C. When GBTx is powered, its NTC is about 13 degrees warmer than the other 3. When it's off, its NTC is about 3 degrees warmer than the others.
3. Bad TFC counting in PRBS mode for NLO/VP1-1 and NLO/VP1-2. Both count correctly in minimal/QA and when the two other VeloPix remain in power-up state
4. No TFC for CLI/VP0-0
5. The C-side HV cable is not connected to the GBTx hybrid. Nonetheless there is a ground loop and current does flow.

Electrical tests: Not possible to test CLI/VP0-0, but all others are good.
Band gap: Grade A
IV curves: Grade A
Update:

1. VeloPix registers can be read and written, except for matrix_ctrl 0x641. After writing to that register, all other registers start reading back 0xFFFF. These wrong readings disappear again after resetting the VeloPix.
    - This problem is solved by adding the PLL step to the initialisation
2. Needs rework of n-side GBTx hybrid?
3. NLO/VP1-1 and NLO/VP1-2 count correctly with OPBv4 and higher DC/DC for VP1D
4.
5. Rework HV-cable done at 17-09-2021
6. Piggybag test 30-11-2021, did not fix FTC CLI/VP0-0 and modules destiny is Research and development >> 14-12-2021 Found that the wrong wire are pulled, TFC bonds CLI/VP0-0!!

Status DB:

- Add quick communication test
- Select thermal degradation
- Add PI after QA at production site
- Add PI finished module
- Add checklists

N023: Production phase

N025: HV problem

Summary: HV problem for CLI/VP0
Status: Waiting for testing
Problems:

1. For tile CLI/VP0 the HV breakdown is already happening around 160V. Current at 160V is 0.17 uA, increasing to 1.96 uA at 225V. It is slowly decreasing over time to 1.78 uA after 70 minutes.
2. Pattern in the noise on NSI/VP2-1

Electrical tests:
Band gap:
IV curves:
Status DB:

- Add Hybrid glueing C-side
- Add displacement test vcr, pump down and cool down
- Add Thermal cycles
- Add E2
- Select thermal degradation
- Add PI after QA at production site
- Add PI finished module
- Add checklists

N026: Happy send to Liverpool

Had difficulty connecting CSO but with the new tool by Hans Kok it works, sort of.

- Add quick communication test
- Add PI after QA at production site

N027: ?

N029: Happy send to Liverpool

happy module

- Add quick communication test
- Add PI after QA at production site

N030: Happy send to Liverpool

Summary:
16/8/2021: TFC for VP1-0 is missing.
17/8/2021: replaced interconnect SKT12. VP1-0 is now fine, but VP2-2 does not configure. visual inspection shows damaged wirebonds. probably happened during the cable replacement.

- Add quick communication test
- Add PI after QA at production site

N031: Production phase

Status on 2/11/2021

- bad link 2 (NSI ASIC 2)

N032: Production phase

N033: Production phase

No TFC for CLI/VP0-1
TFC for NLO/VP1-2 counts wrong
Still bad PRBS for CSO/VP3 after changing data cable
PRBS CLI/VP0 good, except link 8 has 1 error after changing data cable; found a wire in the connector to the data flex tape