VLSI System Design

ECE 474/574

Covid-19 Edition year two: The Vengeance

(the vaccines are coming!!)

(Syllabus subject to changes)

Syllabus for 2022 is here.

This class is an introduction to two important concepts in digital design: higher-level descriptions of digital designs in the SystemVerilog Hardware Description Language (HDL) and an introduction to the concepts of testing and exhaustive (formal) verification of a digital design. We emphasize connections to synthesis, differences between simulation and synthesis, and abstract thinking. You will not learn all of Verilog in this class, nor even a quarter of it. Our first objective is to develop your critical abilities when reading and coding Verilog so you know what is good "coding" practice and what isn't, what is a particular piece of code describing, and what happens to your code after you're done with it and it turns (hopefully) into gates. Our second objective is to instill in you the importance of verifying that your design works correctly in a systematic, quantitative and reproducible manner.
This course does not teach digital design. It is assumed you already have an idea of how to do that (see Prerequisites below). This course teaches how to implement a given design in Verilog.

Online Learning

One general guideline: *if you have difficulties with any part of the online setup to attend lectures, reach out to me NOW. Do not wait a week or 2 for things to get better. I might not be able to help you then.*
See "Guidelines for Remote Learning" under References and Guides module on Canvas. Read this syllabus carefully.

All listed times are Pacific Time. If you live in a different time zone, please make sure that you know what the deadlines are in your time zone.

If you are having IT issues - e.g., logging in, invoking a tool once logged in, ssh-related problems, etc --- please contact engineering IT. They will be able to help you. If it turns out your issue is not specific to you (e.g. a server is down) do let the class know through a Discussion on Canvas.

"Meeting" times

Tuesday and Thursday 12-1:50pm through Zoom.

The zoom link and password are sent in an announcement to registered students on Canvas

I do expect you to join the zoom lecture - this is to your benefit to ask questions which you otherwise can't, and interact with your classmates.
If, on a given week, you have some situation at home that would prevent you from joining us at the scheduled time, please let me know, so we can work something out.

Instructor and office hours

Prof. Houssam Abbas
(It's preferable to use Canvas for communicating about the course. Email is not a reliable medium because I get a lot of emails and can't get to it all in a timely fashion.)
Office hours: Thursdays 3-4pm
If these hours conflict with your schedule of classes and you wish to meet me, please message me on Canvas to arrange something different. See also TA office hours below.

Office hours will be delivered through Zoom. Link is on Canvas syllabus

I have instituted a "waiting room" on Zoom for office hours, to which you are admitted by default. This allows you to see me 1-on-1 if you want. Otherwise I usually let everyone in at once, as in a normal office.

Teaching Assistants

Connor Kurtz kurtzco@oregonstate.edu
(It's best to use Canvas for communicating about the course)
Office Hours: Mondays 12-1
Zoom link on Canvas syllabus.

Emanuel Caceres cacereem@oregonstate.edu
(It's best to use Canvas for communicating about the course)
Office Hours: Tuesdays 3:00-4:00. Zoom link on Canvas syllabus.
If this conflicts with your schedule of classes, please consider attending at the office hours from Connor or Prof. Abbas, otherwise contact me.

Discord channel

One of your classmates setup a Discord channel for class-related discussions and help:
https://discord.gg/MhVWPUfb

Course website

We use Canvas to assign worksheets, labs, deliver slides, readings and grades, and to communicate with each other: https://canvas.oregonstate.edu/

Course Prerequisites

ECE 271 and 272 or equivalent

Course learning outcomes

List the steps of the digital design process from market requirements to transistor layout
Analyze gate-level net lists to determine potential for glitches, timing-critical paths, and correspondence with the Verilog they were synthesized from.
Describe and use various Verilog constructs and their uses.
Explain the rationale for various design choices in finite state machines.
Construct an argument in formal methods
Execute a validation plan in terms of code coverage, functional coverage and model-checking properties.

Grading Criteria

Module 1 – Digital Design Flow HW 1: 5%	5%
Module 2 – Digital Design Using Verilog HW 2: 8.75% HW 3: 8.75% HW 4: 8.75% HW 5: 8.75%	35%
Micro-quizzes Distributed throughout the first half of the course	15%
Module 4 (yes 4) – Hardware Verification HW 6: 10% HW 7: 10% HW 8: 10%	30%
Micro-quizzes Code coverage:5% Functional coverage: 5% Formal Property Verification: 5%	15%

I may occasionally assign additional homeworks or give additional short quizzes if I feel the class needs it.

The conversion from numerical to letter grades is as follows:
95 - 100 = A
90 - 94 = A-
87 - 89 = B+
83 - 86 = B
80 - 82 = B-
77 - 79 = C+
73 - 76 = C
70 - 72 = C-
67 - 69 = D+
63 - 66 = D
60 - 62 = D-
Below 60 = F

Schedule

There is no textbook for this course. We will post reference material to the Canvas page under module References. The lectures should already be available before class, but I might update them after class too if needed.

In case of a discrepancy between the assigned dates below and the Canvas dates, the Canvas dates are the official ones.

Date	**Topic**	**Assignment released**
Module 1: Digital Design Flow Review Refresh the basics of digital design, timing diagrams, overview of design flow from architecture to transistors		
March 30	00 *Digital design flow* Abstraction levels; Synthesis; Process nodes; Leaky abstractions; *Syllabus*	
April 1 (Last day to drop with 100% refund is April 4)	*01 Architecture partitioning* 32bit multiplier refresher Tool usage Shell scripts and do files	HW1

Module 2: Design Using The Verilog Hardware Description Language Introduction to Verilog with an emphasis on the connection to synthesis and simulation.		
April 6	*02 About HDLs* About HDLs Verilog modules, ports, instantiation Verilog Execution Semantics	
April 8	*03 Always blocks and conditionals* Verilog always blocks Conditionals	HW2
April 13 (Last day to withdraw with 50% refund is April 18)	*04 Unique and synchronous logic* unique, priority Assign Statement initial Block Synchronous Logic	
April 15	*05 Synchronous blocks and Moore Machines* Synchronous Logic Blocks Moore-type State Machines	HW3 (Moore machines)
April 20	*06 One-hot and Mealy machines* EDA playground One-Hot State Machines Mealy State Machines	
April 22	*07 Verilog data types, numbers, and operators* Bash, testbench, do-files, simulation cmd-line verilog_data_types verilog_number_literals verilog_operators	HW4 (GCD)
April 27	*08 Resets* Synchronous or Asynchronous Resets	
April 29	*09 The dangers of X*	HW5 Counting ones
May 4	Quizzes review	
Module 4: Hardware Verification Rudiments of model checking, temporal logic and SystemVerilog assertions.		
May 6	*10 Design Verification in Context* Testing and Formal Verification	HW5.5 Image processor

	Types of coverage Assertions Test Plans	
May 11	*In-class questions-for-points* *11 Abstract Testing*	
May 13 (Last day to change grading basis is May 14) (Last day to withdraw, no refund is May 14)	*12 Code coverage*	HW 6: code coverage
May 18	*Coverage continued (and started)*	
May 20	*13 Functional Coverage*	HW 7: Functional coverage
May 25	*14 Formal Property Verification* SystemVerilog Assertions Model checking in practice	
May 27	*15 Formal Verification* Linear Temporal Logic and model checking	HW 8: Formal Property Verification
June 1	Quiz reviews	
June 3 (Last day to withdraw from term is June 4)	*16 Machine Learning in Verification*	Last mini-quiz due

Assignments

The homeworks are graded labs.
In labs, you must submit all the code you used for the homework. This includes the SystemVerilog files you compiled and simulated, shell scripts, DC input files, etc. Submit all this code as plain text files with the proper extension (.sv for SV files, .dc for DC, .sby for sby input files, etc). *Do not copy your code into a word document or the like. That will get a grade of 0.* We must be able to pass your files as-is to the various tools.

See here for other important submission instructions.

Micro-quizzes

Almost every week you will have a micro-quiz: that's a small quiz on Canvas. It is usually a multiple-choice quiz. Some questions have a checkbox by each answer rather than a radio button, which means that they have one *or* more correct answers. For these, select all answers that apply to get the point. Questions are shown one at a time. You can go back and forth between them.

You can start anytime in the week where it is assigned, but once you start it you must complete it within a time limit, usually between 5 and 10 minutes. (Canvas will tell you). **You only get one attempt.**
It mostly asks factual questions about the lecture material. The quizzes are designed so that you don't really have time to review the material *while* taking it. I strongly suggest you study the lecture first, *then* start the quiz. As the class advances, you must also be comfortable creating small Verilog programs and run them quick.
Questions are randomly selected from a pool of questions, so different students get different questions, and the choices appear in random order.
The correct answers are shown on Canvas after the quiz due date, so make sure you don't miss the due date because you can't submit it after the answers have become public.

Computing

Tool Usage Tutorial here:
https://docs.google.com/document/d/1V8X_23n4WmzFKZHuNFEa8X6C-dhOUIgjKRBrofgOy3w/edit?usp=sharing

Policies

Collaboration

You are encouraged to work together.

You may discuss the homework with other people to understand the problem and reach a solution. However, each student must write down the solution independently, without referring to written notes from others. I.e., you must understand the solution well enough in order to reconstruct it by yourself. In addition, each student must write on their homework the names of the people with whom they collaborated. If I suspect cheating, I might have the student come and solve additional problems in my office. If my suspicions are confirmed, I *will* refer the student to the disciplinary committee and request that the student fail the class.

Honor code

The purpose of problem sets in this class is to help you think about the material, not just give us the right answers. You are encouraged to use online resources for learning more about the material covered in class; however, you should **not** look for or use found solutions to questions in the problem sets. Specifically, you must not look at any code that has been created to solve the assignment, including solutions found on the internet to questions in the problem sets, code created by a student in a previous class or code created by a current classmate. Cheating will be punished according to university regulations as determined by the Office of Student Conduct. Familiarize yourself with the standards set forth in the OSU Code of Student Conduct section 4.2 (available at studentlife.oregonstate.edu/code). If there is any question about whether an act constitutes academic misconduct, it is your responsibility to seek clarification and approval from the instructor prior to acting. When in doubt, don't do it.

Late assignment policy

Assignments are due, as a general rule, a week after the day they are assigned, at 11:59 pm. Every late day is automatically penalized by 10 points. Thus suppose your assignment earns a grade of 80, but you submitted a day late. Your actual grade will be 80-10=70. After three days of delay, the grade is 0 (e.g. assignment is due Thursday but you submit on Monday). In exceptional circumstances (as determined by myself), I might allow a delay. Once a delay is set, it cannot be further extended. Please reach out as early as possible to discuss exceptions.

Grading policy

You have one week after a grade is released to ask me questions about it and seek a correction. After the week has passed, the grade is finalized. When releasing a grade, I also post comments where appropriate, explaining where you lost points, made mistakes, etc.

In case you are seeking a correction to the grade, you need a specific reason: e.g., your reasoning on question 2.a was essentially correct but your written explanation, you now realize, was ambiguous; my comments say that your model had syntax errors and I couldn't run it, but you can run it fine on your machine; etc. I cannot accommodate general requests that are a variation on "I think my grade was too low." Why do you think that? Based on our discussion, I might increase the grade, decrease it, or leave it as is.

Towards the end of the course, I usually get requests like "is there anything I can do now to bump me into the next letter grade?": the answer is almost always No. To get a grade you want, do the work above, and I will help you do it.

Of course, you can stop by anytime during the term to ask questions *about any part of the material*. The one-week deadline applies to grade-specific questions.

Special Accomodations

Accommodations for students with disabilities are determined and approved by Disability Access Services (DAS). If you, as a student, believe you are eligible for accommodations but have not obtained approval please contact DAS immediately at 541-737-4098 or at http://ds.oregonstate.edu. DAS notifies students and faculty members of approved academic accommodations and coordinates implementation of those accommodations. While not required, students and faculty members are encouraged to discuss details of the implementation of individual accommodations.

The definition of disability is not limited to physical disability. OSU's Nondiscrimination on the Basis of Disability policy states:

"...no qualified person shall, solely by reason of disability, be denied access to, participation in, or the benefits of, any program or activity provided by the University. Each qualified person shall receive the reasonable accommodations needed to ensure equal access to employment, educational opportunities, programs and activities in the most integrated setting feasible."