MICROPROCESSOR—CISC, RISC

1. RISC and CISC are both examples of different designs for computer microprocessors. The microprocessor, known as the central processing unit (CPU), is the brain of the computer.
2. It reads instructions from memory that tells the computer what to do.
3. Microprocessors use those instructions to perform very simple tasks, such as basic logic, controlling and input/output operations that are specified by the makers of the operating system.
4. RISC, which is an acronym for Reduced Instruction Set Computer, and CISC, short for Complex Instruction Set Computer, refer to the category of the processor, or more accurately, the instruction set architecture (ISA).
5. The ISA is the particular way the processor communicates with the human programmer.
6. The earliest computers had a CISC architecture, but in the 1980s, RISC architecture was developed to overcome the increasing complexity of CISC processors.

The CISC approach

The main idea behind CISC processors is that a single instruction can be used to do all of the loading, evaluating and storing operations. The goal of the CISC approach is to minimize the number of instructions per program. However, that increases the number of cycles per instruction.

Characteristic of CISC

1. Complex instruction, hence complex instruction decoding.
2. Instructions are larger than one-word size.
3. Instruction may take more than a single clock cycle to get executed.
4. Less number of general-purpose registers as operations get performed in memory itself.
5. Complex Addressing Modes.
6. More Data types.

The RISC approach

The primary goal of RISC processors is to make hardware simpler by using an instruction set that's composed of a few basic steps for loading, evaluating and storing operations. It's not necessarily about having fewer instructions, it's more about how those instructions are used. That reduces the number of cycles per instruction but comes at the cost of increasing the number of instructions per program.

Characteristic of RISC

1. Simpler instruction, hence simple instruction decoding.
2. Instruction comes undersize of one word.
3. Instruction takes a single clock cycle to get executed.
4. More general-purpose registers.
5. Simple Addressing Modes.
6. Fewer Data types.
7. A pipeline can be achieved.

Both approaches try to increase the CPU performance

RISC:

Reduce the cycles per instruction at the cost of the number of instructions per program.

CISC:

The CISC approach attempts to minimize the number of instructions per program but at the cost of an increase in the number of cycles per instruction.