Checklist for Schematics v2025-08-20

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- ☐ **Visual Design Best Practices**
  - ☐ Power supplies use supply symbols (not wires) with useful names.
  - ☐ Positive supplies point up, ground and negative supplies point down. Always.
  - ☐ All important nets are descriptively named
  - ☐ Net "stubs" (nets visually connected to only one pin) use an "off-sheet" type of label with the correct In/Out/Bidirectional flag shape and cross reference info (sheet / location)
  - ☐ Functional blocks are clearly labeled (maybe even with a box!)
  - ☐ Functional blocks have text that describes what they do and their requirements (e.g., Vbatt to 3.3 V @ 1 A switching power supply")
  - ☐ There's a frame around the schematic
  - ☐ It's clear where your power is coming from and what the power requirements are (V/I)
  - ☐ Data flow (inputs, outputs, requirements) are clear and labeled
  - ☐ All connectors have text that describes what they go to
  - ☐ Groups of nets above about ≥ 4 nets collected into buses
- ☐ **Schematic Symbols**
  - ☐ All symbols are schematic symbols, not packages (inputs on left, outputs on right, power on top and bottom)
  - ☐ Pins have correct electrical rule check (ERC) direction (inputs, outputs, passives, etc)
  - ☐ Components with symbolic shapes use those shapes (e.g, opamps are triangles)
- ☐ **Part values**
  - ☐ Capacitors have the appropriate voltage (≥ 2x working voltage)
  - ☐ Special case capacitors marked with power and tolerance
  - ☐ Power dissipation checked on all resistors
  - ☐ Special case resistors marked with power and tolerance
  - ☐ Layout features that are circuit elements (e.g., copper inductor) are labeled in the schematic
- ☐ **Circuit Gotchas**
  - ☐ MOSFETs oriented correctly WRT the body diode (!)
  - ☐ Check IC part numbers reflect the correct package type
  - ☐ Small, low ESR (e.g., ceramic) bypass capacitors on all IC supplies
  - ☐ Check voltage inputs and outputs match across power domains (e.g., 5V to 3.3V)
  - ☐ Check that powered-off domains are not phantom powered by their inputs from other circuits (including test circuits, like UARTs)
- ☐ **Design for Test**
  - ☐ Place test points on critical signals (consider through hole test points for bed-of-nails testers)
  - ☐ Add debugging hardware (e.g., LEDs, UART connectors, jumpers, scope probe points, etc)
- ☐ **Design for Fail**
  - ☐ Group components in separable modularly powered blocks and use zero ohm resistors or cuttable jumpers to disconnect (especially for switching power supplies!)
  - ☐ Unused pins go to usable test points. Consider adding some random pull-up and pull-down resistors connected to a test point on the board, too.
  - ☐ UART (serial port) TX/RX are always mixed up, consider cuttable jumpers here.
- ☐ **Electrical Rule checks**
  - ☐ **No unapproved errors OR warnings in the ERC**
  - ☐ All important excluded errors/warnings have a comment on why they're approved

- [ ] **BOM Fixes**
    - [ ] Add “MFR” (Manufacturer) and “MPN” (Manufacturer’s Part Number) to all components as attributes
    - [ ] Bonus points for adding a datasheet link and description to part attributes
- [ ] **“Almost Done” checks**
    - [ ] **Your schematic is peer reviewed by at least one person not involved in the design.**
    - [ ] Check that your specialized parts are in stock at a distributor
    - [ ] Re-run ERC and double check your approved errors, looking for accidentally approved errors..
    - [ ] Update your schematic version and/or date

Please comment on this checklist using Google Doc Comments!!