SIR C R REDDY COLLEGE OF ENGINEERING, ELURU

Approved by AICTE & Affiliated to JNTUK, Kakinada

Department of ECE

II/IV B.TECH (R20), SEMESTER –II, A.Y. 2023-24		
ASSIGNMENT -1		
Subject:	**DICD (R2022042)**	
Section:	**A, B & C**	**Marks: 5M**
Date of instruction	**12/01/2024**	

Note	ANSWER ALL QUESTIONS			
S. No	**QUESTIONS**	**Marks**	**CO**	**Level**
1	Write brief notes on data types, data objects, operators and identifiers in VHDL?	**5**	1	**L1**
2	Design half Subtractor using three modeling styles?	**5**	2	**L2**
3	Write functional tables and excitation table for all Flip-flops with logic diagram?	**5**	3	**L2**
4	List out the different Operators available in Verilog HDL. Explain with example? What are the various data types supported by Verilog HDL?	**5**	1	**L1**
5	Explain hazards in digital circuits?	**5**	3	**L2**

CO. NO.	**COURSE OUTCOMES**
CO1	**Learn the Hardware Description Language (VHDL & VERILOG).**
CO2	**Understand the structure of commercially available digital integrated circuit families.**
CO3	**Analyze and design combinatorial and sequential logic circuits using HDL code.**
CO4	**Interpret the digital logic circuits using MOS logic circuits.**

BLOOMS TAXONOMY LEVEL					
L1	**L2**	**L3**	**L4**	**L5**	**L6**
Remember	Understand	Apply	Analyze	Evaluate	Create