BMS College of Engineering, Bangalore-560019

LESSON PLAN – Even Semester 2011

Subject	Credits	Faculty	Department	Sem
Low power VLSI design (06IT841)	4	Mr. Harish V. Mekali	Instrumentation Technology	VIII

Week	Unit	Class	Topics
1	1	1	Introduction
		2	Need for low power VLSI chips
		3	Sources of power dissipation on Digital Integrated circuits
		4	Emerging Low power approaches
2		5	Physics of power dissipation in CMOS devices
		6	Discussion
	2	7	Device & Technology Impact on Low Power
		8	Dynamic dissipation in CMOS
3		9	Transistor sizing & gate oxide thickness
		10	Impact of technology Scaling
		11	Technology & Device innovation
		12	Discussion
4		13	Discussion
	3	14	Power estimation, Simulation Power analysis
		15	SPICE circuit simulators, Gate level logic simulation
		16	Capacitive power estimation, Static state power
5		17	Gate level capacitance estimation
		18	Architecture level analysis
		19	Data correlation analysis in DSP systems
		20	Monte Carlo simulation
6	4	21	Probabilistic power analysis
		22	Random logic signals, probability & frequency
		23	Probabilistic power analysis techniques, signal entropy
		24	Circuit level power consumption in circuits

7		25	Flip Flops & Latches design
		26	High capacitance nodes, low power digital cells library
	5	27	Logic level: Gate reorganization
		28	Signal gating
8		29	Logic encoding
		30	State machine encoding
		31	Pre-computation logic
		32	Discussion
9	6	33	Low power Architecture & Systems
		34	Power & performance management
		35	Switching activity reduction
		36	Parallel architecture with voltage reduction
10		37	Flow graph transformation
		38	Low power arithmetic components
		39	Low power memory design
	7	40	Low power Clock Distribution
11		41	Power dissipation in clock distribution
		42	Single driver Vs distributed buffers
		43	Zero skew Vs tolerable skew
		44	Chip & package co-design of clock network
12		45	Discussion
		46	Discussion
	8	47	Algorithm & architectural level methodologies
		48	Introduction, design flow
13		49	Algorithmic level analysis & optimization
		50	Architectural level estimation & synthesis
		51	Discussion
		52	Discussion

TEXT BOOKS:

1. Practical Low Power Digital VLSI Design-Gary K. Yeap, KAP, 2002
2. Low power design methodologies Rabaey, Pedram-Kluwer Academic, 1997.

REFERENCE BOOKS:

1. Low-Power CMOS VLSI Circuit Design-Kaushik Roy, Sharat Prasad, Wiley, 2000