

# AMD: “It’s Hammer time”

Athlon 64 codename “Hammer” became an architectural design revolution. From a single core architecture bonded by a front side bus to a northbridge which implemented a memory controller and southbridge for peripherals the paradigm has shifted to a multi-core design with an integrated memory controller, a relatively narrow but reaching very high frequency dedicated bus to connect either with peripheral hub (what the southbridge has transformed to) or another CPU in case of an SMP configuration. Even modern systems released more than 20 years later fit this description - that’s how revolutionary this design was back then.

I’ll make a brief review of its history for better understanding of the latter and will describe it in detail in a separate chapter. The first live demonstration of AMD Hammer was ironically during Intel Development Forum (IDF) in 2002. It was done using A0 revision engineering samples equipped with 256KB of L2 cache and with a frequency of 800MHz. Later this year demonstrations were made using A1 revision samples achieving 1200-1400MHz with the same 256KB L2 cache. In the end of 2002 and beginning of 2003 AMD produced pre-production CPUs using B0 revision. Starting from March 2003 AMD produced B3 revision Opterons that became the first Hammer CPUs to hit the market. And later this year AMD announced its Athlon 64 CPUs (and Athlon 64 FX) based on C0 revision chips. This is pretty much where this story starts.

## 1. Model number (rating)

First of all, we need to figure out how AMD model number is calculated for the K8 family. CPU name is being programmed by the BIOS during POST; it’s not fused in the CPU. If you check the [Revision Guide for AMD Athlon 64 and AMD Opteron Processors](#), you’ll see that, first, the BIOS checks BrandId to figure out the CPU family name (Athlon 64, Athlon 64 FX, Opteron) and its model number formula.

**Table 3. Processor Name String Table**

| BrandTable Index[5:0] | Name String                                    | Notes | Description                                    |
|-----------------------|------------------------------------------------|-------|------------------------------------------------|
| 00h                   | AMD Engineering Sample                         | -     | Reserved                                       |
| 04h                   | AMD Athlon(tm) 64 Processor XX00+              | 1     | Desktop/DTR Client                             |
| 05h                   | AMD Athlon(tm) 64 X2 Dual Core Processor XX00+ | 1     | Dual Core Client                               |
| 08h                   | Mobile AMD Athlon(tm) 64 Processor XX00+       | 1     | Mobile Client                                  |
| 09h                   | Mobile AMD Athlon(tm) 64 Processor XX00+       | 1     | Mobile Client<br>Low Power Mobile VIDs         |
| 0Ah                   | AMD Turion(tm) 64 Mobile Technology ML-XX      | 1     | UP Client LPM 35W                              |
| 0Bh                   | AMD Turion(tm) 64 Mobile Technology MT-XX      | 1     | UP Client LPM 25W                              |
| 0Ch                   | AMD Opteron(tm) Processor 1YY                  | 2     | UP Server                                      |
| 0Dh                   | AMD Opteron(tm) Processor 1YY                  | 2     | UP Server                                      |
| 0Eh                   | AMD Opteron(tm) Processor 1YY HE               | 2     | UP Server Low Power                            |
| 0Fh                   | AMD Opteron(tm) Processor 1YY EE               | 2     | UP Server Low Power                            |
| 10h                   | AMD Opteron(tm) Processor 2YY                  | 2     | DP Server                                      |
| 11h                   | AMD Opteron(tm) Processor 2YY                  | 2     | DP Server                                      |
| 12h                   | AMD Opteron(tm) Processor 2YY HE               | 2     | DP Server Low Power                            |
| 13h                   | AMD Opteron(tm) Processor 2YY EE               | 2     | DP Server Low Power                            |
| 14h                   | AMD Opteron(tm) Processor 8YY                  | 2     | MP Server                                      |
| 15h                   | AMD Opteron(tm) Processor 8YY                  | 2     | MP Server                                      |
| 16h                   | AMD Opteron(tm) Processor 8YY HE               | 2     | MP Server Low Power                            |
| 17h                   | AMD Opteron(tm) Processor 8YY EE               | 2     | MP Server Low Power                            |
| 18h                   | AMD Athlon(tm) 64 Processor EE00+              | 6     | UP Client                                      |
| 1Dh                   | Mobile AMD Athlon(tm) XP-M Processor XX00+     | 1     | Mobile Client, 32-Bit                          |
| 1Eh                   | Mobile AMD Athlon(tm) XP-M Processor XX00+     | 1     | Mobile Client, 32-Bit<br>Low Power Mobile VIDs |
| 20h                   | AMD Athlon(tm) XP Processor XX00+              | 1     | Desktop/DTR Client 32-Bit                      |
| 21h                   | Mobile AMD Sempron(tm) Processor TT00+         | 4     | Mobile Client, 32-bit                          |
| 22h                   | AMD Sempron(tm) Processor TT00+                | 4     | Desktop/DTR Client, 32-bit                     |
| 23h                   | Mobile AMD Sempron(tm) Processor TT00+         | 4     | Mobile Client, 32-bit<br>Low Power Mobile VIDs |
| 24h                   | AMD Athlon(tm) 64 FX-ZZ Processor              | 3     | Desktop Client                                 |
| 26h                   | AMD Sempron(tm) Processor TT00+                | 4     | Desktop/DTR Client, 64-bit                     |

Then we need to calculate the model number.

**Table 4. Model Number Calculation**

| # | Note                                                                                                                                                                      |
|---|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | $XX = 22 + NN$ . For example, 000001b stands for "23", 111111b stands for "85".                                                                                           |
| 2 | $YY = 38 + (2 * NN)$ . Defined for NN from 000001b to 011110b. Reserved for NN from 011111b to 111111b. For example, 000001b stands for "40" and 011110b stands for "98". |
| 3 | $ZZ = 24 + NN$ . Defined for NN from 000001b to 111111b. For example, 000001b stands for "25" and 111111b stands for "87".                                                |
| 4 | $TT = 24 + NN$ . Defined for NN from 000001b to 111111b. For example, 000001b stands for "25" and 111111b stands for "87".                                                |

As you can see, the model number is calculated using part of BrandId value to determine the CPU family and corresponding formula. The other part is then used for the PR calculation. For example, a regular Athlon 64 3200+ will have BrandId of 04h and  $XX = 0A$  hex = 10 dec. Using the formula in Table 4, row 1, we find that  $XX = 22 + 10 = 32$ . So the overall CPU name will be Athlon 64 3200+. This is what the BIOS will program as the CPU name.

## 1.1 Unrated samples

From Table 3 above, you can see that CPUs with BrandId = 0 should be identified as "AMD Engineering Sample." However, there's another case mentioned in a note for Table 4 (Model Number Calculation):

**All of the following model codes are expressed in decimal. NN is defined by Table 2 on page 9. If NN=0 then the name string is "AMD Engineering Sample".**

This is another type of ES that has BrandId labeled correctly but NN=0. It is pretty much an AMD equivalent for Intel's "CPU 0000" ES. Unfortunately, most boards ignore this note and program a model number using NN=0 as a correct value (which is incorrect).

What do we get then?

We'll have the following awkward names (by row number in Table 4):

- 1) Athlon 64/Mobile Athlon 64 2200+
- 2) Opteron 138/238/838
- 3) Athlon 64 FX-24
- 4) Sempron/Mobile Sempron 2400+

We've seen some of these names and categories on HWBot; now we know they're all wrong. These are simply ES counterparts of other existing SKUs. We can estimate which ones exactly by stock frequency and L2 cache size given that the BrandId is correct.

## 1.2 Rating change

Another interesting story is the so-called "misrated CPUs"—they have one model number engraved on the IHS but software detects a different model number. One might think, "Why do such a dumb thing—write one model number on the CPU and a different one inside the

core registers?"

But what if they weren't mismatched at all?

There were three such CPUs with a total of 5 OPN:

Athlon 64 2800+ (ADAAA2800ACN5)

Athlon 64 3100+ (ADA3100AEP5AJ/ADA3100AEP5AO)

Athlon 64 3400+ (ADA3400AEP5AJ/ADA3400AEP5AO)

|                                                                                                      |                                                                                      |                                                                |                                                      |
|------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|----------------------------------------------------------------|------------------------------------------------------|
|                                                                                                      | Athlon 64<br>1MB L2<br>3400+/3100+/<br>2800+                                         | Athlon 64<br>1MB L2<br>3700+/3400+                             | Athlon 64<br>1MB L2<br>4000+/3700+                   |
|                                                                                                      |                                                                                      | Athlon 64 Paris<br>256KB L2<br>3200+                           | Athlon 64 Paris<br>256KB L2<br>3500+/3200+           |
| Athlon XP"Barton"<br>FSB333<br>3000+/2800+/2500+                                                     | Athlon XP"Barton"<br>FSB333<br>3000+/2800+/<br>2500+                                 | Athlon XP"Barton"<br>FSB333<br>3200+/3000+/<br>2800+/2500+     | Athlon XP"Barton"<br>FSB333<br>3200+/3000+/<br>2800+ |
| Athlon XP<br>"Thoroughbred"<br>FSB333<br>2700+/2600+                                                 | Athlon XP<br>"Thoroughbred"<br>FSB333<br>2700+/2600+                                 | Athlon XP<br>"Thoroughbred"<br>FSB333<br>2700+/2600+           | Athlon XP<br>"Thoroughbred"<br>FSB333<br>2600+       |
| Athlon XP<br>"Thoroughbred"<br>FSB266<br>2600+/2400+/<br>2200+/2100+/<br>2000+/1900+/<br>1800+/1700+ | Athlon XP<br>"Thoroughbred"<br>FSB266<br>2600+/2400+/<br>2200+/2100+/<br>2000+/1900+ | Athlon XP<br>"Thoroughbred"<br>FSB266<br>2400+/2200+/<br>2000+ | Athlon XP<br>"Thoroughbred"<br>FSB266<br>2400+/2200+ |
| Q1'03                                                                                                | Q2'03                                                                                | Q3'03                                                          | Q4'03                                                |

Roadmap dated around 17.01.2002

## CPUs

The Athlon 64 2800+ was based on revision B0 and was produced mostly 48-51 weeks of 2002 (25 November - 22 December).

Athlon 64 3100+ and 3400+ were based on release revision C0 and were produced during 18-26 weeks of 2003 (28 April - 29 June).

## Tests

On 10 July, 2003, a member named **I Love Fang** from Taiwanese PCDDVD forum posted tests of a pre-release Athlon 64 3400+ which were reposted by the Chinese website [E04hardware](#). We can see screenshots of CPU-Z showing the CPU detected by its old rating.

On 1 September 2003, [OCworkbench](#) published a review of an Athlon 3100+. Given the specs, it is most likely an ADA3100AEP5AJ (or ADA3100AEP5AO). Additionally, they mentioned that on another board, the CPU is detected as 2900+ (new rating system).

## New rating

On 5 August, 2003, [Planet 3DNow!](#) posted a change in the AMD model rating system retiring the old line of 2800+/3100+/3400+ and announcing that socket 754 will start from the Athlon 3200+ clocked at 2.0 GHz.

If we take another look at Table 4 above, we can see that the first (Athlon 64 and Mobile Athlon 64) category adds 22 to NN to calculate the model number. Since we know the rating was lowered by 200 points, the formula before added 24. This is similar to rows 3 (Athlon 64 FX) and 4 (AMD Sempron and Mobile AMD Sempron) which remained intact, serving as another sign of a rating change.

If you want to calculate the model number from CPU frequency, the [old formula](#) (for socket 754 Athlon 64) looked like this:

**Model number = CPU frequency x 1.5 + 400.**

So for a Clawhammer 1800MHz it would transfer to  $1800 * 1.5 + 400 = 3100$ .

For Clawhammer 2000MHz it would be  $2000 * 1.5 + 400 = 3400$ .

And for the slowest Clawhammer 1600MHz it's like  $1600 * 1.5 + 400 = 2800$ . This matches the pre-production lineup of Athlon 64 model numbers.

After the rating changed, it is as follows:

**Model number = CPU frequency x 1.5 + 200.**

Hence, we have a model number that is 200 lower.

The BIOS calculates (and programs the CPU name string) differently, as mentioned above.

It is worth mentioning that AMD claimed no such formula existed and model numbers were based solely on tests.

## 1.3 Yet another rating change

This one was hidden much deeper than socket 754. A user, ~~¥The\_One¥~~, has asked about his CPU—a socket 939 Athlon 3600+ based on the Clawhammer core—that is absent from all databases. With a CPU-Z screenshot and some luck from Google, I've managed to find out the following:

During CES 2004, which took place in January, 2004, the following information was collected and compiled: socket 939 was to be announced on 29 March, 2004, and was expected to consist of the AMD Athlon 64 FX-53 (socket 939), Athlon 64 3400+ and 3700+ (Newcastle, with 512KB L2 cache and clocked at 2.2GHz and 2.4GHz respectively). It turns out that another CPU was sampled—Athlon 64 3600+ with 1MB L2 cache and 2.2GHz, which had just a 1x lower multiplier than the FX-53. This CPU would fill the gap between 3400+ and 3700+.

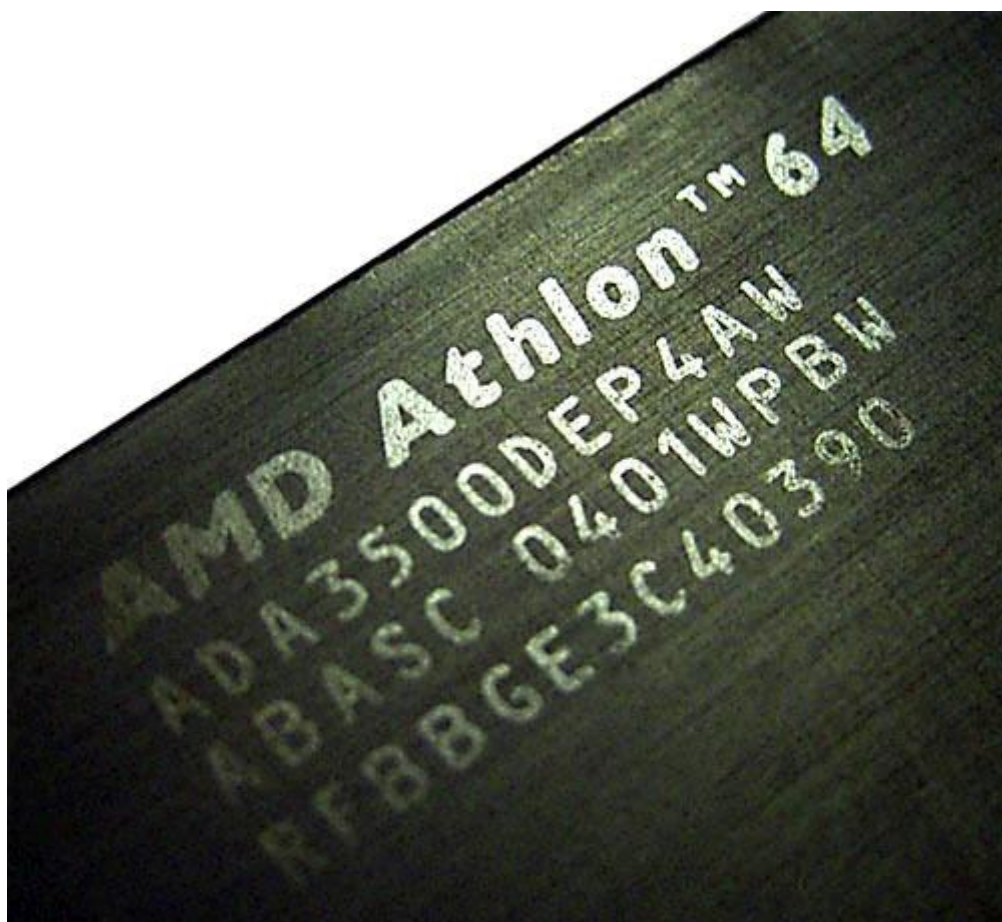
|                          | Q1 2004           | Q2 2004                                                                          | Q3 2004                                     | Q4 2004                                                                          | 2005                              |
|--------------------------|-------------------|----------------------------------------------------------------------------------|---------------------------------------------|----------------------------------------------------------------------------------|-----------------------------------|
| Opteron<br>(940pin)      |                   | SledgeHammer : 130nm, 1MB<br>850 (2.4Ghz)<br>250 (2.4Ghz)<br>150 (2.4Ghz)        |                                             | Athens/Troy/Venus : 90nm, 1MB<br>852 (2.6Ghz)<br>252 (2.6Ghz)<br>152 (2.6Ghz)    | Egypt/Italy/<br>Denmark :<br>90nm |
| Athlon 64 FX<br>(940pin) | FX-53<br>(2.4Ghz) |                                                                                  |                                             |                                                                                  |                                   |
| Athlon 64 FX<br>(939pin) |                   | ClawHammer : 130nm, 1MB<br>FX-53 (2.4Ghz)                                        |                                             | San Diego : 90nm, 1MB<br>FX-55 (2.6Ghz)                                          | Toledo :<br>90nm                  |
| Athlon 64<br>(939pin)    |                   | Newcastle : 130nm, 512KB<br>Athlon 64 3700+ (2.4Ghz)<br>Athlon 64 3400+ (2.2Ghz) |                                             | Winchester : 90nm, 512KB<br>Athlon 64 4000+ (2.6Ghz)<br>Athlon 64 3700+ (2.4Ghz) |                                   |
| Athlon 64<br>(754pin)    |                   | Athlon 64 3700+ (2.4Ghz, 1MB)<br>Athlon 64 3400+ (2.2Ghz, 512KB)                 |                                             |                                                                                  |                                   |
| Athlon XP<br>(754pin)    |                   |                                                                                  | Paris : 130nm SOI, 256KB<br>Athlon XP 2800+ | Athlon XP 3000+                                                                  | Palermo :<br>90nm SOI             |



CPU photo taken by ¥The\_One¥



These CPUs have been sampled starting from 0344 up until 0352 (all the way to the end of 2003), whereas CPUs with the model numbers we know have been sampled starting from 0401 (the very beginning of 2004). By the time of CES 2004 AMD had already altered their rating once again. Socket 939 was eventually launched on 1 June, 2004.



Another interesting detail is that, despite having a Newcastle OPN, the older rating CPUs use a Clawhammer stepping, meaning they have a Clawhammer core. The most logical reason for this is that AMD had to sample socket 939 Newcastle CPUs for validation and testing (to vendors) but didn't have enough real working Newcastle cores. So, they took their good old Clawhammer core (the first core ever), disabled half its cache, and fused it to be recognized as a Newcastle CPU. Given that this was mostly seen on early samples obviously used for testing and validation, I would call them 'prototypes.'

## 2. CPU

The initial goal of this research was simply to figure out how cores relate to their CPUID values. It turns out they have a very different approach from Intel. But then this work got out of control and turned into something much bigger.

So where do we start when we see such a table in CPU-Z?

|             |   |            |    |          |       |
|-------------|---|------------|----|----------|-------|
| Family      | F | Model      | F  | Stepping | 2     |
| Ext. Family | F | Ext. Model | 2F | Revision | DH-E6 |

AMD Athlon 64 and Opteron are known as AMD Family 0Fh processors. Therefore, for all CPUs discussed in this article, the Family (and Ext. Family) will always be "F".

Now let's take a look at the Revision. It consists of two parts. The first one could be called “core configuration” because it estimates the physical core count and L2 cache volume. “Physical” refers to cores and cache that are implemented in a certain die, not those that are available (doesn't care if cores or cache have been disabled for a certain model).

**Table 1. Core configuration**

|    |                   |
|----|-------------------|
| SH | Single core 1MB   |
| DH | Single core 512KB |
| CH | Single core 256KB |
| BH | Dual core 2*512KB |
| JH | Dual core 2*1MB   |

This is where you should start to see something unusual, but let's go further. The second part consists of a letter which can be considered a “tier” or “generation” and a number that serves as an index.

**Table 2. Core configuration/revision**

| Revision | C  | D0 (no other indexes are known) | E  |
|----------|----|---------------------------------|----|
|          | SH | SH                              | SH |
|          | DH | DH                              | DH |
|          | CH |                                 | BH |
|          |    |                                 | JH |

At this point, there are already two questions that should come to mind for anyone who knows the K8 family good enough:

- Were there cores with physical 256KB L2 cache?
- What is SH-D0?

## 2.1 On the rocky road to Dublin

As everyone knows, Athlon 64 did cost a lot at launch. The main reasons for this were the very large die size of 193mm<sup>2</sup>, which was 2.5x times bigger than the Thoroughbred, and problems with SOI technology, which resulted in low yields and several release delays. They ended up being significantly faster than their counterparts, so this time AMD didn't have to start price wars; however, the high price tag resulted in moderate sales. They released an Athlon 64 3000+ with 512KB of cache so they could reuse some faulty Clawhammer chips by disabling half of their cache. But they needed something to create a cheaper solution for both production and end users.

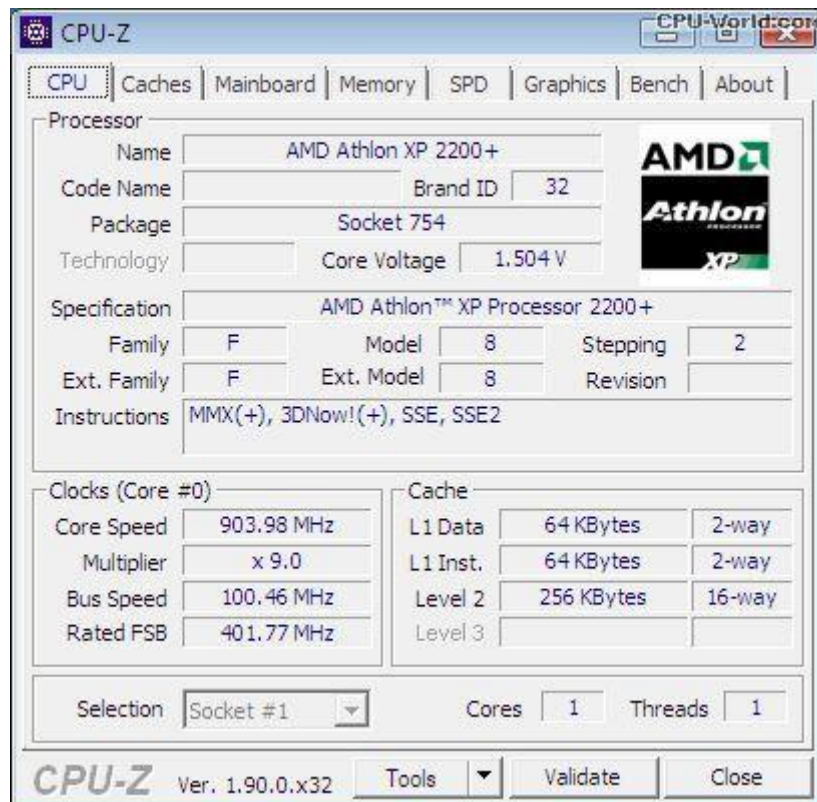
It all started with Newcastle. Around 5 November, 2003, [news](#) came out about a new Athlon 64 core—Newcastle—that intended to bring a cheaper 512KB core to the market. We also read about a familiar core, Paris, which has less cache and doesn't support the AMD64 instruction set. They were rumored to come out in Q2 2004, with the Paris core in Q4 2004, which we later came to know as AMD Sempron. Newcastle was announced on 17 April, 2004, and had a die size of 144mm<sup>2</sup> with a physical 512KB of L2 cache and DH-CG core (512KB, CG revision), opening the way to produce cheaper CPUs with a lower defect rate.

Furthermore, AMD [wanted](#) to release a crippled version of the Athlon 64 without 64-bit mode and with only 256KB L2 cache.

Even more, some samples have been produced.



This sample was based on the Clawhammer core (as indicated by the AAAIC stepping code) but the OPN points to Dublin (so it was meant to be Dublin). This is the same “prototype” case mentioned in Chapter 1.3.



Mind the 9x multiplier, which means an 1800MHz frequency and a 3200+ rating (without an 64) on the IHS. And the 2200+ rating indicates that this sample is an “unrated” one. The F82 CPUID is the same as the one used for Mobile Sempron and Mobile Athlon XP-M Dublin cores. Only the 32 BrandId corresponds to the “Athlon XP” brand from the AMD revision guide.

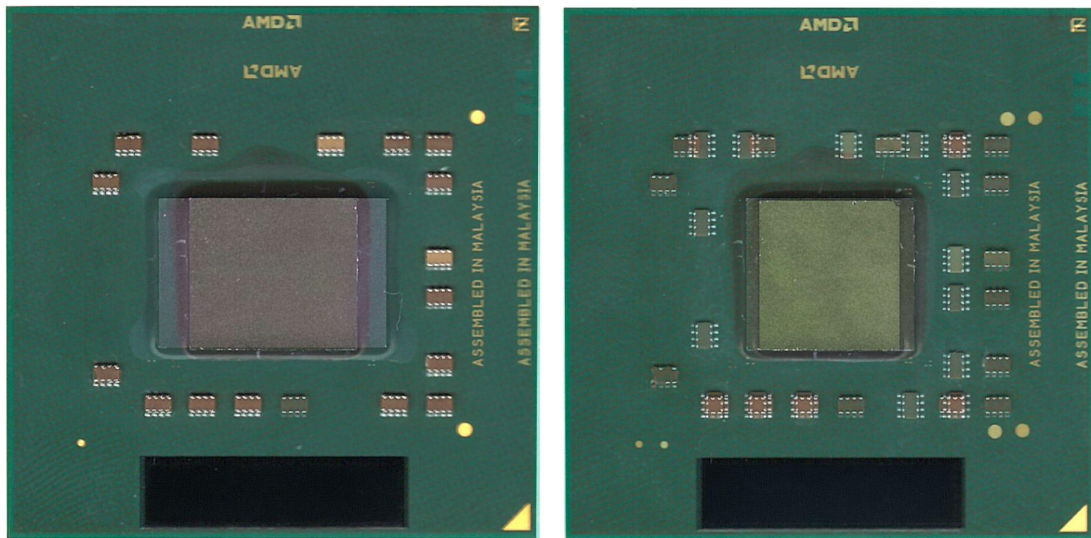
Source: [CPU world](#).

This news appeared on 3 October, 2003. A bit later, on 3 March, 2004, a [roadmap was published](#) revealing the lineup of Athlon XP s754 to be released around Q4 2004 to Q1 2005. And it was long before AMD Sempron became a thing, which had only been [rumored](#) on 7 June, 2004.

AMD even [planned](#) to make a socket 939 Athlon XP based on the Paris core, which we would later know as Sempron. After all, AMD abandoned the idea of Athlon XP on s754 and s939 based on the Dublin core and announced Sempron processors for their value segment. The first Sempron CPUs were based on the Paris core (which is a Newcastle die with partly disabled cache and no 64-bit capabilities). This seemed like the end of the Dublin idea, but not in the mobile market.

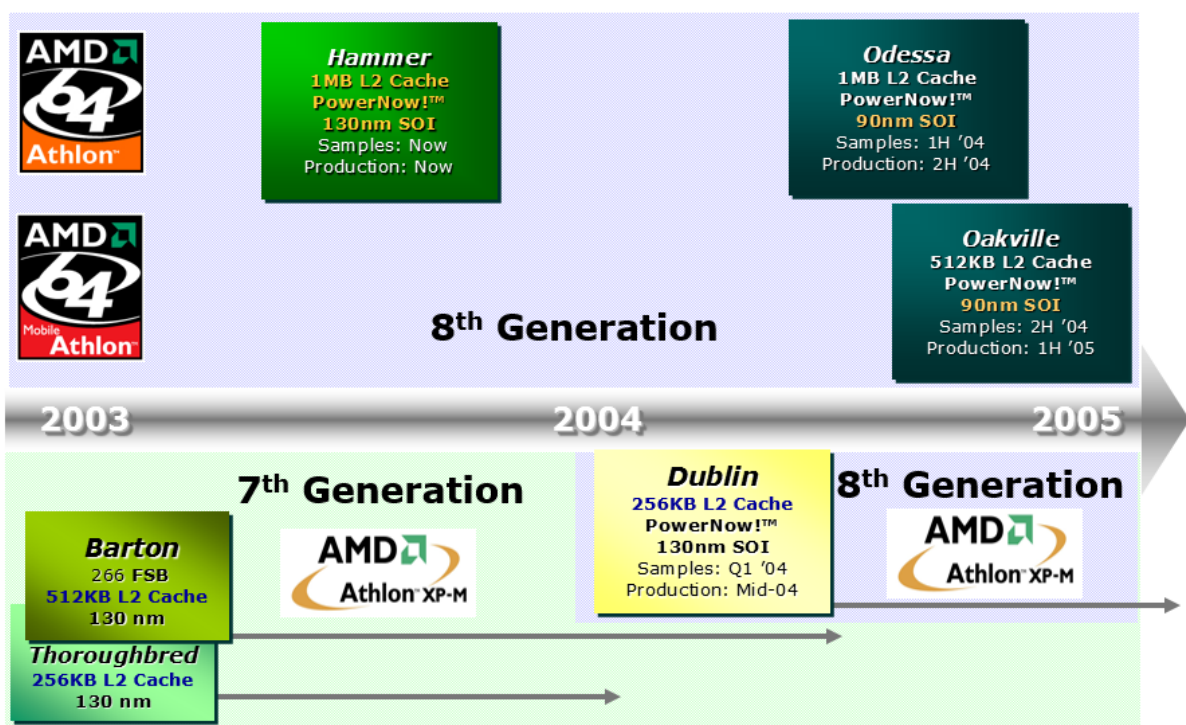
On 1 April, 2004, a [news](#) article popped up about laptops based on the K8 XP-M which was concluded to be Dublin. So, what does a Dublin core look like? On the left, you can see a Newcastle core over a Clawhammer core (144mm<sup>2</sup> vs 193mm<sup>2</sup>), and on the right is a Dublin core over a Newcastle core (132mm<sup>2</sup> vs 144mm<sup>2</sup>). As you can see, the size difference between Clawhammer and Newcastle is much larger than that between a Newcastle and a

Dublin core (25% vs 8%). The smaller size difference is probably one of the reasons why it didn't become massive.



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So, the K8 XP-M CPUs were produced using three cores: Clawhammer (suffix AR), Newcastle (AX) and Dublin (AY). Despite common assumptions, only one of these was the real Dublin core, which had a physical 256KB L2 cache in its die. K8 XP-M CPUs with the Dublin core were produced from the 9th week of 2004 to the beginning of 2005. Later, they were made only with Newcastle and Clawhammer cores (probably defective leftovers). Additionally, the first Mobile Semprons were produced using this core, with a lower TDP, which we will address a bit later.

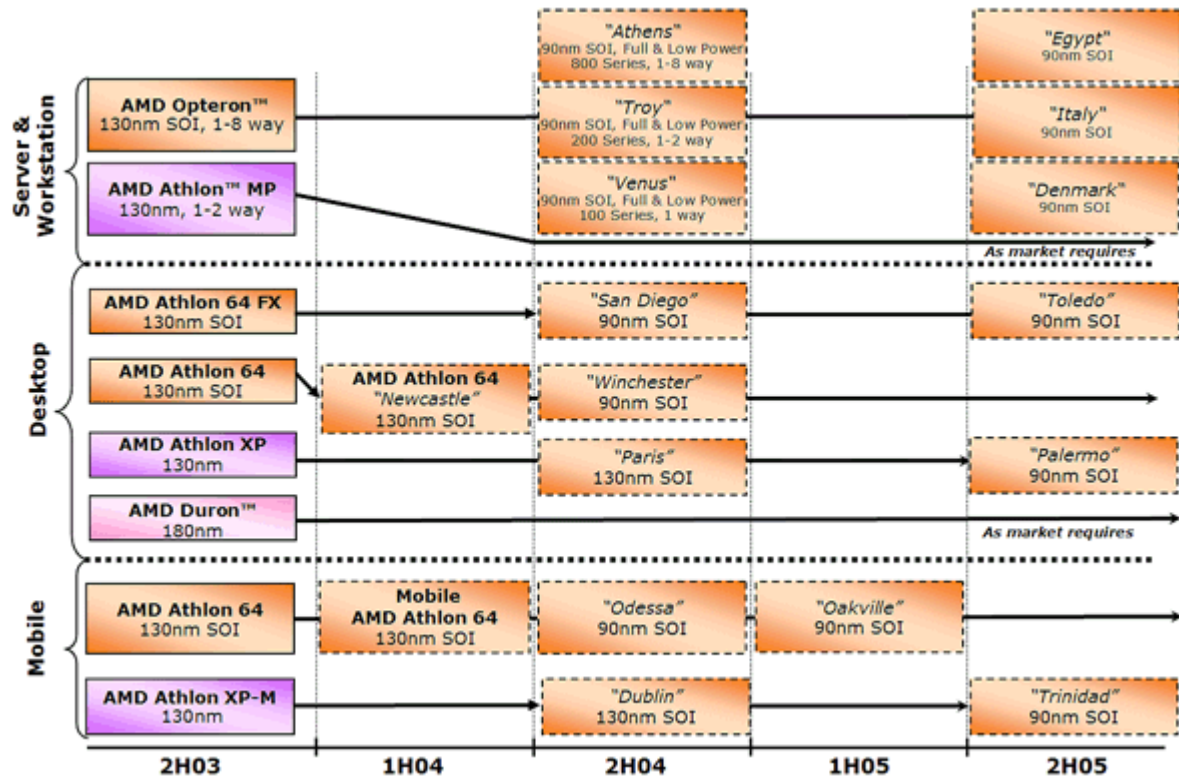


| <i>Mobile Transportable</i> | Q4 '03 | Q1 '04 | Q2 '04 | Q3 '04 | Q4 '04 |
|-----------------------------|--------|--------|--------|--------|--------|
| <b>Mainstream 3</b>         | 3000+  | 3200+  | 3400+  | 3400+  | 3700+  |
| <b>Mainstream 2</b>         | 2800+  | 3000+  | 3200+  | 3200+  | 3400+  |
| <b>Mainstream 1</b>         |        | 2800+  | 3000+  | 3000+  | 3200+  |
| <b>Value 3</b>              |        |        |        | 3000+  | 3200+  |
| <b>Value 2</b>              |        |        |        |        | 3000+  |
| <b>Value 1</b>              |        |        |        |        |        |

62W Mobile Athlon™ 64  
 'Hammer' & 'Odessa'  
 754-pin Package

62W Athlon™ XP-M  
 'Dublin'  
 754-pin Package

Lastly, if you refer to the [Revision Guide for AMD Athlon 64 and AMD Opteron Processors](#), you'll find that there were plans for the CH-CG core (Dublin) for socket 939 as an Athlon 64, which was never released. Along with the CH-D0 (90nm SOI version of Dublin) core, which appeared in the roadmap as "Trinidad", it never came out for either socket 754 or 939.

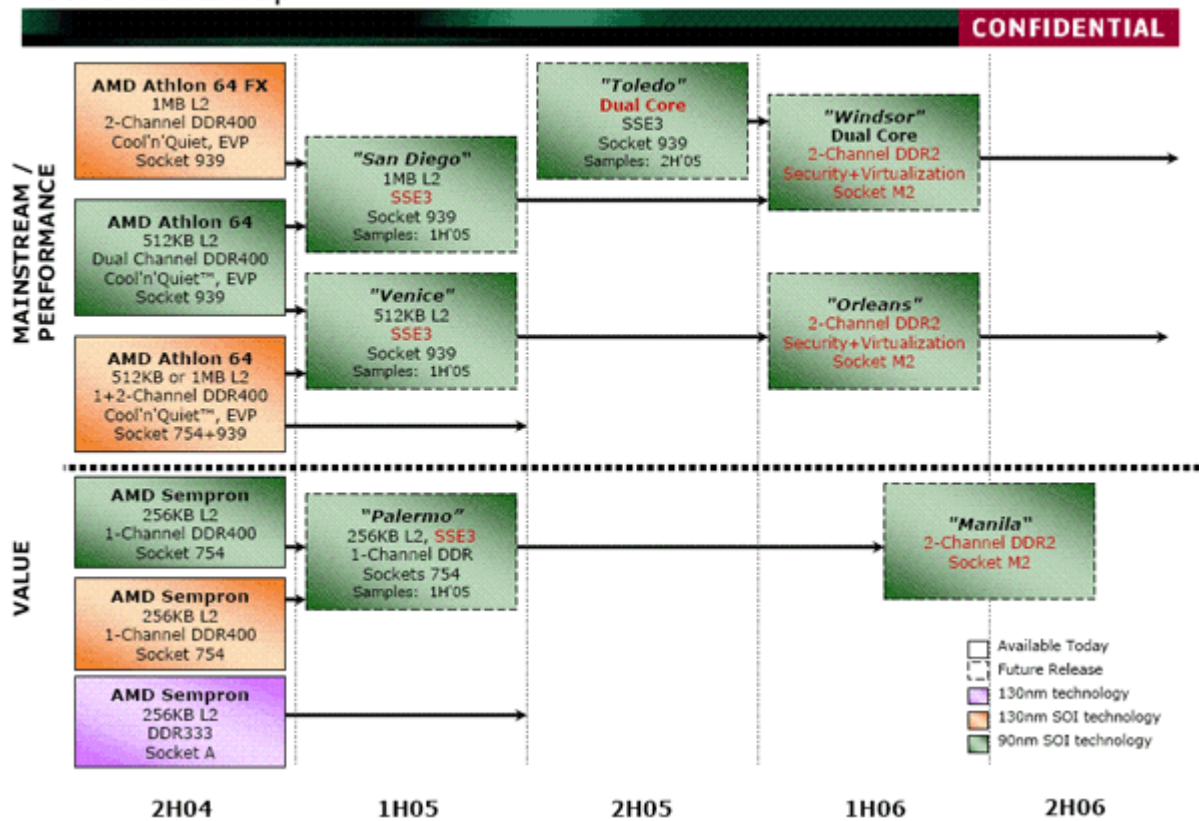


That is all for Dublin, probably the most unacknowledged core sold in the K8 family.

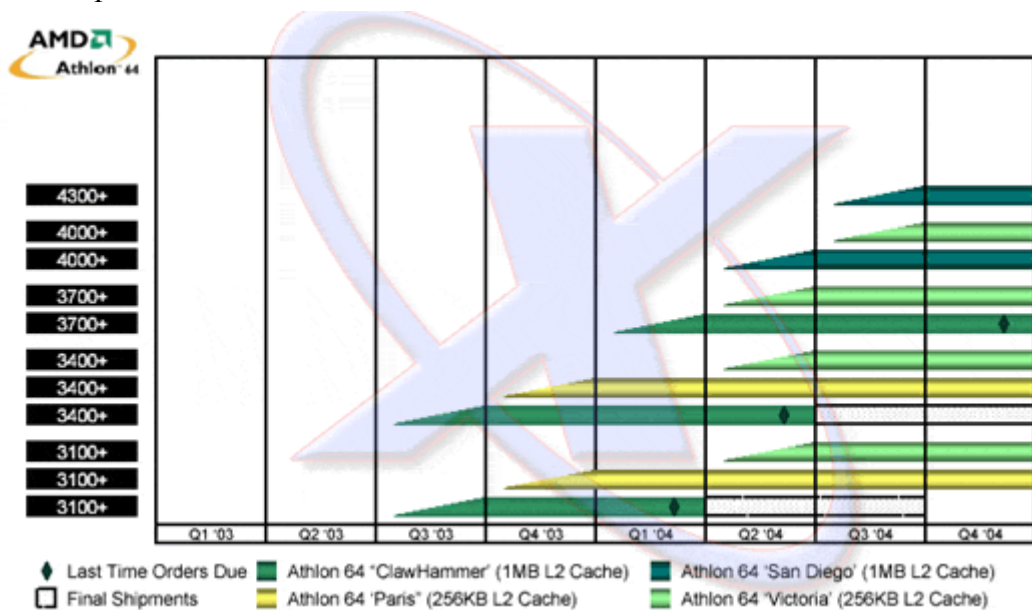
## 2.2 Victoria

We all know what happened after CG revision: AMD transitioned to the 90nm SOI technological process which is primarily known by its Winchester core. But what if I told you that there are a bunch more D0 revision cores? Let's get back to the Sempron family, which started with the Paris core (Newcastle with a partly disabled L2 cache). Later, CPUs known as "Palermo-D0" were produced. So, let's take a look at another roadmap.

## Core Roadmap



We can see SSE3 support announced for the Palermo core. However, SSE3 appeared only in revision E of the K8 family. This can mean only one thing: whatever a Sempron D0 revision is, it's definitely not a Palermo. So let's check some old news on [Xbitlabs](#) and [x86-secret](#) to figure out that there was a 90nm successor to the Paris core codenamed "Victoria". There's also a roadmap that identifies Victoria as a 256KB L2 cache CPU.



I suppose that, due to the very short lifetime of D0 revision in general, it has been forgotten. Yet, there are certain differences between both Victoria and Paris (90nm vs. 130nm) and Palermo and Victoria (SSE3 support vs. lack thereof), which clearly separate it from the other two.

## 2.3 SH-D0

We all know what the D0 revision is. It's the Winchester core. However, SH-D0 assumes we're talking about a CPU with 1MB L2 cache and 90nm SOI, but not E4, which refers to the San Diego (and its server/mobile modifications). Revision D0 was a rather short-lived transition from 130nm CG revision to the E revision. Yet, AMD did leave some traces. From the Abit AV8 BIOS update, we can find out that a D0 revision of FX-55 had been sampled.

A screenshot of a BIOS update interface. It shows the BIOS file name as 'av816.exe' with a link to the mirror site. The mirror site is listed as 'ASIA Europe US'. The BIOS ID is '16'. There are two notes: '1. Enhanced compatibility with D0 stepping FX-55 and 3200+ CPUs.' and '2. BIOS compile date: 10/12/2004'. The BIOS issue date is '2004/10/12'.

BIOS: [av816.exe](#) Bios Issue Date: 2004/10/12  
Mirror Site: [ASIA](#) [Europe](#) [US](#)  
BIOS ID: 16  
1. Enhanced compatibility with D0 stepping FX-55 and 3200+ CPUs.  
2. BIOS compile date: 10/12/2004

But were there any CPUs that actually hit the market? Well, it turns out there are a few. To be precise, only two SKUs are known: Opteron [OSA246FIK5BC](#) and [OSA248FIK5BC](#). There were tables from AMD that suggest more OPNs had this revision, but no evidence of their existence have been found (probably paper releases or very limited quantities).

|                               |     |         |       |          |      |     |                |    |        |
|-------------------------------|-----|---------|-------|----------|------|-----|----------------|----|--------|
| <a href="#">OSA146FIK5BB</a>  | 146 | 2.0GHz  | 67w   | 800 MHz  | 1 MB | 940 | .09 micron SOI | D4 | 2.0GHz |
| <a href="#">OSA246FIK5BC7</a> | 246 | 2.0GHz  | 67w   | 800 MHz  | 1 MB | 940 | .09 micron SOI | D4 | 2.0GHz |
| <a href="#">OSA248FIK5BC</a>  | 248 | 2.2GHz  | 67w   | 800 MHz  | 1 MB | 940 | .09 micron SOI | D4 | 2.2GHz |
| <a href="#">OSA846FIK5BD</a>  | 846 | 2.0GHz  | 67w   | 800 MHz  | 1 MB | 940 | .09 micron SOI | D4 | 2.0GHz |
| <a href="#">OSA242BLBOX</a>   | 242 | 1.6GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.6GHz |
| <a href="#">OSA242BLWOF</a>   | 242 | 1.6GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.6GHz |
| <a href="#">OSA242FAA5BL</a>  | 242 | 1.6GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.6GHz |
| <a href="#">OSA244BLBOX</a>   | 244 | 1.8GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.8GHz |
| <a href="#">OSA244BLWOF</a>   | 244 | 1.8GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.8GHz |
| <a href="#">OSA244FAA5BL</a>  | 244 | 1.8GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.8GHz |
| <a href="#">OSA246BLBOX</a>   | 246 | 2.0GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.0GHz |
| <a href="#">OSA246BLWOF</a>   | 246 | 2.0GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.0GHz |
| <a href="#">OSA246FAA5BL</a>  | 246 | 2.0GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.0GHz |
| <a href="#">OSA248BLBOX</a>   | 248 | 2.2GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.2GHz |
| <a href="#">OSA248BLWOF</a>   | 248 | 2.2GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.2GHz |
| <a href="#">OSA248FAA5BL</a>  | 248 | 2.2GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.2GHz |
| <a href="#">OSA250BLBOX</a>   | 250 | 2.4GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.4GHz |
| <a href="#">OSA250BLWOF</a>   | 250 | 2.4GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.4GHz |
| <a href="#">OSA250FAA5BL</a>  | 250 | 2.4GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.4GHz |
| <a href="#">OSA252BLBOX</a>   | 252 | 2.6 GHz | 92.6w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.6GHz |
| <a href="#">OSA252BLWOF</a>   | 252 | 2.6 GHz | 92.6w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.6GHz |
| <a href="#">OSA252FAA5BL</a>  | 252 | 2.6 GHz | 92.6w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.6GHz |
| <a href="#">OSA842BMWOF</a>   | 842 | 1.6GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.6GHz |
| <a href="#">OSA842FAA5BM</a>  | 842 | 1.6GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.6GHz |
| <a href="#">OSA844BMWOF</a>   | 844 | 1.8GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.8GHz |
| <a href="#">OSA844FAA5BM</a>  | 844 | 1.8GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 1.8GHz |
| <a href="#">OSA846BMWOF</a>   | 846 | 2.0GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.0GHz |
| <a href="#">OSA846FAA5BM</a>  | 846 | 2.0GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.0GHz |
| <a href="#">OSA848BMWOF</a>   | 848 | 2.2GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.2GHz |
| <a href="#">OSA848FAA5BM</a>  | 848 | 2.2GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.2GHz |
| <a href="#">OSA850BMWOF</a>   | 850 | 2.4GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.4GHz |
| <a href="#">OSA850FAA5BM</a>  | 850 | 2.4GHz  | 85.3w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.4GHz |
| <a href="#">OSA852BMWOF</a>   | 852 | 2.6 GHz | 92.6w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.6GHz |
| <a href="#">OSA852FAA5BM</a>  | 852 | 2.6 GHz | 92.6w | 1000 MHz | 1 MB | 940 | .09 micron SOI | E4 | 2.6GHz |

The claimed D4 revision doesn't align with the AMD revision guide, so it's probably a typo in this table. Although the suffixes are correct (which will be addressed later).

But what about revision E? Well, from a core configuration/revision point of view, everything seems easy and well-known: SH-E4 (San Diego), DH-E3/6 (Venice/Palermo), BH-E4

(Manchester), JH-E6 (Toledo), along with their server and mobile variations. So let's once again dive deeper and check out CPUID model and extended model values.

## 2.4 CPUID model and extended model

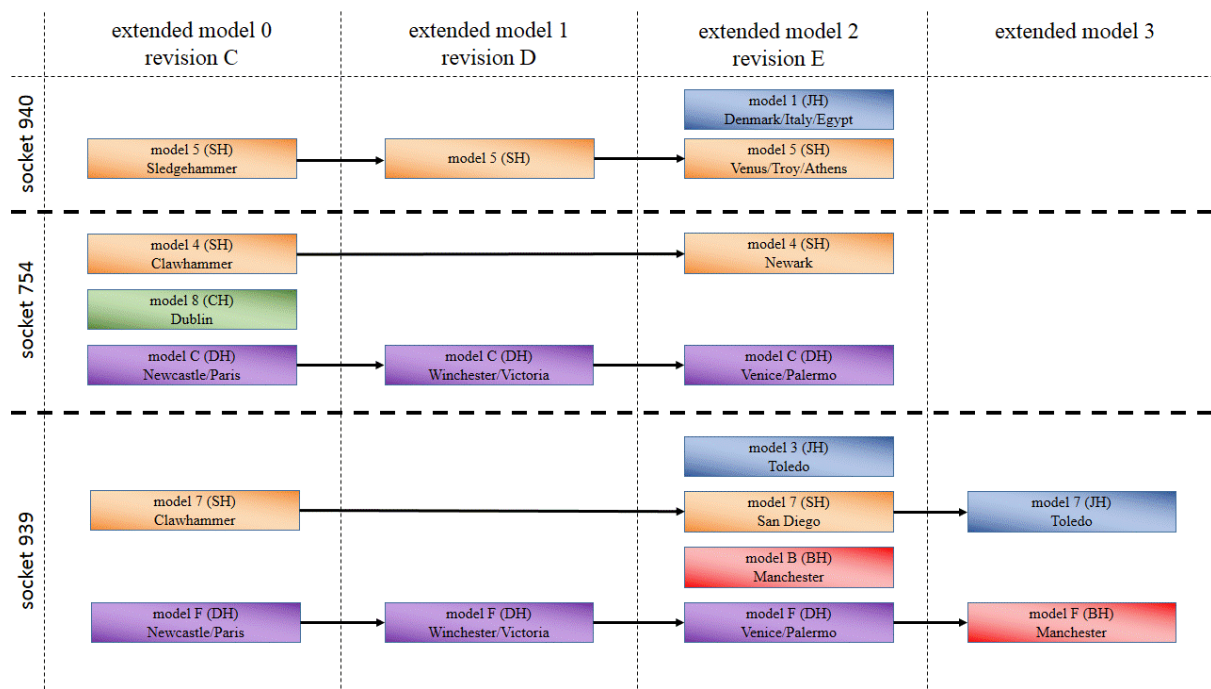
The CPUID model number in the AMD K8 family is quite different from those of the previous K5, K6 and K7 generations. It encodes both the core configuration and the socket.

|            | core configuration | model number dec | model number bin |            |
|------------|--------------------|------------------|------------------|------------|
| socket 940 | JH                 | 1                | 00 01            | socket 940 |
|            | SH                 | 5                | 01 01            |            |
| socket 754 | SH                 | 4                | 01 00            | socket 754 |
|            | CH                 | 8                | 10 00            |            |
|            | DH                 | C                | 11 00            |            |
| socket 939 | JH                 | 3                | 00 11            | socket 939 |
|            | SH                 | 7                | 01 11            |            |
|            | BH                 | B                | 10 11            |            |
|            | DH                 | F                | 11 11            |            |

As you can see, the upper two bits represent the core configuration, whereas the lower two bits represent the socket. You might ask, "What was socket '10' supposed to be?" I assume it should be the Clawhammer-DP, which didn't hit the market.

The extended model, in turn, is a representation of tier or generation and aligns with the revision in all but one case. This one case is the same for both the model and the extended model.

To make things clearer, take a look at the following table I've compiled:



[link to full size](#)

## 2.5 single-core Toledo and Manchester

So, what are the CPUs with the extended model 3? Two of them, the Athlon 64 3200+ and 3500+, based on the Manchester core, are more well-known. These are dual-core dies with one core disabled. The other two are less known. An overclocker from HWBot.org contacted me, stating that CPU-Z recognized the single-core Toledo as a San Diego E6 (which, as we know, was only E4). Finding any good information about them yielded no results, so I had to do some research. It turned out there are two CPUs, ADA4000DKA5CF and ADA3700DKA5CF, identified as San Diego DH-E6. Let's take a look at the table:

|              | OPN           | CPUID | ext. model | revision |
|--------------|---------------|-------|------------|----------|
| Athlon 64 X2 | ADA4800DAA6CD | F32   | 23         | E6       |
| E6           | ADA4000DKA5CF | F72   | 37         | E6       |
| E4           | ADA4000DAA5BN | F71   | 27         | E4       |
| Venice E3    |               | FF0   | 2F         | E3       |
| Venice E6    |               | FF2   | 2F         | E6       |

First, the part number is different. This means that AMD had sold it as a different part (they sometimes sold CPUs with different cores under one part number).

Second, the CPUID is different, but this is because the revision is different.

And now for the (al)most interesting part - the extended model. For E4, it's 27, and for E6, it's 37. However, this is not the case for Venice; both E3 and E6 have the same 2F model. This

means it's the same core but with different revisions. For our 3700/4000+, there are different extended models.

Lastly, the most important aspect is stepping. The stepping code is like a silicon batch. Here are the stepping codes for several CPUs:

Athlon 64 X2 4800+ Toledo: ACBWE CCB2E CCBWE LCB9E LCBIE

Athlon 64 4000+ E6: CCBWE LCB9E LCBBE LCBIE

Athlon 64 4000+ E4: AABHE CABGE CABHE KAB1E KAB2E KAB3E KABYE KACAE

Summing this up: AMD produced a CPU with a different part number, a different extended model number and steppings that are the same as those of Toledo CPUs. This means that it indeed is a Toledo core.

Moreover, according to the AMD revision guide (where we unfortunately don't see our CPUs), if they were included, they'd be in the last line (same core as Toledo) but with their own CPUID (F72), indicating that their revision is JH-E6. JH stands for dual-core die.

| Revision | CPUID Function 1 EAX Value         |                                    |                                    |                                       |                                    |                                       |                                 |                                    |                               |                                   |                               |
|----------|------------------------------------|------------------------------------|------------------------------------|---------------------------------------|------------------------------------|---------------------------------------|---------------------------------|------------------------------------|-------------------------------|-----------------------------------|-------------------------------|
|          | AMD Opteron™ Processor             | Dual-Core AMD Opteron™ Processor   | AMD Athlon™ 64 Processor           | AMD Athlon™ 64 X2 Dual Core Processor | AMD Athlon™ 64 FX Processor        | AMD Athlon™ 64 FX Dual Core Processor | Mobile AMD Athlon™ 64 Processor | AMD Sempron™ Processor             | Mobile AMD Sempron™ Processor | Mobile AMD Athlon™ XP-M Processor | AMD Turion™ Mobile Technology |
| SH-D0    | 00010F50h (940)                    | N/A                                | 00010F40h (754)<br>00010F70h (939) | N/A                                   | 00010F50h (940)<br>00010F70h (939) | N/A                                   | 00010F40h (754)                 | N/A                                | N/A                           | 00010F40h (754)                   | N/A                           |
| DH-D0    | N/A                                | N/A                                | 00010FC0h (754)<br>00010FF0h (939) | N/A                                   | N/A                                | N/A                                   | 00010FC0h (754)                 | 00010FC0h (754)<br>00010FF0h (939) | 00010FC0h (754)               | 00010FC0h (754)                   | N/A                           |
| CH-D0    | N/A                                | N/A                                | 00010F80h (754)<br>00010FB0h (939) | N/A                                   | N/A                                | N/A                                   | 00010F80h (754)                 | N/A                                | 00010F80h (754)               | 00010F80h (754)                   | N/A                           |
| JH-E1    | N/A                                | 00020F10h (940)                    | N/A                                | N/A                                   | N/A                                | N/A                                   | N/A                             | N/A                                | N/A                           | N/A                               | N/A                           |
| DH-E3    | N/A                                | N/A                                | 00020FF0h (939)                    | N/A                                   | N/A                                | N/A                                   | N/A                             | 00020FF0h (939)<br>00020FC0h (754) | N/A                           | N/A                               | N/A                           |
| SH-E4    | 00020F51h (940)<br>00020F71h (939) | N/A                                | 00020F71h (939)                    | N/A                                   | 00020F71h (939)                    | N/A                                   | N/A                             | N/A                                | N/A                           | N/A                               | N/A                           |
| BH-E4    | N/A                                | N/A                                | N/A                                | 00020FB1h (939)                       | N/A                                | N/A                                   | N/A                             | N/A                                | N/A                           | N/A                               | N/A                           |
| SH-E5    | N/A                                | N/A                                | N/A                                | N/A                                   | N/A                                | N/A                                   | 00020F42h (754)                 | N/A                                | N/A                           | N/A                               | 00020F42h (754)               |
| DH-E6    | N/A                                | N/A                                | 00020FF2h (939)                    | N/A                                   | N/A                                | N/A                                   | N/A                             | 00020FF2h (939)<br>00020FC2h (754) | 00020FC2h (754)               | N/A                               | N/A                           |
| JH-E6    | N/A                                | 00020F12h (940)<br>00020F32h (939) | N/A                                | 00020F32h (939)                       | N/A                                | 00020F32h (939)                       | N/A                             | N/A                                | N/A                           | N/A                               | N/A                           |

I've sent my arguments to the author of CPU-Z, Franck Delattre, and he agreed, adding identification of single-core Toledo Athlons starting from version 2.07. This Toledo research

took place back in 2022 and I didn't know why the extended model is 3 and model number is 7. Now we do.

## 2.6 OPN suffix

As we can see in the previous chapter, a San Diego part has a different OPN than a single-core Toledo. So how does the suffix relate to the core? Take a look at the following [table](#). Since all K8 CPUs are Family "F", I've deleted the first column of CPUID. CPUs are grouped by extended family and list model numbers in descending order. As we can see, the model number stays the same within one socket and core configuration (SH, DH), except for the extended model 3 we discussed earlier.

CPUs from different segments sharing the same die (Athlon, Sempron, and their mobile counterparts) share the same model number. Another interesting detail is that Opterons and their socket 939 Athlon counterparts come with consequent suffixes. For rev C, it was 939/1-way 940/2-way 940 and 8-way 940 (AS/AT/AU/AV), while for rev E, it was the other way around, with socket 939 following 940: 1-way 940/2-way 940/8-way 940 and 939 (BK/BL/BM/BN). Since the suffix "BA" is taken by socket 754 Winchester, we can guess that the Athlon 64 FX D0 revision would have a suffix "BE" if it had reached the market. The non-existing cores are greyed out. A number of CPUs are mentioned in the revision guide but didn't make it to production.

But is it all there is to know about suffixes? Well, not quite. Have you ever wondered what the difference is between a Newark CPU (mobile Athlon 64) and Lancaster (Turion)? Both share the same cache size, die size, CPUID and almost everything else.

### 2.6.1 Low-power suffixes

Let's take a look at a document named "[Near-Term-Print.ppt](#)" by AMD.



## MOBILE AMD ATHLON 64 PROCESSOR

---

### UPCOMING FEATURES AND TECHNOLOGIES (Nov. 2005 -> Nov. 2006)

- DDR2
- Dual-channel memory interface
- Dual-core technology
- Virtualization

### CURRENT FEATURES AND TECHNOLOGIES

- AMD64
- 90nm SOI
- DDR
- SSE3
- 8 GB/sec HyperTransport™ Technology
- AMD PowerNow!™ Technology
- Direct Connect Architecture
- Simultaneous 32- and 64-bit Computing
- Wireless compatibility
- Enhanced Virus Protection

Now, let's compare it with Turion:



## AMD TURION™ 64 MOBILE TECHNOLOGY

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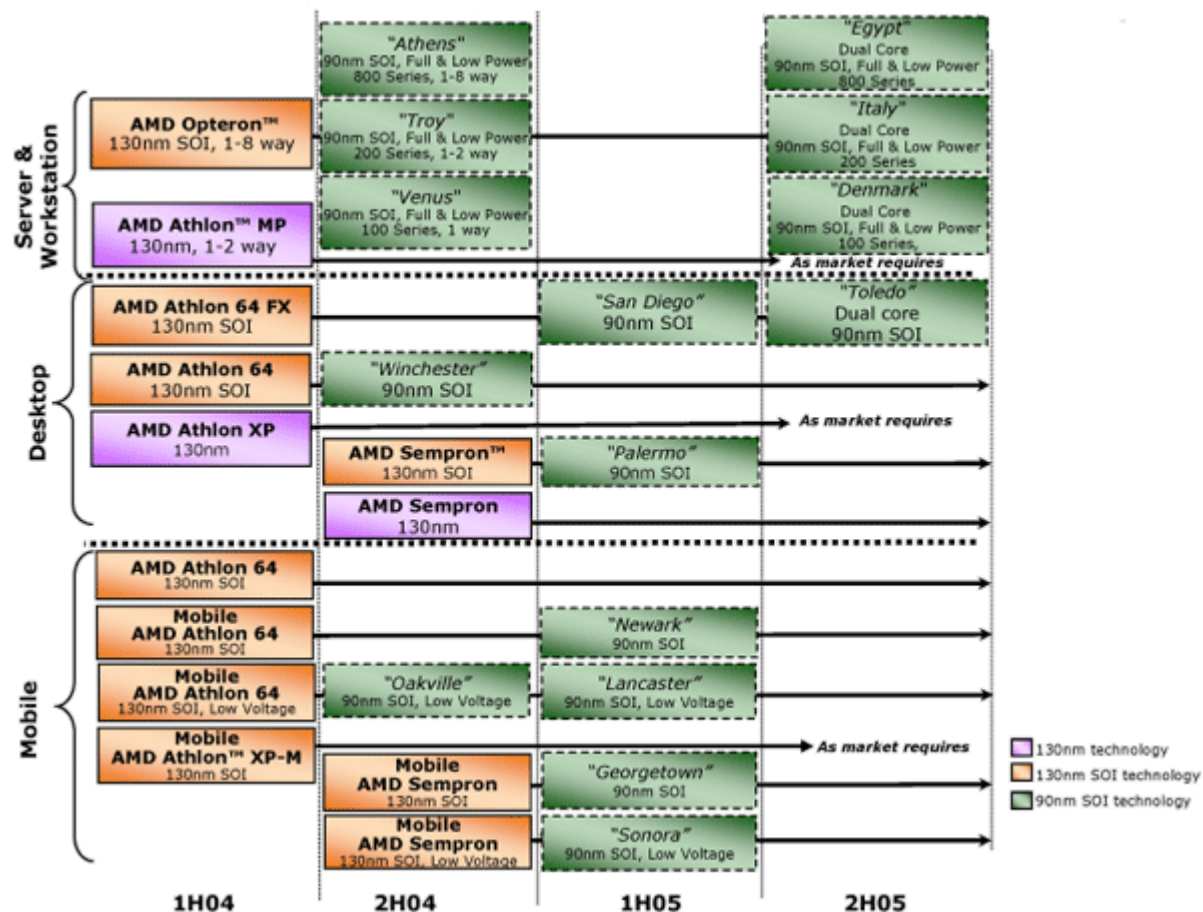
### UPCOMING FEATURES AND TECHNOLOGIES (Nov. 2005 -> Nov. 2006)

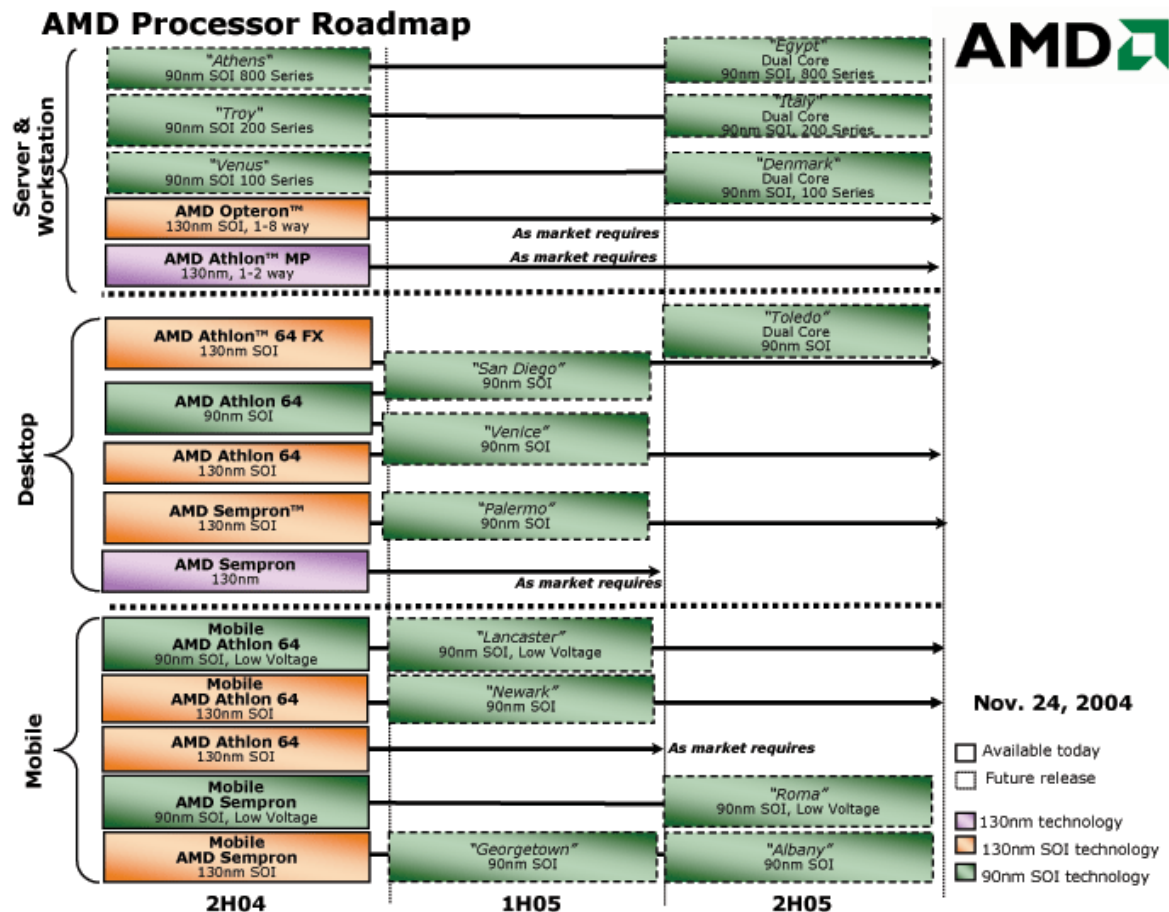
- DDR2
- Dual-channel Memory Interface
- Dual-core technology
- Virtualization

### CURRENT FEATURES AND TECHNOLOGIES

- AMD64
- SSE3
- DDR
- Wireless Compatibility
- AMD PowerNow!™ Technology
- Simultaneous 32- and 64-bit computing
- Enhanced Virus Protection
- Direct Connect Architecture
- 90nm SOI
- 6.4 GB/sec HyperTransport™ Technology
- Mobile specific process technology

To clear things even more let's take a look at two roadmaps:





So, what do we see here? Newark is based on a tech process called “90nm SOI,” whereas Lancaster is based on “90nm SOI, Low Voltage.” Although they have the same VID, what hides under these terms is likely the TDP. And yes, all low-power parts have specific suffixes. Here’s a list:

**LA** - Mobile Sempron “Dublin,” a low-power version of the AY suffix

**LB** - Mobile Athlon 64 “Oakville,” mobile Sempron “Sonora,” low-power version of the BA suffix

**LD** - Turion 64 “Lancaster,” low-power version of the BU suffix

**LF** - Mobile Sempron “Roma,” low-power version of the BX suffix

So, all low-power parts have a suffix starting with “L,” which might stand for low-power (pretty obvious, though I couldn’t find any information in this regard). But what does it mean? I remember reading back then that a chip production line could be tuned to make either higher clocking but more power-demanding dies or more energy efficient but lower clocking parts. I couldn’t find any editorial regarding this case in present day, so you can consider this a theory. So some lines were tuned to make cooler and slower chips that went into low-TDP CPUs, while others were tuned for standard power and higher clocking specs.

## 2.6.2 OEM suffixes

Another interesting case is OEM CPUs. These were made for the OEM market, primarily for customers like HP or Dell. Their only difference was the HT bus speed, which has been limited to 800MHz (down from 1000MHz). The following suffixes were used for those OEMs:

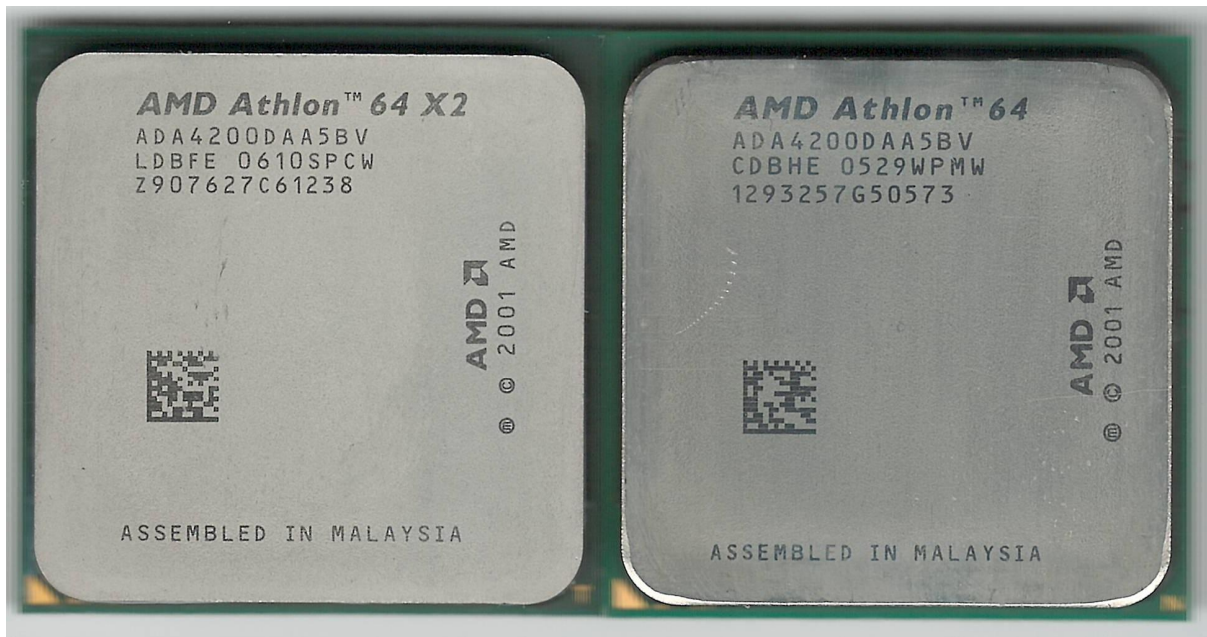
**AZ** - [Newcastle HT 800MHz](#)

**BZ** - [Venice E3 HT 800MHz](#)

**BY** - Venice E6 HT 800MHz

## 2.7 Curious peculiarities

- The year 2001 printed on all K8 CPUs is the year the Hammer architecture was announced, and the first samples were built.
- DDR 400 support was added to AMD CPUs starting from the C0 revision. Therefore, early retail AMD Opteron CPUs with the B3 revision and all earlier pre-production and ES CPUs supported only DDR 333.
- DDR 466 and 500 support was added in revision E. While this is well-known for socket 939, the same memory modes are available to socket 754 with the proper CPUs.
- The Athlon 64 in the 754 pin package supports up to four registered DIMMs, just like socket 940 Opterons (four DIMMs per channel), although such a motherboard appeared only once at [Comdex 2002](#). This feature probably has its roots in Clawhammer-DP.
- The Athlon 64 [can work](#) with registered DIMMs, despite such combinations not being officially supported.
- Opterons using socket 940 can work with unbuffered memory; this is more a BIOS feature, as some will initialize with regular sticks, while most won't.
- So, what are the main differences between an Athlon 64 and an Opteron if they support the same memory types? According to a page dedicated to the [Opteron 100 series](#), it's the die material (wafer), along with the extended testing and validation used by the Opteron family.
- Socket 754 CPUs (except for Semprons and Athlon XP-M) can run at HT 1000MHz (with a x5 multiplier) when paired with a chipset that supports it, so it's more of a chipset limitation back in those days rather than a CPU limitation.
- Retail Athlon 64 X2 CPUs didn't have an "X2" marking on the IHS up until around week 0537.



## 2.8 Crazy theory

This is just my theory, and I haven't been able to find any information on this subject. But what if the core configuration names aren't random letters? Given that this is what is called AMD Hammer, maybe they stand for the following:

- SH - Sledgehammer
- CH - Clawhammer
- DH - Dead-blow hammer
- BH - Ball peen hammer
- JH - Jackhammer

An interesting [mention](#) has been found to solve the CH = Clawhammer contradiction:

*"Originally, AMD introduced "SledgeHammer" with MB-class L2 cache to "Opteron" for servers & workstations, and "SledgeHammer" for desktops. The Athlon 64 was supposed to be loaded with ClawHammer, whose L2 cache capacity is estimated to be around 256-512KB."*

## 3. AMD chipset and boards

Along with the new CPUs, AMD announced a new chipset which consisted of the following:

- AMD-8151 ("Lokar") - HyperTransport AGP 3.0 Graphics Tunnel
- AMD-8111 ("Thor") - Southbridge
- AMD-8131 ("Golem") - HyperTransport PCI-X Tunnel. Later upgraded to
- AMD-8132 ("Golem2?") - HyperTransport PCI-X 2.0 Tunnel

Worth mentioning is the ALi M1687/M1563 chipset. It was rumored that the M1687 is nothing more than a licensed AMD 8151 bridge. Both use 564-Ball, 31mm x 31mm BGA Package.



AMD 8151 A1 ES.



ALi M1687 press-release. Note the same package number **27271**. AMD has been using five-digit package markings for almost forever; I think it speaks for itself. If you're not convinced, you can check out the retail B2 revision:



and a retail M1687:



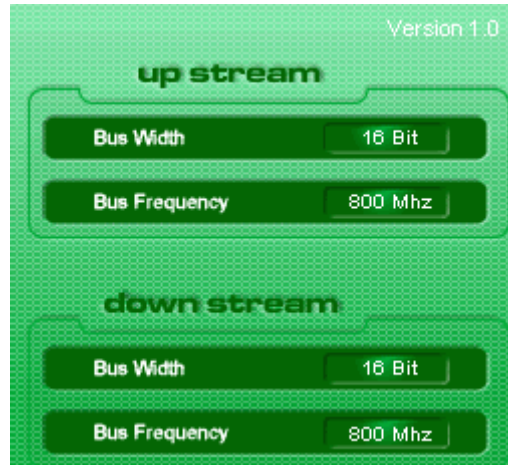
Mind the same **27482** package number this time. If the ES version had a K6-like heatspreader, the release version has a heatspreader like the ones we see on NICs, RAID controllers, and other smaller chips. What is interesting is that the southbridge was ALI's already existing chip that used HyperTransport for connection with the AGP bridge. That's why they could use AMD's AGP bridge and their in-house southbridge. It's rare to see a board using chips from different vendors, although such cases exist throughout PC history. The next chip from ALi, the M1689, was their own development and became a single-chip solution.

### **VIA HyperTransport Analyzer**

Along with a new CPU microarchitecture, AMD has implemented a new data bus in their Athlon 64 CPUs: HyperTransport, formerly known as Lightning Data Transport (LDT), a codename, which has been used in a number of boards like DFI. Although the Athlon 64 CPUs initially supported a 16/16 bit (downstream/upstream) bus width and an 800MHz frequency, most chipsets had problems achieving this bandwidth. Some supported only 8/8bit or 16/8bit widths, while others supported the full 16/16 width but at 600MHz. And this was a chance for VIA to let their marketing department mock other vendors. They developed a utility called the VIA HyperTransport analyzer that showed upstream and downstream bus width and frequency, all to promote their K8T800 chipset, which achieved full 6.4Gb/s bandwidth due to their Hyper8 technology that “eliminates noise on the HyperTransport link between the processor and chipset”—whatever that means.

As we can see, some chipsets had problems even achieving stock clocks. That’s why, at first, Athlon 64 overclocking was very limited until overclockers figured out it was the HT frequency to blame and started dropping HT multiplier to hit higher CPU frequencies.

Another interesting detail is that the HT standard supports bus widths of 2 and 4 bits, but this feature isn’t used in any production boards; it was found as a hidden option in the AMD Solo 5 development board BIOS. Additionally, HT supports bus frequencies of 300 and 500MHz, meaning a half-integer multiplier that isn’t commonly seen. The 300MHz option has been used on some NF3 150 boards.

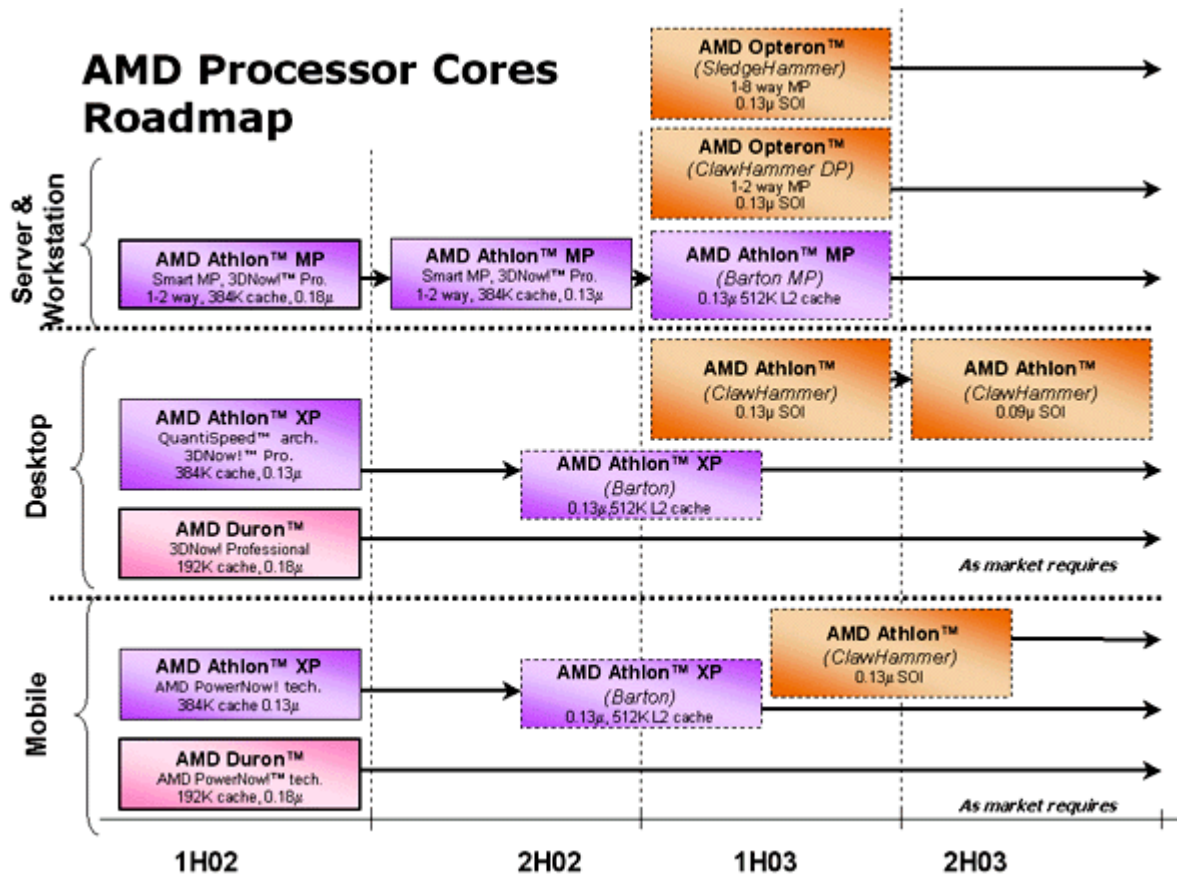


### 3.1 AMD development boards

#### AMD Stretto

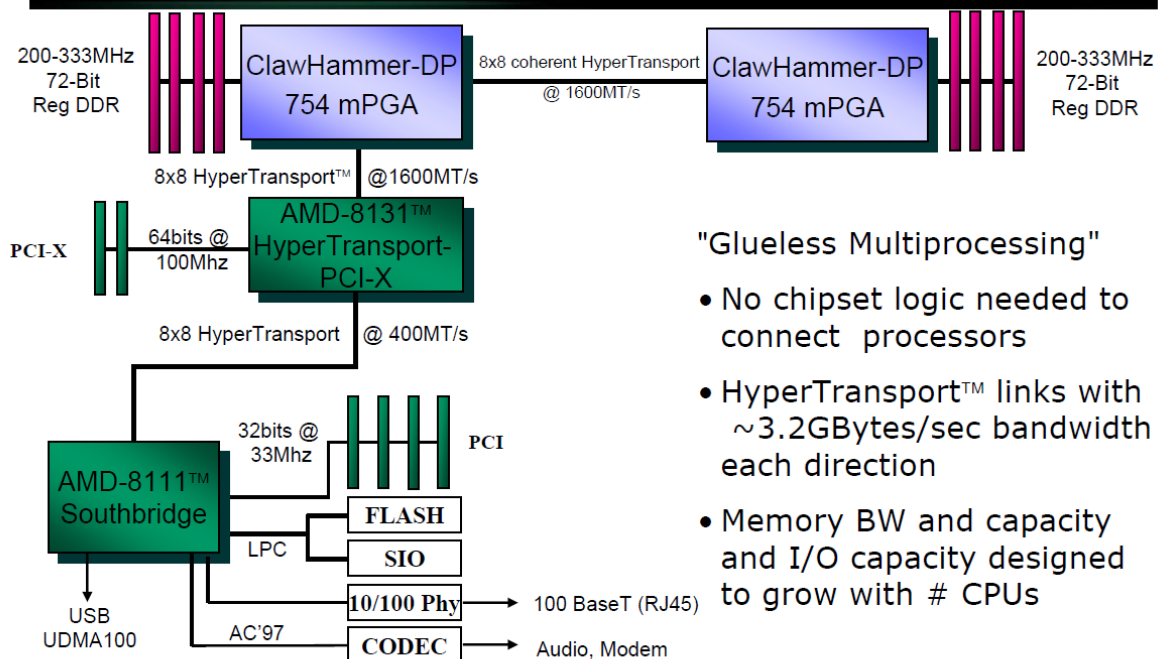
This platform appeared only in early roadmaps and in the [Hammer Overview](#) during the AMD Developer Symposium dated 17 October, 2002.

Fun fact: on page 2, they messed up the descriptions for the AMD-8131 and AMD-8151; they should be the other way around. Page 14 describes them correctly.



This roadmap is dated 12 September, 2002.

# Hammer 2P System Builder Server (Stretto)



## "Glueless Multiprocessing"

- No chipset logic needed to connect processors
- HyperTransport™ links with ~3.2GBytes/sec bandwidth each direction
- Memory BW and capacity and I/O capacity designed to grow with # CPUs

The project was quickly abandoned, but what should come to your mind is: how on Earth did a strictly UP socket 754 get a DP version? And this is a good question. As you know, a K8 SMP system should have a second HT link for CPUs to communicate with each other, not only with the chipset. And here's how the magic worked.

# Foundation: AMD Silicon & Hammer Family Processors

## AMD Athlon™ processor (ClawHammer-DT)

- Performance Desktop Processor
- One 72-bit DDR channel supporting 200, 266, and 333 MHz
  - Future memory technology support as it is defined
- One 16-bit HyperTransport™ Link at 1600MT/s
- 256K-Byte and 1M-Byte integrated L2 cache products
- 754-pin mPGA Package

## AMD Athlon (ClawHammer-DP)

- 2-way Entry Server & WS Processor
- One 72-bit DDR channel supporting 200, 266, and 333 MHz
  - Future memory technology support as it is defined
- Two 8-bit HyperTransport Links at 1600MT/s
- 512K-Byte and 1M-Byte integrated L2 cache products
- 754-pin mPGA Package

**NOTE: All Hammer family processors support x86-64 technology**

## AMD Opteron™ processor(SledgeHammer-MP)

- Up to 8-way Server-Class Processor
- Two 72-bit DDR channels supporting 200, 266, 333 MHz
  - Future memory technology support as it is defined
- Three 16-bit HyperTransport™ Links at 1600MT/s
- 1M-Byte integrated L2 cache
- 940-pin mPGA Package

It appears that Stretto used what is now known as port bifurcation for PCI-E technology. In other words, it refers to the ability of a 16/16 bit HT link to work as two 8/8 bit HT links. Moreover, since Hammer cores were developed as a unified architecture, I have some arguments suggesting that this feature could be present in s754 CPUs, at least in Clawhammer cores, although I won't go into detail to keep this story from growing too large. Aside from that, the Clawhammer DP CPUs were essentially identical to their s754 counterparts, utilizing single-channel memory with ECC capability and four slots of registered DDR memory.

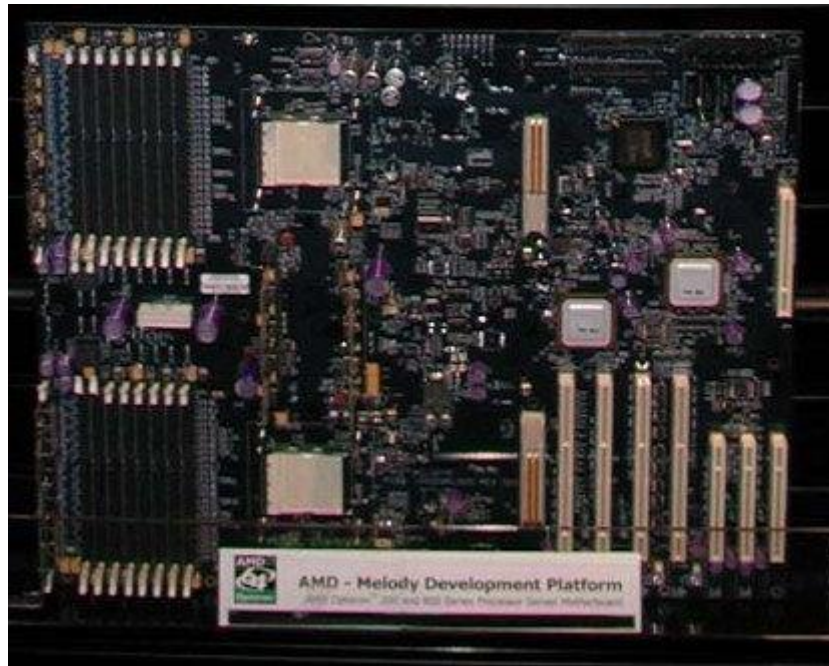
A real photo appeared only once when it was sold at an [auction](#).



You can see a 2+4 memory slot configuration (the outer “slots” on each side are used for the memory VRM).

### **AMD Melody**

Another development board from AMD, but this time it’s a dual socket 940. This board was used to demonstrate the first beta version of 64-bit Windows .NET Enterprise Server, build number "3620.Lab01\_N.020331-2000". The first demonstration took place during SBS Europe 2002 in Monaco, and a few weeks later at Computex 2002 in Taipei.



### **AMD Harmony**

A daughterboard with 2 socket 940 for the AMD Melody board that allows to build a 4-way Opteron system. During Computex 2002 in Taipei, such a system [was shown](#) running 4 Opteron CPUs on Linux.

### **AMD Solo**

A line of uniprocessor boards by AMD that were used for demonstration and internal testing.

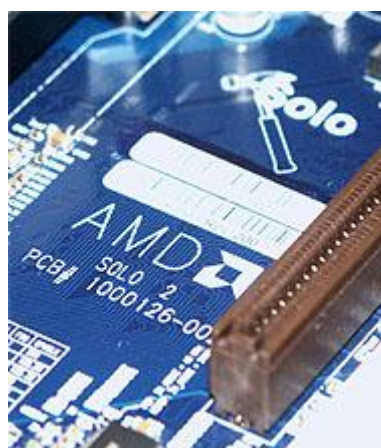
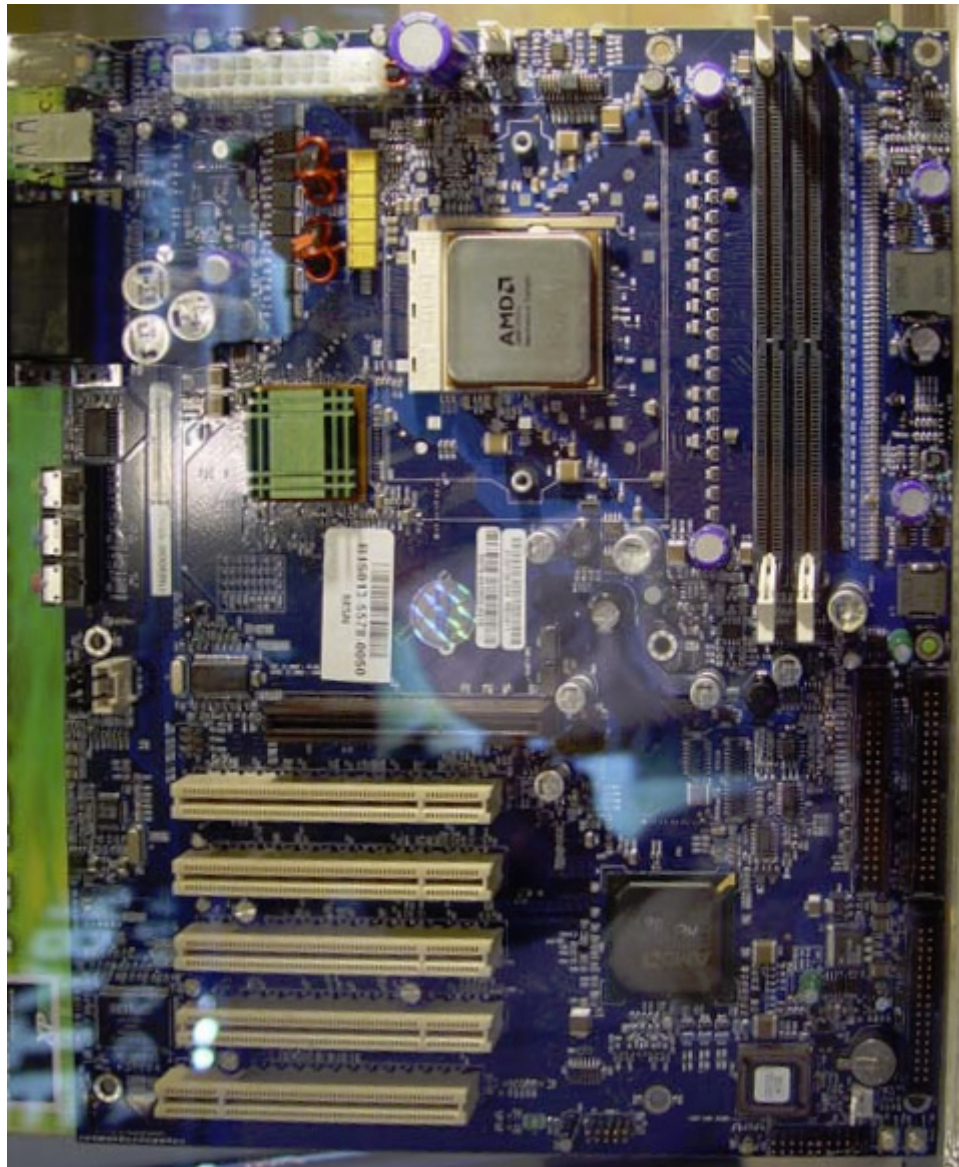
#### **Solo 2 (0100126-004 REV200)**

The first AMD Hammer board ever known to the public. AMD used this board for their first Athlon 64 demonstration during Intel IDF 2002. The board designers showed their sense of humor by placing five notes of the famous Intel tune using silkscreen on the PCB, along with a hammer very similar to the Tom's Hardware Guide logo.



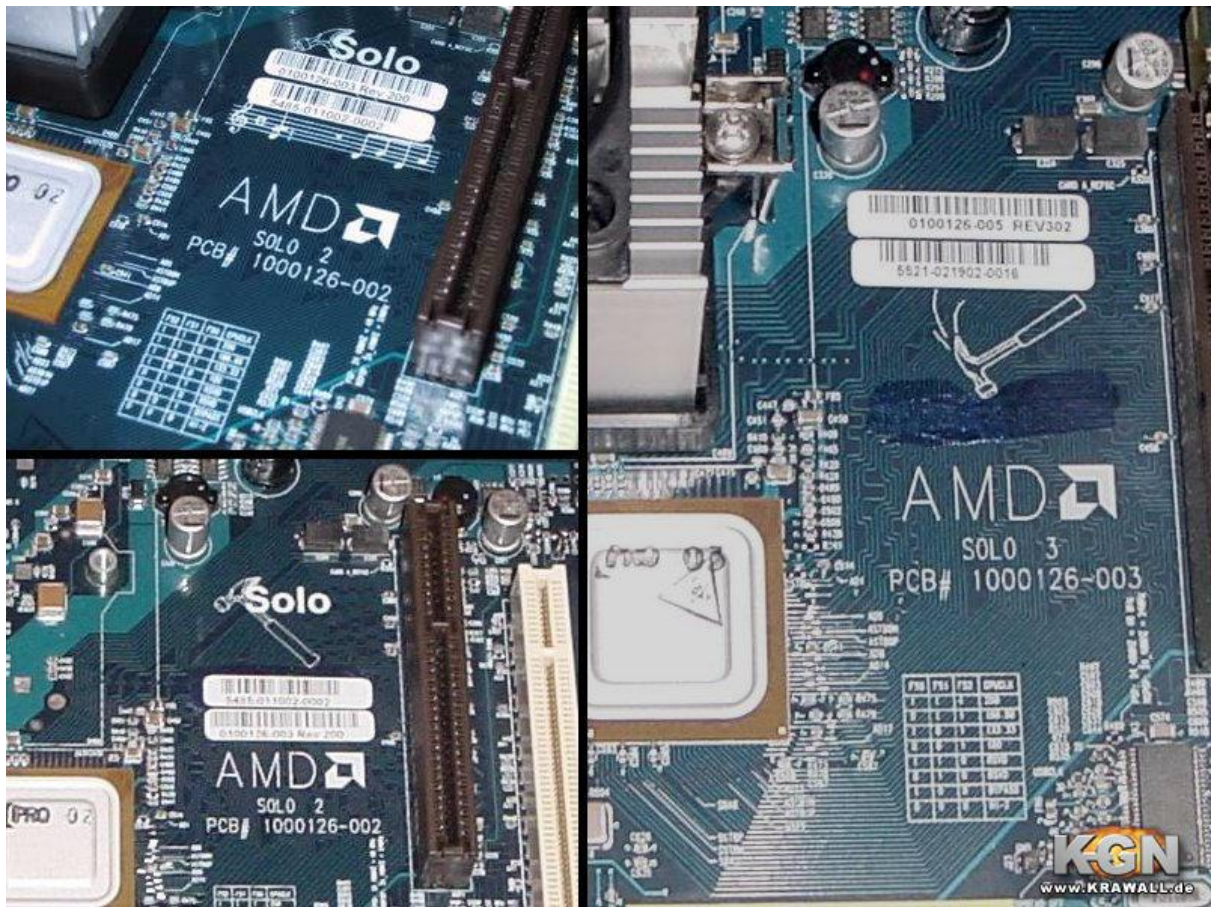
**Solo 2 (0100126-003 REV200)**

This board was used for a demonstration during CeBit 2002. During this demonstration, the Intel tune was covered with stickers because AMD's lawyers didn't find this joke funny. I must admit it was a hilarious one.



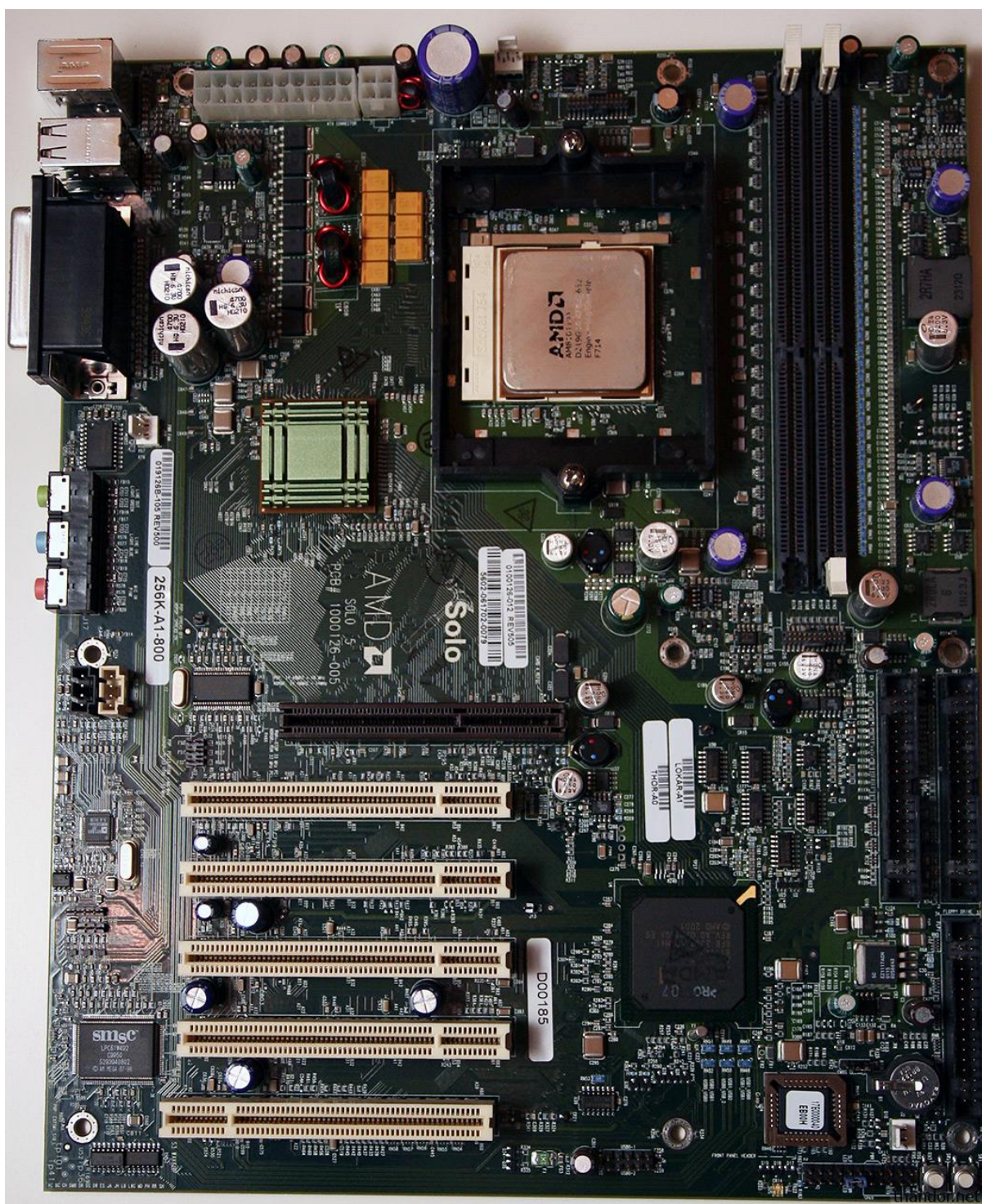
### **Solo 3 (0100126-005 REV302)**

Only a few photos have been found. This board was used in live systems demonstrated at CeBit 2002. Mind the hammer about to strike something that has been painted out. We can guess it's the crashed Intel tune again.



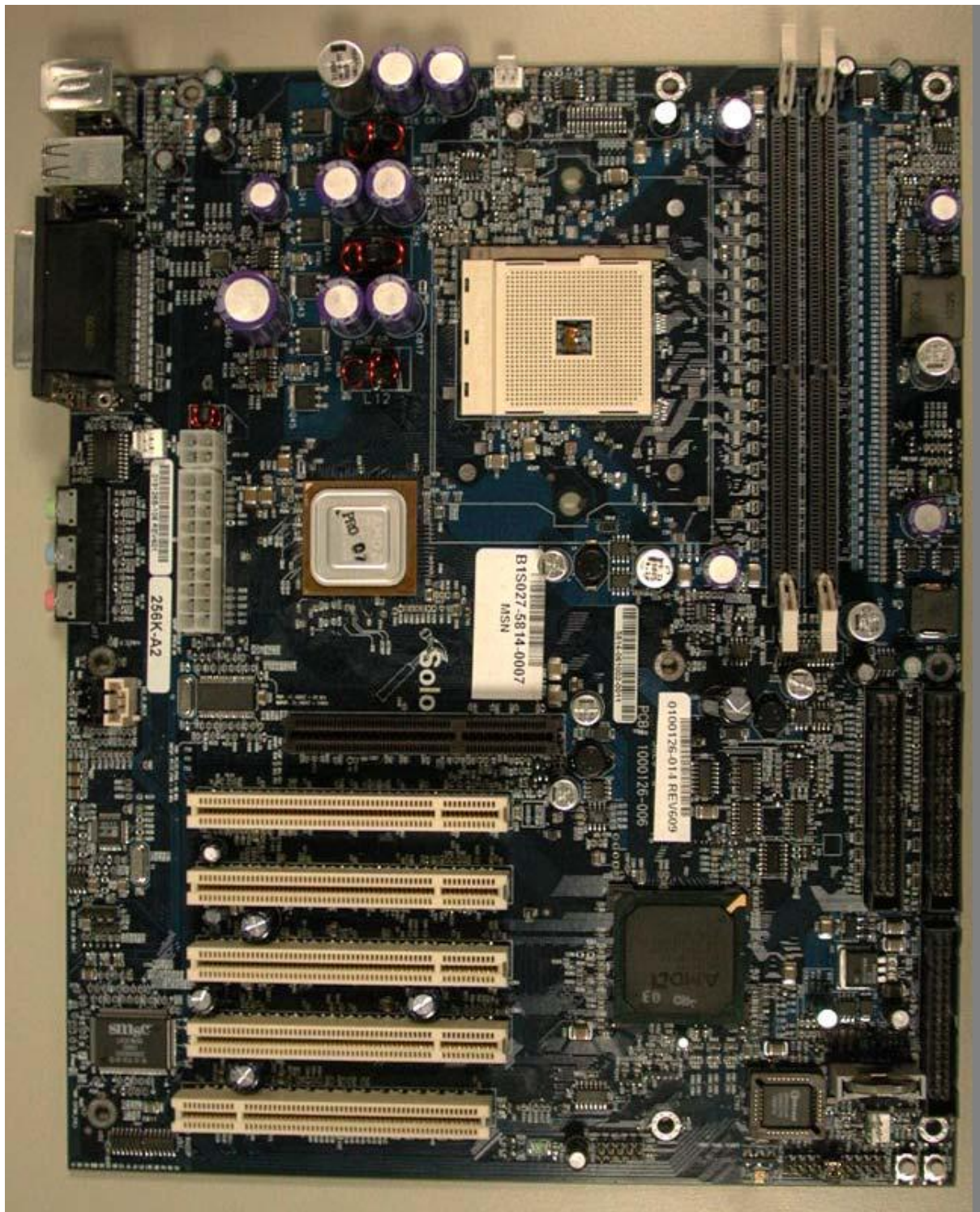
### **Solo 5 (0100126-012 REV505)**

The first version of the Solo boards with a dark green PCB. It was shipped with an Athlon 64 800MHz 256KB L2 cache, revision A1, making it the second ever known. This board does not work with retail revisions and is incompatible even with B0 revision CPUs (2800CN5). You can read more about this board on Thandor's [website](#). He has provided valuable info about his CPU and board along with CPU-Z reports and a BIOS image of Solo 5 and info about other AMD samples.



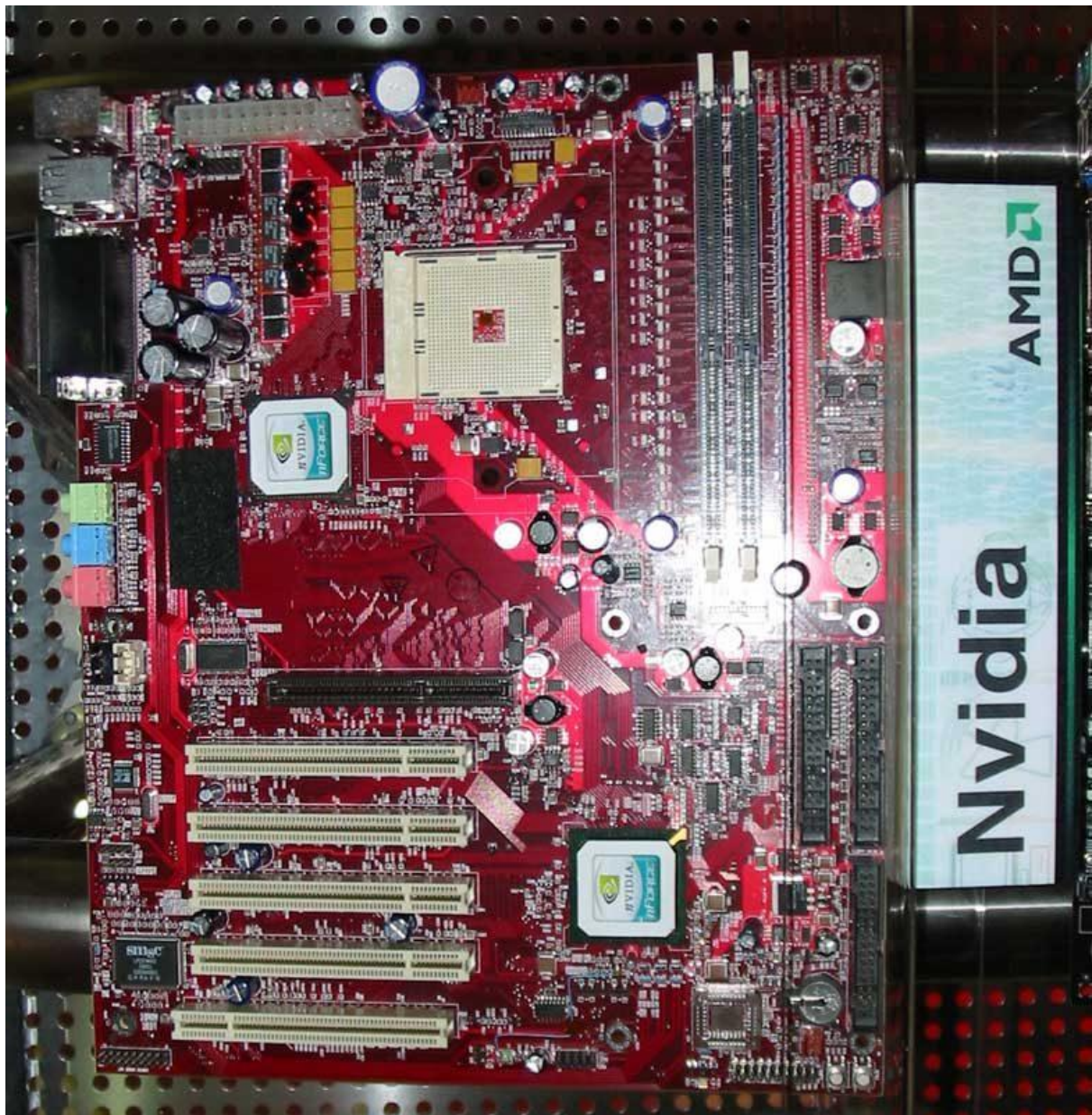
### Solo 6 (0100126-014 REV609)

It is known to have appeared only once in public during [SMAU 2002](#) in Milan. Be careful, as the preview by Hardware Upgrade used a photo of Solo 5; the real photos of Solo 6 can be found on page 3. This is the first version that started using a 3-phase VRM and lacks the HDT connector with JTAG (although the traces remain present). As we can see, it was shipped with Athlon 64 A2 revision and 256KB L2 cache.



### **Nvidia “reference” board**

This board was shown during Computex 2002 as an Nvidia board, but [Japanese journalists](#) say that AMD chips are hidden under the stickers. The design looks exactly like the Solo 2 board, with a custom PCB color and silkscreen.



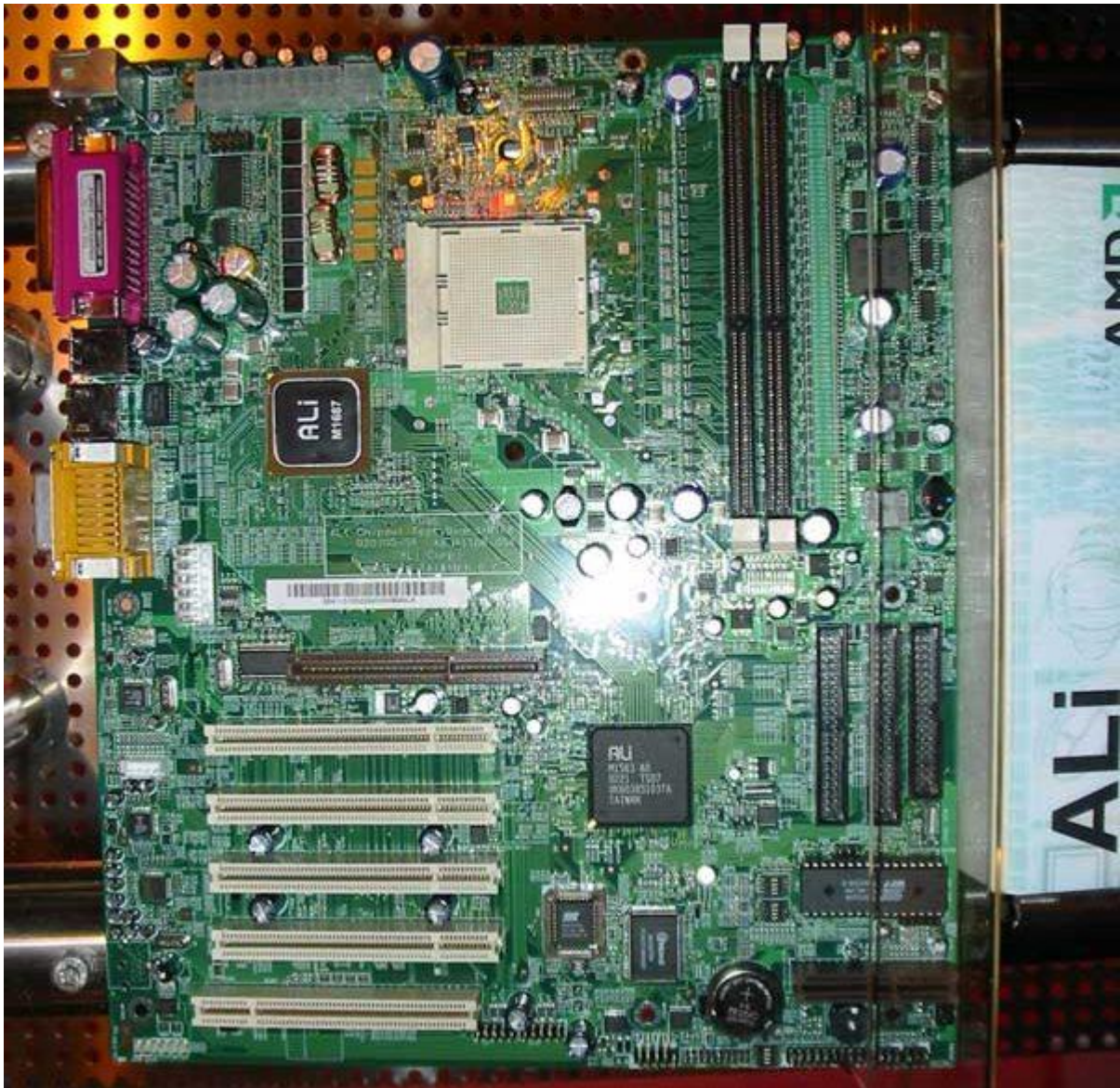
### **Abit K8A (unreleased)**

It is essentially a clone of the AMD Solo 2. There is a bit of empty PCB space on the right and left sides, tantalum capacitors in the CPU VRM have been switched to ceramic, and there are some other minor changes.

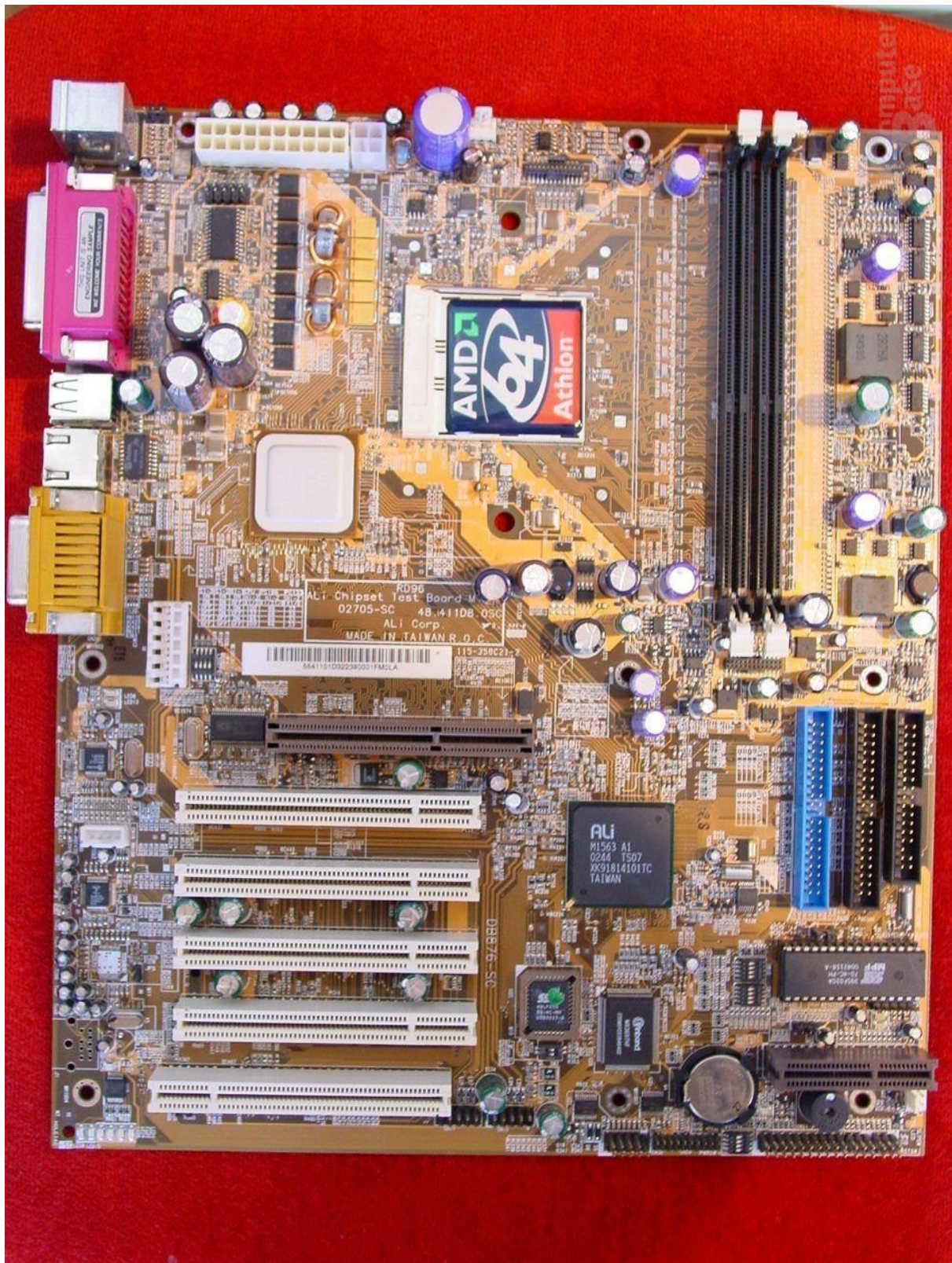


### **ALi M1687 reference board**

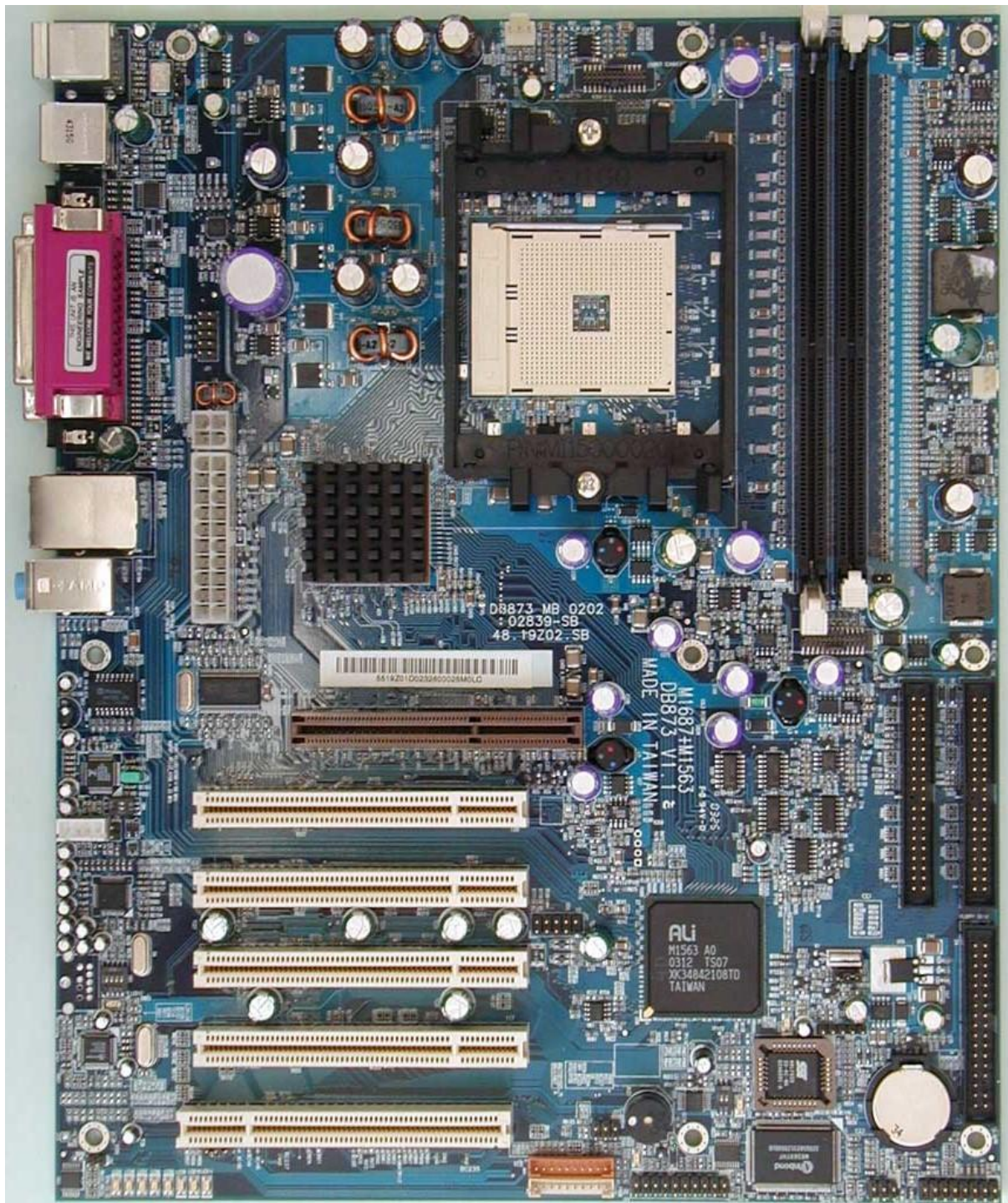
Not quite an AMD reference, but the M1687 is licensed from the AMD-8151, and the board is based on AMD Solo boards. This earlier reference board seems to be based on the Solo 2. You can notice a sticker on the northbridge, probably because they used an AMD-8151 for reference.



This slightly newer version has bigger input capacitors just like Solo2; the tantalum capacitors are closer to each other, and there are thicker wires in the inductors. The HDT connector is present. This version was displayed using both green (but with all the differences from the first version mentioned above) and brown PCBs, as shown in the photo below. Also note the two BIOS chips: LPC and parallel. This is due to a southbridge from ALi, which supports both standards.



This seems to be a newer revision of the ALi M1687 reference board and looks like it is based on the Solo 6. The second BIOS chip is gone.



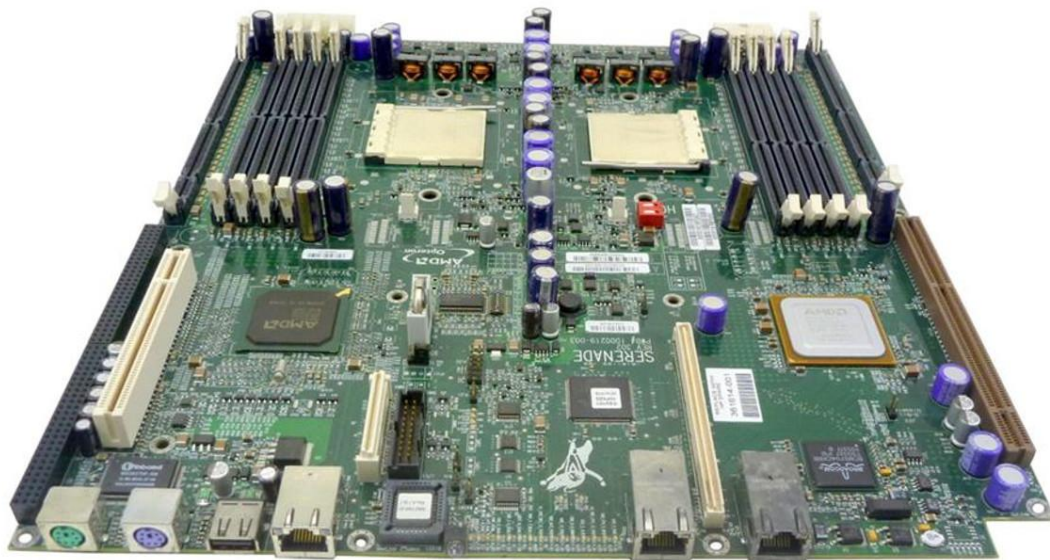
Additionally, there's a comprehensive list of early and pre-production socket 754 boards compiled by [AMDboards](#), along with [socket 940](#) boards.

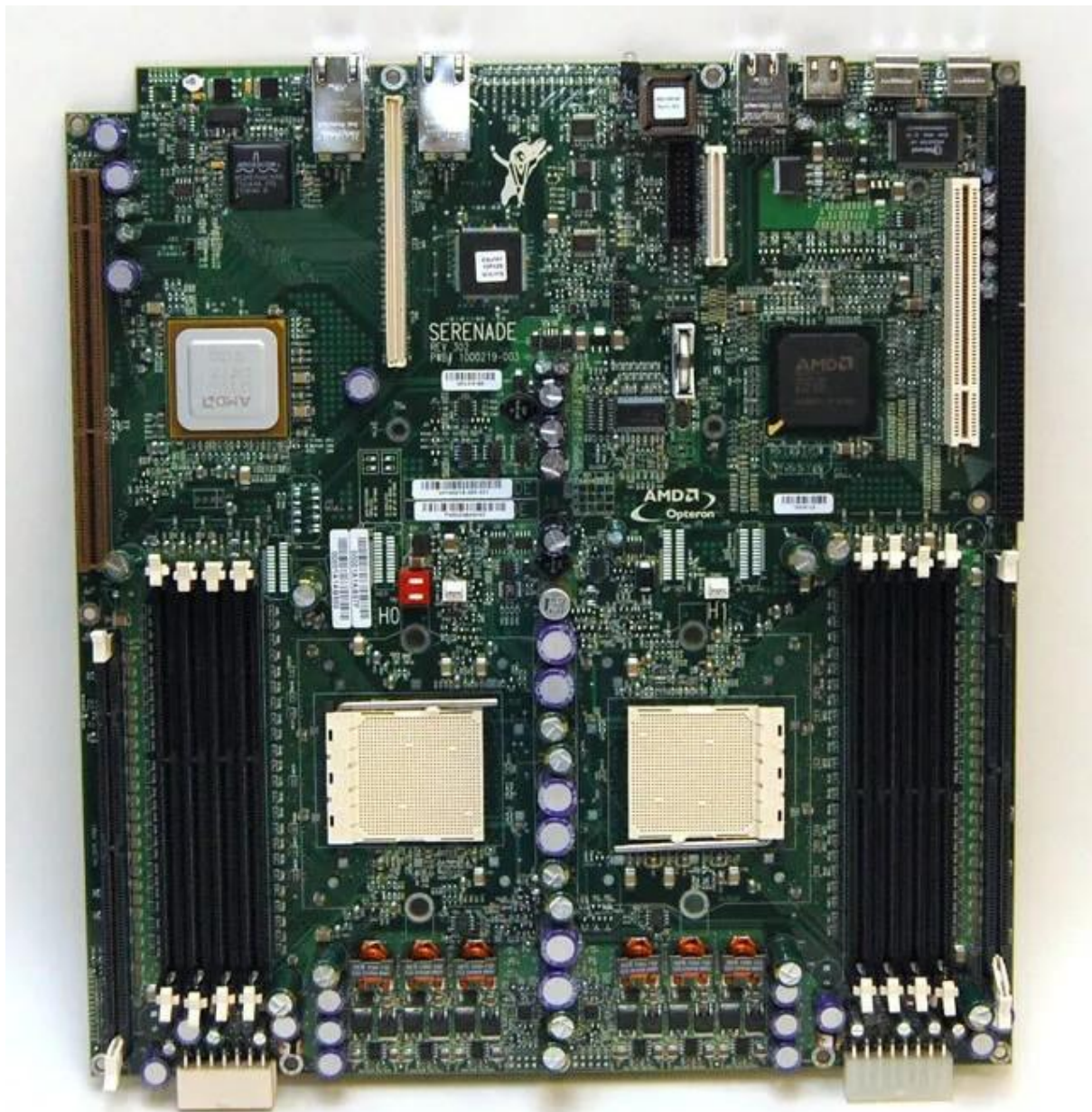
## 3.2 AMD production boards

### AMD Serenade

A 2-way production board by AMD has been sold as part of the Celestica A2210 Dual Opteron server platform for OEMs and system builders. It was also being sold as HP ProLiant DL145 server.

Link to [specifications](#).

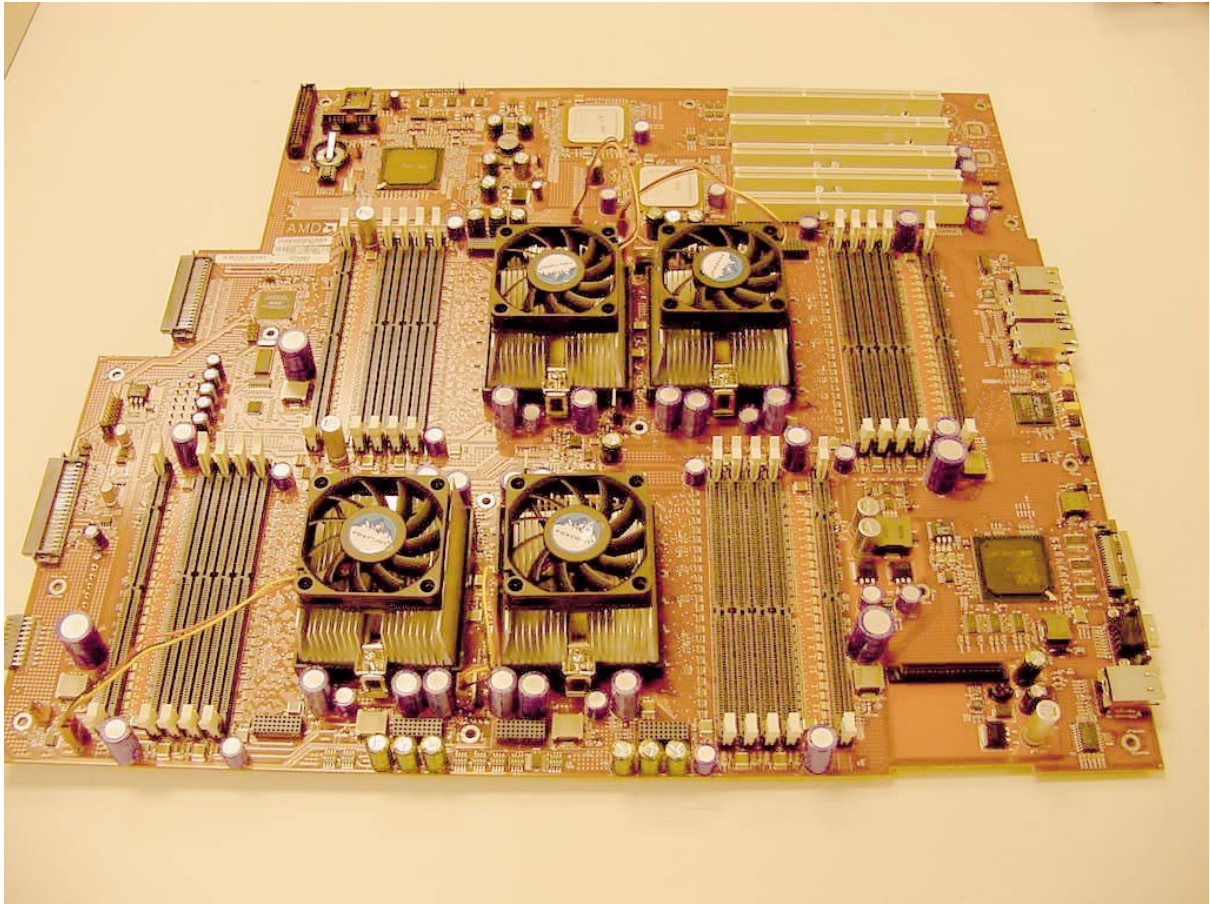




### **AMD Quartet**

A 4-way board by AMD has been sold as part of the Celestica A8440 Quad Opteron server platform for OEMs and system builders.

Link to [specifications](#).



## 4. Before the launch

### 4.1 The sacred timeline

The story of the AMD Hammer began long before its launch in 2003. Here is a list of the most significant milestones along the way.

#### **5 October 1999**

Fred Weber [talked](#) about the AMD K8 x86-64 architecture with two cores on a single die and a fast LDT (Lightning Data Transfer) bus (later known as HyperTransport) at the Microprocessor Forum 1999. [Microprocessor report, 1999](#).

#### **10 August 2000**

AMD released the [x86-64 Architectural Specification](#).

#### **6 October 2000**

AMD [released](#) the x86-64 technology simulator, also referred to as the AMD SimNow! simulator.

#### **27 April 2001**

AMD [delayed](#) the Clawhammer and Sledgehammer release for the first time, moving it from the originally planned Q1 2002 to H2 2002 to produce it using their upcoming SOI technology.

## **2 October 2001**

[AMD's Hammer micro architecture preview](#) by Hans de Vries, based on information collected from AMD's patents. Some patents date back to '98, showing that the work started long ago.

## **15 October 2001**

Fred Weber (AMD VP and CTO) [presented](#) the AMD Hammer architecture at the Microprocessor Forum 2001. A [white paper](#) has also been published on AMD's website.

## **8 November 2001**

Sledgehammer is [now planned](#) for H1 2003, and Clawhammer is planned to Q3 2002.

## **26 November - 2 December 2001**

The first samples being demonstrated [have been produced](#).

## **21 February 2002**

AMD has [announced](#) the AMD-8000 series of chipsets.

## **26 February 2002**

First AMD Hammer live demonstration during IDF Spring 2002. [Anandtech](#), [THG](#). Live systems used the Solo 2 board with PCI VGAs and an 800MHz 256KB Clawhammer ES. The exhibition sample was a Solo 2 board featuring the famous mocking Intel jingle and a THG-ish hammer over it. Mechanical samples of Clawhammer and Sledgehammer were also shown (they didn't have marketing names by that time).

A much lesser-known fact is that in a separate demo room, AMD has shown a working [Sledgehammer system](#) to selected company representatives.

## **28 February 2002**

AMD [announces](#) SUSE Linux support for x86-64.

## **17 March 2002**

AMD Hammer samples are demonstrated on two live systems: one based on Solo 2 and the other based on [Solo 3](#), both equipped with AGP cards.

## **24 April 2002**

AMD [announces](#) the Opteron family. Microsoft announces a 64-bit version of Windows.

## **6 May 2002**

Production date of the Athlon 64 1.4GHz engineering sample and the AMD Solo 5 motherboard in [Thandor's](#) collection.

### **16 May 2002**

First demonstration of a [dual Opteron setup with the AMD Melody board](#) ([1](#), [2](#) more) running a beta version of 64-bit Windows .NET Enterprise Server, build number "3620.Lab01\_N.020331-2000," during [SBS Europe 2002](#) in Monaco.

### **3 June 2002**

First demonstration of a 4-way Opteron server running 64-bit SUSE Linux using a 2-CPU AMD Melody motherboard and a 2-CPU AMD Harmony daughterboard during [Computex 2002 Taipei](#). Real [engineering samples](#) were shown (dated the same week as those shown during IDF, 48th week 2001). Several vendors displayed early samples of their motherboards, although some just used “placeholder” boards like Nvidia.

### **12 September 2002**

AMD [delays](#) Clawhammer to Q1 2003 and keeps Sledgehammer for H1 2003.

### **16 October 2002**

During [MPF 2002](#), AMD showcased a [dual 1.4GHz Opteron](#) ([2](#)) system from Newisys running at 1.4GHz.

### **29 October 2002**

AMD [opens](#) AMD Developer Center.

### **19 November 2002**

The AMD Athlon 64 family is announced for desktop and mobile processors at Comdex 2002. [Athlon 64 samples](#) run at 1.4GHz. Opteron systems are shown in both [4-way](#) (AMD Quartet) and 2-way (Newisys) configurations. Many motherboard manufacturers have shown their socket 754 boards.

### **20 November 2002**

AMD [has demonstrated](#) a 64-bit version of Unreal Tournament 2003 at Comdex 2002. Although Epic games stated that the 64-bit version would be shipped when the Athlon 64 “show up on retail shelves”, it has been delayed and only became available in [Unreal Tournament 2004](#) on 1 October 2005.

### **17 January 2003**

The Athlon 64 lineup is [disclosed in a new roadmap](#), which should introduce the Athlon 64 2800+ 1.6GHz, 3100+ 1.8GHz, and 3400+ 2.0GHz.

### **22 January 2003**

AMD [announces](#) the AMD Opteron Processor-Based Server Evaluation Program.

### **31 January 2003**

The Opteron launch date [was announced](#), and the Athlon 64 was once again delayed to

September 2003.

### **19 February 2003**

First demonstration of an [Athlon 64 based notebook](#) during IDF 2003 ([more pictures](#)).

### **22 April 2003**

AMD Opteron 240, 242, and 244 launched.

### **19 June 2003**

AMD plans [revealed](#) (2) to release the Athlon 64 with dual-channel memory support in the second half of 2004, what we now know as socket 939.

### **25 June 2003**

Hardware Mania has published a review of an [Opteron 240 B3](#) with Asus SK8N.

### **26 June 2003**

AMDZone conducted its first [overclocking tests](#) ([CPU-Z screenshot](#)) with the ES Opteron 242 B0 revision. They were able to achieve an HT bus frequency up to 210MHz in 3D, 220MHz in 2D, and 225 to POST.

### **29 June 2003**

AMDZone has [overclocked the ES Opteron 244](#) C0 up to 2000MHz.

### **17 July 2003**

AMD officially [discloses](#) the Athlon 64 launch date: 23 September 2003.

### **18 July 2003**

Detailed [tests](#) of the Opteron 144 (1.8GHz) with nForce3 150 have been published ([another one](#) with Opteron 144 + Asus SK8N).

### **22 July 2003**

Opteron 244 (1.8GHz) [overclocked to over 2.2GHz](#) using LN2 ([CPU-Z screen here](#)).

### **5 August 2003**

AMD Opteron 246 (2.0GHz) launched. Rumors [disclose](#) a new rating system for Athlon 64 socket 754 (3200+, 3400+, and 3700+) and a lineup of high-end consumer processors for socket 940 named Athlon 64 FX, with model numbers FX-51, FX-53, and FX-55, rather than a performance rating like Athlon 64.

### **8 August 2003**

Tests of [Opteron 246](#) (2.0GHz) are published, along with results from a month later showing it [being overclocked](#) to 2.25GHz, which roughly estimates FX-51 performance).

### **8-9 August 2003**

The T-break forum crew achieved a 3DMark 2001SE score of [24182](#) on air cooling with an Athlon 64 3200+ at 2.16GHz and **24747** at 2.4GHz. A day later, they achieved [25051](#) with some additional GPU clocks. The day before launch, they achieved a score of [26336](#) with a 2.6GHz CPU clock using a Prometeia single stage.

### **12 September 2003**

Early evaluation results show the Athlon 64 FX-51 being overclocked to 2.3GHz on air and 2.48GHz on single stage Prometeia Mach II ([1](#), [2](#), [3](#)).

### **13 September 2003**

The first retail Athlon 64 CPUs and motherboards [appear](#) in Japanese stores.

### **23 September 2003**

The AMD Athlon 64 FX-51 and Athlon 64 3200+ are launched. One of the first detailed reviews of the Athlon 64 3200+, FX-51, and P4 EE 3.2GHz, including overclocked modes, is [published](#) on x86-secret.

### **23 September 2003**

AMD founder Jerry Sanders [confirms plans](#) to create multiple Athlon 64 cores on a single chip.

### **30 September 2003**

Japanese overclocker Katsumi has overclocked the Athlon 64 FX-51 to [3.05GHz](#) ([some pictures here](#)) using dry ice, and several days later to [3.3GHz](#) with LN2 ([some pictures here](#)). SuperPi was run at 3206MHz.

### **1 June 2004**

Socket 939 is launched.

### **7 June 2004**

Announcement of the AMD Sempron family.

### **31 August 2004**

[Presentation](#) of the Opteron dual-core.

### **10 January 2005**

Announcement of the AMD Turion 64 family.

## **4.2 The early tests**

A list of all known peek-in tests of engineering and pre-release samples:

- **6 June 2002:** The first-ever test of the Athlon 64 800MHz 256KB revision A0 by [tecChannel](#) during Computex 2002.
- **17 October 2002:** A [first glance at a socket 754 motherboard](#) by THG.
- **14 December 2002:** An Athlon 64 1.2GHz with 1MB L2 cache [was tested](#) by C't magazine.
- **26 January 2003:** The Athlon 64 1.4GHz with 256KB cache, revision A2/A3, [was tested](#) by x86-secret (some additional details and screenshot can be found on [overclockers.ru](#)).
- **31 January 2003:** [Screenshots](#) of SiS tests of the Athlon 64 1.4GHz, revision B0, were published.
- **18 April 2003:** An Athlon 64 2800+ 1.6GHz (old rating) was tested by [Xbitlabs](#).
- **10 July 2003:** An Athlon 64 3400+ 2.0GHz (old rating) [was tested](#) by a user named **I Love Fang**.
- **1 September 2003:** An Athlon 64 3100+ 1.8GHz (old rating) [was tested](#) by OCWorkbench.
- **7 September 2003:** An Athlon 64 3100+ 1.8GHz (old rating) [was tested](#) by En Ming (aka p4coverclocker).

## 4.3 Engineering samples

All ES CPUs I was able to find (before the release, not samples of later generations) were compiled in a [table](#) with their specifications and markings. What is interesting is that AMD used an Fxxxx marking, which appears to encode the multiplier and voltage and should be read as FID x, VID x.xx V. For example, an ES with F9150 will have FID 9x (multiplier 9x) and VID 1.50V. This struck me like lightning due to how easy and succinct it was.

## 4.4 Editorial

1. “[CPU dark history: Intel panics as K8 production stumbles](#)” by Yusuke Ohara - a nice article about Intel’s movements before the Athlon 64 launch and the struggles AMD has been dealing with.
2. [Anandtech](#) explains SOI technology in simple terms.
3. “[Inside AMD - Touring Fab 30](#)” by Anandtech - AMD invited journalists to Fab 30 in Dresden, where the Athlon 64 was manufactured.
4. There is also another article about the tour to Fab 30 by [Computer observer](#), which provides nice information about performance ratings and the people involved in it.

## 4.5 Final words

The K8 architecture became a game changer. It changed the way computers are built, and modern systems continue to follow this design even after two decades. All of this became possible thanks to the following people: Fred Weber, VP and CTO; Richard Heye, VP of Platform Engineering and Infrastructure; and Jerry Sanders, CEO. And of course, many engineers, other AMD employees and their partners whose names we may never know. Thank you for your work; it's a fascinating platform to play with and study on many different levels.

I would like to thank all the enthusiasts and collectors who helped gather very scattered information about ES and other things. I would especially like to thank MIRROR for his consistent stubbornness, which made me search for much more solid proof regarding all my thoughts and theories. It required tenfold more time and effort but expanded this article to its apogee. It has sometimes been devastating, but thank you, my friend, for this journey you made me undertake.