Heading Font Times New Roman of 14 Points On-Chip Center Aligned Wave-Pipelined Serial Interconnect

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ABSTRACT

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Keywords: Controllable inverter pair, Differential interconnect, Method of logical effort, Repeater insertion, Self controllable, Serial link, Surfing, Wave-pipelining.

I. INTRODUCTION

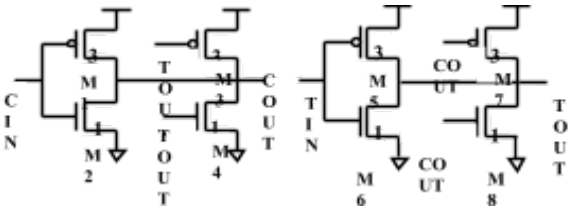
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XxxThe paper is organized as follows: Section II, III describe the design of… Section V provides the post layout simulation results and the observations. The concluding remarks are given in Section VIxxx.

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(a) (b)

Fig. 1. Dynamic Self Controllable inverter pair
a) Surfing circuit for complement path b) Surfing circuit for true data path.

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xxThe absolute delay (D) of a circuit consisting of N stages is given by [4]XX.

$$D = (N F^{1/N} + P) \tau \quad (1)$$

where,

F - path effort

P - parasitic delay of the path (sum of parasitic delay of each stage)

τ - technology constant (12ps for 180nm)

$$T_p = 0.69\left[R_b C_{b0ntt} + \frac{R_b}{f}.fC_b + \ldots + \frac{R_b}{f^{N-1}}.f^{N-1}C_b\right] + 0.69\frac{R_b C_w}{L}\left[a + \frac{ar}{f} + \frac{ar^2}{f^2} + \ldots + \frac{ar^{N-1}}{f^{N-1}}\right] + 0.69\frac{R_w C_b}{L}\left[a + arf + ar^2 f^2 + \ldots + ar^{N-1}f^{N-1}\right] + 0.38\frac{R_w C_w}{L^2}\left[a^2 + a^2 r^2 + a^2 r^4 + \ldots + a^2 r^{2(N-1} \quad (2)$$

III. RESULTS and DISCUSSIONS

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TABLE I
DELAY AND POWER OF THE INTERCONNECT WITH NUR FOR DIFFERENT INTERCONNECT RATIO

Ratio of interconnect segments (r)	Delay of the longest segment in NUR(ps)		Max. operating frequency in Gb/s	
	In [15]	This paper	In [15]	This paper
2.00	643.0	384.6	1.55	2.60
3.00	366.0	340.0	2.73	2.94

Results can be expressed as Fig-2

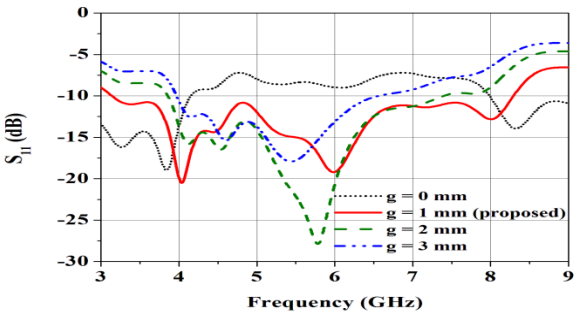


Fig. 2. S_{11} Bandwidth comparison for different values of the gap 'g'

IV. CONCLUSION

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