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**M.Sc. (IT) (Semester –1st)**  
**DIGITAL CIRCUITS & LOGIC DESIGN**  
**Subject Code: MECE0F95**  
**Paper ID: [OE1220424]**

**Time: 03 Hours**

**Maximum Marks: 60**

**Instruction for candidates:**

1. Section A is compulsory. It carries 16 marks. It consists of 4 questions of 4 marks each.
2. Section B consist of 4 questions of 8 marks each. The student has to attempt any 3 questions out of it.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

**Section – A**

**(4 marks each)**

- Q1. What are the Digital signals, Logic Levels, PLAs explain with suitable example?
- Q2. Realize 2 input Ex-OR and Ex-NOR gate using NAND gate only.
- Q3. Minimize the function using K-map method & Implement the same using NAND gate only.  
 $F(A,B,C,D) = \sum m(1,2,3,8,9,10,11,14) + d(7,15)$
- Q4. Convert  $(110101101)_2 = ( \quad )_{10}$   
 $(11011010.110101)_2 = ( \quad )_{16}$

**Section – B**

**(8 marks each)**

- Q5. Draw & explain  $16 \times 1$  Mux using two  $8 \times 1$  Mux and one OR Gate.
- Q6. Draw the Circuit diagram of Full adder & half subtractor.
- Q7. Draw & Explain the JK Flip-Flop. Convert the S-R Flip-Flop to J\_K flip flop.
- Q8. Draw the circuit of BCD adder & perform the function  $(9+6)$  &  $(8+5)$ .

**Section – C**

**(10 marks each)**

- Q9. Explain R-2R ladder network with suitable diagram.
- Q10. Design a 3 Bit up counter using J-K-Flip flop.
- Q11. Discuss the Modelling and Simulation of Moore and Mealy machines.