1. Von Neumann and array processor are different types of computer architecture.

One feature of Von Neumann architecture is that instructions are executed in a linear sequence.

i. Give **three** other features.

1

2

3

[3]

ii. Describe what is meant by array processor architecture.

[2]

iii. Give **one** advantage and **one** disadvantage, other than cost, of using Von Neumann compared with array processor architectures.

Advantage ----------

iv.

v.

vi.

Disdvantage ----------

vii.

viii.

ix. **[2]**

2. Processors following the Von Neumann Architecture use registers.

i. Describe what is meant by the term 'register'.

[2]

ii. Give **one** other feature of the Von Neumann Architecture.

[1]

3. A digital coffee making machine has a CPU that uses the Little Man Computer Instruction Set.

Little Man Computer operates on a computer system based on the Von Neumann Architecture.

i. State **two** features of the Von Neumann architecture.

1

2

v. Describe **one** feature, **not** part of the standard Von Neumann Architecture, which contemporary CPUs may have in order to improve performance.

[2]

END OF QUESTION PAPER

Mark scheme

Question			Answer/Indicative content	Marks	Guidance
1		i	• Single control unit • One instruction at a time • Uses fetch execute **cycle** • Program & data stored together / program & data in same format	3	Accept single ALU Allow FDE Location TV **Examiner's Comments** A significant amount of candidates gave a single processor as a response to this question which was judged to not be sufficient for this level of examination.
		ii	• Single Instruction Multiple Data (SIMD) • Allows same instruction to operate simultaneously on multiple data locations / many ALU's	2	**Examiner's Comments** Well answered by most candidates with almost all getti at least one mark and a large proportion getting both marks.
		iii	*Advantage* • Simpler operating system / easier to program *Disadvantage* • Slower than array processing on large sets of data	2	Disadvantage must be a comparison to an array proces Accept SIMD for array processing **Examiner's Comments** A large number of candidates were of the opinion that "Slower" or "Not as fast" was sufficient for this. It was n
			Total	**7**	
2		i	-Small piece of memory / used for storing data (1) -Within the processor (1)	**2** **AO1.1**	Accept 'location' for MP1 **Examiner's Comment** Most candidates described a register as 'a memory location' with many going on to add 'in the processor' therefore achieving full marks.
		ii	-Single control unit (1) -Single ALU (1) -Follows fetch, decode, execute cycle (1) -Data and Instructions stored in the same memory / format(1) (Max 1)	**1** **AO1.1**	Do not accept use registers – in the question **Examiner's Comment** A number of different correct responses were offered h Most candidates achieved the mark.
			Total	**3**	
3		i	- (Single) Control Unit - (Single) Arithmetic Logic Unit - (Special) registers within CPU - Instructions and Data stored in same area of memory - Instructions and Data stored in same format - A single set of buses / same bus for instructions & data (to connect CPU to Memory and I/O) (1 Mark per -, Max 2)	2 (AO1.1)	Accept acronyms ALU,CU **Examiner's Comments** The majority of candidates answered this question well although some candidates stated that 'instructions and data are stored in the same memory location' more attention to detail is required at this level of study.

		ii	Two separate areas of memory… …one for instructions & one for data./instructions and data can be accessed concurrently. Different (sets of) buses… … one for instructions & one for data./ instructions and data can be accessed concurrently. Pipelining… …whilst an instruction is being executed the next can be decoded and the subsequent one fetched. Use of Cache… …A small amount of high performance memory is (next to the CPU) / which stores frequently used data/instructions Virtual cores/Hyper-threadingTM … …Treating a physical core as two virtual cores. Multiple Cores… …Each core acts as a separate processing unit. Onboard Graphics… …Built in circuitry for graphics processing. (1 Mark for identifying feature, 1 mark for description)	2 (AO1.2)	Accept any reasonable description. Do not accept “64-bit” e.g. Performance boosting mode… …Clock speed can be temporarily increased for performance boost. Out of Order Execution… …Instructions can be executed before earlier ones if the are ready. Super Scalar… …Multiple instructions can be executed simultaneously **Examiner’s Comments** A whole range of features were accepted for this questi Most candidates stated an appropriate feature but som then did not go on to describe how the feature improve performance.
			Total	**4**	