Modul 4(Laporan Akhir 1)

[KEMBALI KE MENU SEBELUMNYA]

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 1. Jurnal

[Kembali]

2. Alat dan Bahan

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class="separator" style="border: 0px none; box-sizing: border-box; clear: both; margin: 0px; padding:
0px; text-align: left;">h. Logicprobe <div class="separator" style="border: 0px none;
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0.1) 1px 1px 5px; box-sizing: border-box; margin: 0px; max-width: 100%; padding: 0px; position:

relative;" width="220" /> Logic Probe

3. Rangkaian Simulasi

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 gambar rangkaian pada percobaan 1 menggunakan De Lorenzo

 4. Prinsip Kerja Rangkaian

[Kembali]

     Pada percobaan 1 ini dirangkai suatu rangkaian Shift Register (register geser) keluaran output 4 bit dengan perwakilan output logicprobe. Pada rangkaian shift register keluaran 4 bit ini berarti menggunakan 4 buah IC J-K flip flop sebagai perwakilan 1 bit keluaran untuk 1 buah J-K flipflop.
     Pada rangkaian ini memiiki 4 input masukan dari J-K flip flop dan 4 input keluaran dari J-K flip flop dimana akan terjadi proses operasi SISO, SIPO, PISO, dan PIPO pada rangkaian sesuai pengaturan switch dan kondisi.Maka pada prosesnya akan terjadi sistem kerja serial dan paralel yang dimana pada rangkaian akan terjadi perwakilan dari penggeseran pada sistem serial maupun serempak pada sistem paralel baik itu masukan maupun keluaran suatu biner yang dimana pergeseran maupun serempak pada sistem serial dan paralel ini akan mewakili MSB dan LSB dari 4

bit binner masukan dan keluaran. Terjadinyam proses input dan output logika pada rangkaian ini juga berarti bahwa proses terjadinya register geser ini dapat menyimpan memori sementara pada masukan menuju keluaran bit ke-4 dari dearah lingkup keluaran 4 bit. <br style="font-size: small;" />
 5. Video Rangkaian

[Kembali]
 <iframe allowfullscreen="" class="BLOG_video_class" height="266" src="https://www.youtube.com/embed/F9ecXSArUEo" width="320" youtube-src-id="F9ecXSArUEo"></iframe>
 video penjelasan rangkaian percobaan 1

 6. Analisa

[Kembali]

Soal analisa yang diberikan ada 2 buah yakni:

 7. Link Download

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