<table>
<tr><td rowspan="3">Course Information</td><td>Course Title</td><td colspan="2">Digital Integrated Circuit Design</td><td>Course ID</td><td>ICE4006</td></tr>
<tr><td colspan="3"></td><td>(Course Type)</td><td></td></tr>
<tr><td colspan="2">(Credit/ hours per week)</td><td>3/3</td><td>Version (date)</td><td></td></tr>
<tr><td>Instructor</td><td colspan="5">Prof. Hanho Lee</td></tr>
<tr><td>Course Learning Objective</td><td colspan="5"><table>
<tr><th colspan="2">Course Objectives</th><th>Relation with Program Outcomes</th></tr>
<tr><td>1</td><td>Ability to solve information and communication engineering problems using mathematics, basic science, and engineering knowledge, and information technology.</td><td>PO 1</td></tr>
<tr><td>2</td><td>Ability to analyze information and communications engineering data and identify given facts or hypotheses through experiments</td><td>PO 2</td></tr>
<tr><td>3</td><td>Ability to define and formulate information and communication engineering problems</td><td>PO 3</td></tr>
<tr><td>5</td><td>Ability to design systems, elements, processes, etc. in consideration of realistic limitations of information and communication engineering</td><td>PO 5</td></tr>
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<tr><td>Course Description</td><td colspan="5">As applied to digital integrated circuits, the CMOS transistor is studied in depth - from its fabrication to its electrical characteristics. Combinational, sequential, and dynamic logic circuits are considered. SPICE is used as both an analysis and design tools. Semiconductor memory circuits are also discussed. CAD Tools for circuit design, layout, extraction, and simulation will be used for Labs and projects.
The emphasis of this class is hands-on transistor level circuit and chip layout design. During the first six weeks, you will complete a series of labs for circuit design, simulation, chip layout and performance analysis. Along the way, you will master a variety of CAD tools and design techniques. Based on this experience, you will carry out a final design project.</td></tr>
<tr><td>Course Outcomes</td><td colspan="5"><table>
<tr><th>NO</th><th>Details</th></tr>
<tr><td></td><td>Learn basic theory and design methods for designing digital logic circuits such as Inverter, NAND, NOR, AND, OR gate as CMOS transistors, and cultivate design capabilities and performance analysis methods for designing addition, subtraction, and multiplier as CMOS transistors through design experiments and projects</td></tr>
<tr><td></td><td>Development of the ability to design logic circuits, adders, subtractors, multipliers, and memories of digital systems using the latest information on digital integrated circuit design using transistors, existing research results, and design CAD tools</td></tr>
<tr><td></td><td>In consideration of performance limitations such as area, clock speed, power consumption, etc., the analysis capability is cultivated by designing and simulating digital integrated circuits using Hspice, and the layout design capability using the magic layout CAD tool</td></tr>
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<tr><td>(Prerequisites)</td><td colspan="5"></td></tr>
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(Recommended Courses after This Course)							
Course Software or Tool							
Textbook	Title		Authors	Publisher	Place	Year	ISBN
	Integrated Circuit Design		Neil H. E. Weste			2011	9780321696946
references							
Lecture type	Lecture						
(Notes)							
(Evaluation Criteria)	(Attendance)	5%	(Quiz)	0%	(Lab Assignment)	5%	(Etc.) 10%
	(Mid-term Exam)	40%	(Final Exam)	40%	(Total)		100 %
(Methods of Evaluation)	Assessment will be made on the basis of written examination and assignment.						

Weekly Topical Outline of Course		
(1st Week)	Topic	Introduction
	Contents	VLSI, digital Integrated circuit technology history, chip design methodology
	Assignment	
(2nd Week)	Topic	Fabrication of MOS circuits, Manufacturing Process.
	Contents	CMOS Processing Technology, Semiconductor processing step, processing and design layout matching
	Assignment	
(3rd Week)	Topic	RISC Microprocessor example
	Contents	RISC Microprocessor example
	Assignment	
(4th Week)	Topic	MOS Transistor Theory and Models for Resistance and Capacitance calculation
	Contents	MOS Transistor Theory and Models for Resistance and Capacitance calculation
	Assignment	
(5th	Topic	CMOS inverter, Logical Effort

Week)	Contents	MOS Inverter operation/Design/Layout/Capacitance characteristics , Logical Effort
	Assignment	
(6th Week)	Topic	Combinational circuits and CMOS logic families
	Contents	Static CMOS design: Complementary CMOS logic, pass-transistor logic NAND, NOR, EXOR gate design with CMOS,Transistor sizing Power consumption in CMOS gates
	Assignment	
(7th Week)	Topic	Midterm Exam
	Contents	
	Assignment	
(8th Week)	Topic	Combinational circuits and CMOS logic families
	Contents	Dynamic CMOS logic
	Assignment	

(9th Week)	Topic	Sequential circuits and layout
	Contents	D-FF circuit with CMOS,Timing consideration for D-FF design, clocked latch, Single phase clocked D-FF
	Assignment	
(10th Week)	Topic	Design methodology and tools
	Contents	Design methodology and tools
	Assignment	
(11th Week)	Topic	Datapath subsystems
	Contents	
	Assignment	
(12th Week)	Topic	Timing Issues in Digital Circuits
	Contents	
	Assignment	
(13th Week)	Topic	Design Arithmetic Building Blocks

	Contents	Arithmetic Building block deisgn
	Assignment	
(14th Week)	Topic	Designing Memory and Array Structures
	Contents	DRAM, SRAM circuit, Memory Cell, Peripheral Circuit
	Assignment	
(15th Week)	Topic	Final examination
	Contents	
	Assignment	
(16th Week)	Topic	
	Contents	
	Assignment	