Google Summer of Code

SUMMER 2023

Mentor

Jose Renau

Project Proposal

Enhancing and Validating LiveHD's Power Modeling Flow

Applicant

Shahzaib Kashif

Table of Contents

Title: Enhancing and Validating LiveHD's Power Modeling Flow

Abstract:

LiveHD is a powerful open-source framework for hardware design that provides various functionalities such as synthesis, simulation, and power estimation. Recently, a new flow has been introduced to estimate power consumption based on netlists and VCD activity rates. This project aims to improve the stability and functionality of the power modeling flow by debugging the existing implementation, running it on various blocks, and developing a systematic validation methodology.

Personal Information:

- Full Name: Shahzaib Kashif
- Email Address: shahzaibceo@gmail.com
- University: Usman Institute of Technology (UIT)
- Major: Software Engineering

Project Proposal:

Background:

Hardware design is a rapidly evolving field that demands continuous optimization and innovation. Power consumption has become a crucial factor in the design process due to the increasing need for energy-efficient devices in various applications. As a result, accurate power estimation has become an essential step in hardware design to predict the power consumption of integrated circuits and systems.

LiveHD is an open-source framework that aims to address the challenges of modern hardware design by providing a comprehensive solution, including synthesis, simulation, and power estimation. The recent addition of power modeling flow in LiveHD marks a significant step towards enabling designers to estimate power consumption based on netlists and VCD activity rates. This new flow brings together the core functionalities of LiveHD to deliver an all-in-one solution for hardware designers.

However, as the power modeling flow is a recent addition to LiveHD, it requires further refinement and validation to ensure its accuracy, stability, and performance. Moreover, expanding its compatibility with diverse netlists and VCD files is essential for wider adoption by the hardware design community. Addressing these challenges and enhancing the existing

documentation will facilitate the adoption of LiveHD's power modeling flow and contribute to the development of energy-efficient hardware designs.

Objectives:

1. Debug the current implementation of the power modeling flow in LiveHD.
2. Expand the range of supported netlists and VCD files.
3. Develop a systematic validation methodology to ensure accurate power estimation.
4. Improve the overall performance and robustness of the power modeling flow.
5. Enhance the existing documentation to facilitate user adoption.

Expected Outcomes:

1. A more reliable and accurate power modeling flow in LiveHD.
2. A broader range of supported netlists and VCD files.
3. A comprehensive validation methodology to ensure the accuracy of power estimates.
4. Improved performance and robustness of the power modeling flow.
5. Updated documentation to help users better understand and utilize the power modeling flow.

Project Plan and Timeline:

Weeks 1-2: Familiarize with LiveHD and power modeling flow

- Study the LiveHD framework, its components, and functionality.
- Understand the current implementation of the power modeling flow.
- Identify possible areas of improvement.

Weeks 3-4: Debug the existing implementation

- Debug the power modeling flow.
- Identify and fix issues related to netlist parsing, VCD file handling, and power estimation.
- Test the updated implementation on a range of netlists and VCD files.

Weeks 5-6: Develop a systematic validation methodology

- Design a methodology to validate the accuracy of power estimation results.
- Implement the validation methodology.
- Compare the results with other power estimation tools to ensure the accuracy of the LiveHD power modeling flow.

Weeks 7-8: Optimize the power modeling flow

- Improve the performance and robustness of the power modeling flow.
- Optimize the flow to handle larger netlists and VCD files efficiently.

- Test the updated implementation on a range of netlists and VCD files.

Weeks 9-10: Enhance documentation and user support

- Update the existing documentation with more details on the power modeling flow.
- Add examples and use-cases to help users better understand the flow.
- Create tutorials or guides for users to get started with the power modeling flow.

Weeks 11-12: Finalize the project and prepare for submission

- Perform extensive testing on the updated power modeling flow.
- Address any remaining issues or bugs.
- Prepare the final report and submit the project.

By the end of the project, the LiveHD power modeling flow will be more stable, accurate, and efficient, providing users with a reliable and comprehensive solution for power estimation.

Skills and Experience:

- RISC-V
- Scala
- Constructing Hardware in Scala Embedded Language (CHISEL) HDL
- C language
- C++17
- SoC Designing
- Bash Scripting
- Makefiles
- Functional Programming
- Object Oriented Software Engineering
- Embedded Software Programming
- FPGA Emulation
- Cloud FPGA Emulation (AWS-FPGA)

Why I'm the Right Candidate:

Throughout my academic career, I have been deeply engaged in the hardware design domain, starting from my undergraduate program's second year. My experience spans designing single-cycle and five-stage pipelined cores from scratch using CHISEL HDL, to FPGA prototyping using the Vivado Design Suite. This has allowed me to develop a comprehensive understanding of the synthesis, implementation, and bitstream generation processes.
Throughout my journey, I have honed my skills using numerous Electronic Design Automation (EDA) tools, both licensed and open-source, such as Foss for FPGAs (F4PGA) and SymbiFlow. My expertise extends beyond merely using these tools; I have also created my own custom EDA tools for rapid bitstream and GDS generation, sh+owcasing my ability to adapt and innovate in the field.

Moreover, my experience includes designing a complete System-on-Chip (SoC) Generator for my undergraduate Final Year Project (FYP). The SoC generated from this project was further processed and submitted to Google's MPW Shuttle program, utilizing open-source SkyWater PDKs for tape-out. During this phase, I gained valuable knowledge about the GDS generation process, including netlist generation, power modeling, and the intricacies of GDS generation.
In summary, my extensive experience in hardware design, proficiency in EDA tools, and ability to innovate demonstrate my qualifications as the right candidate for the hardware design domain. I am confident in my ability to contribute significantly to any team or project in this field.

Mentor: Jose Renau

By refining and validating LiveHD's power modeling flow during the GSoC program, I aspire to contribute to the development of energy-efficient hardware designs and gain valuable experience working with state-of-the-art hardware design tools and methodologies.