Mazad Shaheriar Zaveri, Ph.D.
Associate Professor, School of Engineering and Applied Science (SEAS), Ahmedabad University

Ex. Associate Professor, Department ICT, SoT, Pandit Deendayal Petroleum University (PDPU)
Ex. Assistant Professor, School of Engineering and Applied Science (SEAS), Ahmedabad University
Ex. Assistant Professor, Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT)

EDUCATION

Doctor of Philosophy (Ph.D.) - *Electrical and Computer Engineering* (December 2009) **GPA** 3.9/4.0

- *Portland State University, Portland, Oregon, USA*
  - **PhD Dissertation Title:** CMOL/CMOS Hardware Architectures and Performance/Price for Bayesian Memory – The Building Block of Intelligent Systems
  - **Dissertation Advisor:** Prof. Dan W. Hammerstrom (Ph.D.), IEEE fellow, Professor Emeritus, PSU
    Previously: Ex. Associate Dean for Research, Portland State University (PSU), Oregon, USA, and Ex. Program manager at Microsystems Technology Office, in DARPA.

Master of Science in Engineering (M.S.E) - *Electrical Engineering* (2003) **GPA** 3.8/4.0

- *Arizona State University, Tempe, AZ, USA*
  - **Specialization:** Digital CMOS VLSI

Bachelor of Engineering (B.E.) - *Instrumentation and Control Engineering* (2000) Gold Medalist

- *Gujarat University, India*

RESEARCH INTERESTS

- ***Digital CMOS VLSI design:***
  - Design/implementation, simulation, and characterization [investigation of performance, power and area; and targeting low power-delay product (PDP)] of digital CMOS VLSI circuits and sub-system blocks:
    - CMOS transistor/circuit-level implementation of Arithmetic-Logic/data-path modules of the ALU, such as: optimized multi-bit tree-adders and multipliers
    - CMOS transistor/circuit-level and RTL implementations of specialized blocks: CORDIC, neural networks; FPGA implementations of neural networks/algorithms (part of edge computing and high-speed computing or accelerators)
- ***Computer Engineering:***
  - Develop Computer Engineering based solutions for:
    - Drone based data collection for Indian Road Traffic and baseline algorithms for vehicle detection and trajectory extraction
    - Road Traffic & Safety Audit using Computer Vision
      - Road Infrastructure Audit
      - Defensive Driving Behavior and Traffic Analytics
      - Detailed traffic violations** and driving trajectory analyses (using Machine-Learning and Computer Vision based techniques).

      ** MVA-MVDR (Motor Vehicles Act 1988 - Motor Vehicle Driving Regulation 2017)
    - Youtube link to our video: https://www.youtube.com/watch?v=3NYZnBAcPuY

ACADEMIC WORK (Teaching and Research) EXPERIENCE (Post Ph.D.) : 16 Years

Associate Professor (December 2020 onwards) at *School of Engineering and Applied Science, Ahmedabad University, India*

- UG core courses:
  - Computer Organization and Architecture (Semester 4, CSE) [Core for BTech]
  - Advanced Computer Arithmetic: Algorithms and Sub-systems [Elective BTech/MTech]
  - VLSI Design [Elective BTech/MTech]

Associate Professor (December 2018 to December 2020) at Dept of ICT, *School of Technology, PDPU, Gandhinagar, India*

- UG core courses:
  - Embedded Systems (Semester 6, ICT) [Core for BTech]
  - Computer Organization and Programming (Semester 5, ICT) [Core for BTech]
  - Digital VLSI Circuits and HDL (Semester 7, ICT) [Core for BTech]
  - Digital Logic and Design (Semester 3, CE) [Core for BTech]

Assistant Professor (December 2014 to Nov 2018) at *School of Engineering and Applied Science, Ahmedabad University, India*

- UG core courses taught:
  - Digital Design (Winter 2015 to 2018)
- UG/PG specialization core/electives courses taught:
  - VLSI Design (Monsoon 2014 to 2018) [Core for BTech Specialization / Elective for MTech]
  - VLSI Sub-system Design (Winter 2014 to 2018) [Elective for BTech/MTech]
  - (Project based course) Circuit Characterization of VLSI Sub-systems (Monsoon 2015 to 2018) [Elective for BTech/MTech]
- PhD-level self-study courses mentored:
  - Low-Power VLSI Sub-systems (Winter 2014-15)
  - Systems Approach (Winter 2014-15)

Visiting Faculty (Jan. 2014 to May 2014) at *Indian Institute of Information Technology, Vadodara* (Campus: GEC Gandhinagar)

- UG courses taught:
  - EL 102 Basic Electronic Circuits [Core for BTech]

Assistant Professor (June 2010 to November 2014) at *Dhirubhai Ambani Institute of Information and Communication Technology* (DA-IICT)*, Gandhinagar, India*

- UG core courses taught:
  - EL 114 Digital Logic Design (Winter 2011 to 2013) [Core for BTech]
  - EL 103 Basic Electronic Circuits (Autumn 2013 to 2014) [Core for BTech]

- PG specialization-core courses taught:
  - EL 511 VLSI Design (Autumn 2010 to 2013) [Core for MTech]
  - EL512 VLSI Sub-system Design (Winter 2013 to 2014) [Core for MTech]

WORK/RESEARCH EXPERIENCE (During Ph.D.) : 4 Years 6 Months

Research Assistant (Sept. 2003 to Sept. 2004, and Sept. 2005 to Sept. 2009) at *Oregon Health and Science University*, and *Portland State University*, *Oregon*, *USA*

- Worked on several topics:
  - Performance/price investigation of application-specific CMOS and emerging hybrid nanoelectronics technology – CMOL based architectures, including digital and mixed-signal circuits. The application/models for the hardware implementation included: Artificial neural networks, associative memory, spiking neural networks, biologically-inspired computational models and algorithms, Pearl's belief propagation/inference algorithm, etc.
  - Formal performance/price assessment methodology for exploring the hardware design space was studied, which included: algorithm – model, specifications, and computational requirements; circuit component/block-level performance/price modeling; hardware system-level performance/price estimation.
  - Performance/price estimates for building large-scale, possibly cortex-scale, intelligent computing systems using CMOS and CMOL technology, consisting of millions of ASIC processing nodes, each with distributed conventional/CMOL memory, and/or CMOS/CMOL based array structures with inherent storage and mixed-signal computational capabilities.
- Research assistantship was funded through the following grants/awards:
  - **Grant No.** 801884-BS from the U.S. Defense Advanced Research Projects Agency (DARPA), subcontract to HRL (Hughes Research Laboratories); Under **DARPA program**: *Systems of Neuromorphic Adaptive Plastic Scalable Electronics* (SyNAPSE).
  - **Grant No.** CCF-829947 from the National Science Foundation, USA. **Grant title**: *EMT/MISC Nanogrid Implementation of Massively Parallel Algorithms*; Under **NSF program**: *Emerging Models and Technologies*. URL: http://www.nsf.gov/awardsearch/showAward.do?AwardNumber=0829947
  - **Grant No.** ECS-0408170 from the National Science Foundation, USA. **Grant title**: *Nano-scale Devices – Looking at Alternative Models*; Under **NSF program**: *Design Auto. for Micro & Nano Systems, Electronics, Photonics, & Device Technologies*. URL: http://www.nsf.gov/awardsearch/showAward.do?AwardNumber=0408170
  - **Grant No.** CCF-0508533 from the National Science Foundation, USA. **Grant title**: *NER/SNB Implementing Nano-scale, Hierarchical, Distributed Memories with CMOL (Cmos / MOLecular) Circuits*; Under **NSF program**: *Nano-scale Exploratory Research*. URL: http://www.nsf.gov/awardsearch/showAward.do?AwardNumber=0508533
  - **Grant No.** F19628-02-C-0080 from the U.S. Air Force Research Laboratory (AFRL), Hanscom - AFB, MA, subcontract to Max-Viz Inc. Portland, OR; **Grant title**: *Real-time Sensory Image Fusion for Enhanced Vision System for Aircraft Landing Guidance*.

Teaching Assistant (Sept. 2004 to June 2005) at *Oregon Health and Science University*, and *Portland State University*, *Oregon*, *USA*

- Conducted laboratory for courses: Electrical Circuits Laboratory; Signals and Systems Laboratory; Computer Organization and Design; Advanced Logic Design

PUBLICATIONS

Journal Papers

1. Mazad Zaveri and D. Hammerstrom, "CMOL/CMOS implementations of Bayesian polytree inference: Digital & mixed-signal architectures and performance/price," *IEEE Transactions on Nanotechnology*, vol. 9(2), pp. 194-211, Mar. 2010. DOI: https://doi.org/10.1109/TNANO.2009.2028342 **(IEEE Xplore, SCOPUS, WoS)**
2. Mazad Zaveri and D. Hammerstrom, "Performance/Price Estimates for Cortex-Scale Hardware: A Design Space Exploration," *Neural Networks* (Official Archival Journal of the *International Neural Network Society*, the *European Neural Network Society*, and the *Japanese Neural Network Society*), vol. 24(3), April 2011, **Elsevier**, pp.291-304. DOI: https://doi.org/10.1016/J.NEUNET.2010.12.003 **(SCOPUS, WoS)**
3. Pavan Vyas and Mazad Zaveri. "Verilog implementation of a node of hierarchical temporal memory," *Asian Journal of Computer Science and Information Technology*, vol. 3(7), pp. 103-108, July 2013. (ISSN: 2249-5126)
4. Nilay Mehta, Mazad Zaveri, "Investigation of Communication Schemes for ANN Implementation - Multiple Processing nodes (Based on FPGA/u-controller Boards)," *Journal of Maharaja Sayajirao University of Baroda (Science and Technology)*, Feb. 2017. (ISSN: 0025-0422)
5. Manan Mewada, Mazad Zaveri, Rajesh Thakker, "Improving the performance of transmission gate and hybrid CMOS Full Adders in chain and tree structure architectures", *Integration*, vol. 69, November 2019, **Elsevier**, pp. 381-392. DOI: https://doi.org/10.1016/j.vlsi.2019.09.002 **(SCOPUS, SCIE)**
6. Manan Mewada, Mazad Zaveri, Ratnik Gandhi, Rajesh Thakker, "Transmission Gate and Hybrid Cmos Full Adder Characterization and Power-Delay Product Estimation Based on Mathematical Model", *Procedia Computer Science*, vol. 171, June 2020, **Elsevier**, pp. 999-1008. DOI: https://doi.org/10.1016/j.procs.2020.04.107 **(SCOPUS)**
7. Ankur Changela, Mazad Zaveri, Deepak Verma, "FPGA implementation of high-performance, resource-efficient Radix-16 CORDIC rotator based FFT algorithm", *Integration*, vol. 73, July 2020, **Elsevier**, pp. 89-100. DOI: https://doi.org/10.1016/j.vlsi.2020.03.008 **(SCOPUS, SCIE)**
8. Ankur Changela, Mazad Zaveri, Deepak Verma, "Mixed-Radix, Virtually Scaling-Free CORDIC Algorithm Based Rotator for DSP Applications", Integration, **Elsevier**, May.2021. **(SCOPUS, SCIE)** DOI: https://doi.org/10.1016/j.vlsi.2021.01.005
9. Ankur Changela, Mazad Zaveri, Deepak Verma, "A comparative study on CORDIC algorithms and applications", Journal of Circuits, Systems and Computers, **World Scientific**, Vol. 32, No. 5 (October 2022), 2330002-47 pages.
   DOI: https://doi.org/10.1142/S0218126623300027
10. Ankur Changela, Mazad Zaveri, "A new angle set based absolute scaling-free reconfigurable CORDIC algorithm", Circuits, Systems & Signal Processing **(Springer)**, July 2023.
    DOI: https://doi.org/10.1007/s00034-023-02452-w
11. Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "Vision-based Investigation of Road Traffic and Violations at Urban Roundabout in India using UAV Video: A Case Study", Transportation Engineering **(Elsevier)**, October 2023, DOI: https://doi.org/10.1016/j.treng.2023.100207
12. Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "Evaluating defensive driving behaviour based on safe distance between vehicles: A case study using computer vision on UAV videos at urban roundabout", Multimodal Transportation, **(Elsevier), vol.** 4 (3), pp. 1-22, December 2024, DOI: https://doi.org/10.1016/j.multra.2025.100227

Book Section/Chapter

1. C.-H. Luk, M. S. Zaveri, D. Hammerstrom, and R. J. Kerr, "Vision-Based Hazard Detection," in *Intelligent Engineering Systems Through Artificial Neural Networks: Smart Engineering System Design*, vol. 16, C. H. Dagli, A. L. Buczak, D. L. Enke, M. Embrechts, and O. Ersoy, Eds. ASME Press:NY, 2007, pp. 439-444. DOI: https://doi.org/10.1115/1.802566 **(AMSE)**
2. M. S. Zaveri and D. Hammerstrom, "Chapter 4. CMOL/CMOS Implementations of Bayesian Inference Engine: Digital & Mixed-signal Architectures and Performance/price – A Hardware Design Space Exploration" in *CMOS Processors and Memories*, Kris Iniewski Ed., Aug. 2010, **Springer**, pp. 97-138. DOI: https://doi.org/10.1007/978-90-481-9216-8_4 **(WoS)**
3. Manan Mewada, Mazad Zaveri, Anurag Lakhlani, "Estimating the Maximum Propagation Delay of 4-bit Ripple Carry Adder Using Reduced Input Transitions," in *VLSI Design and Test*, Book series: *Communications in Computer and Information Science*, Kaushik B., Dasgupta S., Singh V. (Eds.), vol. 711, Dec. 2017, **Springer**, pp 15-23. DOI: https://doi.org/10.1007/978-981-10-7470-7_2 **(WoS)**

Conference Papers/Presentations (and posters)

1. C.-H. Luk, M. S. Zaveri, D. Hammerstrom, and R. J. Kerr, "Vision-Based Hazard Detection," in *Conf. on Artificial Neural Networks in Engineering (ANNIE)*, St. Loius-MI, Nov. 2007.
2. C. Gao, M. S. Zaveri, and D. Hammerstrom, "CMOS / CMOL architectures for spiking cortical column," in *IEEE World Congress on Computational Intelligence – Int. Joint Conf. on Neural Networks (WCCI-IJCNN)*, Hong Kong, June 2008, pp. 2442-2449. DOI: https://doi.org/10.1109/IJCNN.2008.4634138 **(IEEE Xplore, SCOPUS, WoS)**
3. D. Hammerstrom and M. S. Zaveri, "Bayesian memory, a possible hardware building block for intelligent systems," in *AAAI Fall Symposium Series on Biologically Inspired Cognitive Architectures* , Arlington, VA, TR FS-08-04, Nov. 2008, AAAI Press, pp. 81. URL: https://www.aaai.org/Papers/Symposia/Fall/2008/FS-08-04/FS08-04-021.pdf **(SCOPUS)**
4. M. S. Zaveri and D. Hammerstrom, "Prospects for Building Cortex-Scale CMOL/CMOS Circuits: A Design Space Exploration," in *IEEE Norchip Conference*, Trondheim-Norway, Nov. 2009. DOI: https://doi.org/10.1109/norchp.2009.5397858 **(IEEE Xplore, SCOPUS)**
5. M. S. Zaveri, D. Voils, and D. Hammerstrom, "Using computational neuroscience to build better computers," (poster) in *The Science and Business of the Brain: Oregon Innovation Showcase*, I-C-Oregon, Portland-OR, Nov. 2009.
6. N.B. Ambasana and M. S. Zaveri, "Analysis of increased parallelism in FPGA implementation of neural networks for environment/noise classification and removal," in *Nirma University International Conference on Engineering*, Ahmedabad, Dec. 2012, pp.1-5. DOI: https://doi.org/10.1109/NUICONE.2012.6493242 **(IEEE Xplore, SCOPUS)**
7. Chhaya, Vaibhav and Zaveri, Mazad S."CMOS Current-based Mixed-Signal Architecture for Vector-Matrix Multiplication", in *National Conference on Recent Advances in Communication, Control and Computing Technology*, Surat, March, 2012, pp. 137-143. (Benison Education, ISBN: 978-81-88894-34-5)
8. Shalini Rankawat, Mansi Rankawat, Rahul Dubey, Mazad Zaveri,"Robust Heart Rate Estimation From Multiple Cardiovascular and Non-cardiovascular Physiological Signals Using Signal Quality Indices and Kalman Filter", in *International Conference on Communications and Quantum Systems*, Singapore, Jan. 2015. URL: https://publications.waset.org/abstracts/17506/pdf
9. Tejas Dalal, Mazad Zaveri, "Hardware Implementation of MLP and RBF Neural Networks onto Multiple Processing Nodes", in *International Conference on Multidisciplinary Research & Practice*, paper ID 220, AMA Ahmedabad, November 2014. Proceedings appeared in *International Journal of Research and Scientific Innovation*, vol. 1(7), Nov. 2014, pp. 132-137. (ISSN: 2321-2705)
10. Manan Mewada, Mazad Zaveri, "An Improved Input Test Pattern for Characterization of Full Adder Circuits", in *International Conference on Multidisciplinary Research & Practice*, paper ID 152, AMA Ahmedabad, December 2015. Proceedings appeared in *International Journal of Research and Scientific Innovation*, vol. 3(1), Dec. 2015, pp. 222-226. (ISSN: 2321 – 2705)
11. Manan Mewada, Mazad Zaveri, "A Low-Power High-Speed Hybrid Full Adder", in *International Symposium on VLSI Design and Test (VDAT)*, IIT Guwahati-Assam, 24 - 27 May 2016. DOI: https://doi.org/10.1109/ISVDAT.2016.8064900 **(IEEE Xplore, SCOPUS, WoS)**
12. Manan Mewada, Mazad Zaveri, "An Input Test Pattern for Characterization of a Full-Adder and n-bit Ripple Carry Adder", in *International Conference on Advances in Computing, Communications and Informatics*, September 2016, LNMIIT-Jaipur, September 2016. DOI: https://doi.org/10.1109/ICACCI.2016.7732055 **(IEEE Xplore, SCOPUS, WoS)**
13. Nilay Mehta, Mazad Zaveri, "Investigation of Communication Schemes for ANN Implementation - Multiple Processing nodes (Based on FPGA/u-controller Boards)" in (ISTE, UGC merged scheme funded) *International Conference on Advances in Computing, Communication, and Informatics*, held on 25-Feb-2017, at the Dept. of CSE, Maharaja Sayajirao University, pp. 20-26. Proceedings appeared in MSU journal. (Best paper award in Session 1-2)
14. Manan Mewada, Mazad Zaveri, Anurag Lakhlani, "Estimating the Maximum Propagation Delay of 4-bit Ripple Carry Adder using Reduced Input Transitions," in *International Symposium on VLSI Design and Test (VDAT)*, IIT-Roorkee, June-July 2017. DOI: https://doi.org/10.1007/978-981-10-7470-7_2 Proceedings appeared as book chapter. **(WoS)**
15. Ankur Changela, Mazad Zaveri, Anurag Lakhlani, "FPGA Implementation of Asynchronous Mousetrap Pipelined Radix-2 CORDIC Algorithm," in *IEEE International Conference on Current trends towards Converging Technologies*, Coimbatore - India, 1 - 3 March 2018, PID 7092. DOI: https://doi.org/10.1109/ICCTCT.2018.8551112 **(IEEE Xplore, SCOPUS)**

16. Ankur Changela, Mazad Zaveri, Anurag Lakhlani, "ASIC Implementation of High Performance Radix-8 CORDIC Algorithm," (IEEE sponsored) *International Conference on Advances in Computing, Communications and Informatics*, Bangalore - India, 19 – 22 September, 2018. DOI: https://doi.org/10.1109/ICACCI.2018.8554883 **(IEEE Xplore, SCOPUS, WoS)**
17. Manan Mewada, Mazad Zaveri, Ratnik Gandhi, Rajesh Thakker, "Transmission Gate and Hybrid Cmos Full Adder Characterization and Power-Delay Product Estimation Based on Mathematical Model", in *Third International Conference on Computing and Network Communications (CoCoNet'19)*, IIITM-K Trivandrum, Kerala,, December 18-21, 2019. (Proceedings appeared in journal) **(SCOPUS)**
18. Mehul Raval, Tolga Kaya, Mazad Zaveri, Paawan Sharma, "Experiments with Multinational Cross-Course Projects through Blended Learning", IEEE TALE2020 – An International Conference on Engineering, Technology and Education, Dec. 2020. pp.65-70. DOI: https://doi.org/10.31219/osf.io/ph3e5 **(IEEE Xplore)**
19. Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "U-UTM: A Cyber-Physical System for Road Traffic Monitoring Using UAVs," 18th IEEE InternationalConference on Vehicular Electronics and Safety (ICVES), Ahmedabad, India, December 2024, pp. 1-6, DOI: https://doi.org/10.1109/ICVES61986.2024.10927911 **(IEEE Xplore)**
20. Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, (Poster) "Traffic investigation at roundabout using UAV", 18th IEEE InternationalConference on Vehicular Electronics and Safety (ICVES), Ahmedabad, India, December 2024.

Dissertation as Book

1. M. S. Zaveri, "CMOL/CMOS hardware architecture and performance/price for Bayesian memory - The building block of intelligent systems," PhD dissertation, Dept. of Electrical and Computer Engineering, Portland State University, Nov. 2009. (ProQuest-UMI: Pub No.: 3391676) (http://www.worldcat.org/oclc/550656475)

DATA REPOSITORY - Copyright Mazad Zaveri and Ahmedabad University

Data Repository for Road Safety Audit and Traffic Analytics

Drone based aerial data (images / videos) have been collected in the past few months (under URBSEASI21A3 Ahmedabad University: Seed Grant), and a summary of the same is presented below:
[Status as on May 2022]

- Videos of Roundabouts:
  - (File No. 9,10,11,12) Near Gulmohar party plot, Thaltej-Hebatpur Road [Traffic violations are captured]
  - (File No. 18,19,20) Bakrol Circle, On SP Ring Road [Traffic Analytics] [Traffic violations are captured]

- Videos of Junctions/Intersections:
  - (File No. 13,14,15,16,17) Nr. Time Square Grand Building, Sindhu Bhavan Road [Signals working] [Traffic violations care captured]
  - (File No. 30,31,32,33,34) Pakwan Cross Road [Signals working] [Traffic Analytics] [Traffic violations are captured]
  - (File No. 35,36,37,38) Nr. Magson, Sindhu Bhavan Road [Signals working] [Traffic Analytics]

- Videos of T-Sections:
  - (File No. 2,3,4,5,6,7,8) Nr. Taj Hotel, On SP Ring Road [Traffic Analytics] [Traffic violations are captured]
  - (File No. 39,40,41,42) Road in front of AlphaOne Mall, Nr. Vastrapur Lake [Road Marking Violations]

- Videos related to analyses of object dimensions:
    - (File No. 31 to 42) At SEAS parking ground [To study type of vehicles - dimensions versus height]
    - (File No. 22 to 24) At SEAS football ground [To estimate camera calibrations in all parts of FOV]
- MVDR Road Traffic Violation Dataset(244 traffic violations in dataset; for 131 programmed MVDR rules)
- Dataset for give-way traffic violations and driver behavior at T-junctions(19.9GB videos)
    - (File No. 59 to 66) Nr. Taj Hotel, On SP Ring Road [Traffic Analytics] [Traffic violations are captured]
- Dataset for Ground-Sampling-Distance Modeling and Camera Calibration(6.24GB videos collected for railway track and road lane marking, with altitude and orientation changes)
    - (File No. 67 to 74) Nr. Skyone, Canal Road Shilaj (Nr. Ambli Railway station)

Videos of our work:

- Youtube link explaining our initial work on road/traffic drone data collection and Computer Vision based analyses: https://www.youtube.com/watch?v=3NYZnBAcPuY
- Link to videos showing our work on traffic violation detection:
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptKvLOA9aOu-UltztYyAU9jY
- Link to videos showing driver ratings based on defensive driving parameters:
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptLd-qfA42Mbb-CdKLR-d25G
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptJePV2ljtntipe6j7bH_Ant
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptLws_o6S3fOZ-HuWrHf8-o2
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptI9WT3lvAIsuZxo3DrByMy6
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptK5OJPyvC-eZlnKHunZ-okh
- Link to videos for Ground-Sampling-Distance (GSD) mapping:
    - https://www.youtube.com/playlist?list=PLFa7TK4V1ptJVWpImpnv7cF_Y0r1-3Ojf

STUDENT THESES/PROJECTS GUIDED

Ph.D. Theses Guided (Ongoing)

[Ahmedabad University]

1. Anurag Lakhlani, working on “Low-Power Neuromorphic Architectures”
    - Status: Student completed RPS2 in Feb. 2025.
2. Yagnik Bhavsar, working on “Applications of Computer vision in Road Safety and Traffic Violations”
    - Status: Student has completed RPS3 in Dec. 2024

Ph.D. Theses Guided (Completed)

[Ahmedabad University]

1. Manan Mewada, PhD defense successfully completed on 3-Feb-2020. Thesis title: “A Low Power-Delay Product Hybrid CMOS Full Adder Design for Chain and Tree Structures and Its Characterization”
    - Now working at Pronesis Tech. (previously with Intel Corporation & Sankalp Semiconductors)
2. Ankur Changela, PhD defense successfully completed on 6-October-2021. Thesis title: “FPGA Implementation of High-Radix and Mixed-Radix, Scaling-Free CORDIC Algorithms for FFT Implementation”
    - Now working as faculty at Indus University / Pandit Deendayal Petroleum University

M.Tech. Theses Guided (Completed)

[DAIICT]

1. Nikita B. Ambasana, Thesis Topic: "FPGA Implementation of Environment/Noise Classification Using Neural Networks using Virtualization"
2. Vaibhav Chhaya, Thesis Topic: "CMOS Current-based Mixed-Signal Architecture for Vector-Matrix Multiplication"
3. Sujit Dilipkumar Chavada, Thesis Topic: "FPGA Based Platform for Spiking Neural Networks"
4. Kripal Rupapara, Thesis Topic: "A Study of Power in CR-SRAM in context of Precharge Reference Voltage"
5. Rachit Kacheria, Thesis Topic: "HDL Implementation of Palm Associative Memory"
6. Pavan Vyas, Thesis Topic: "HDL Based Implementation of a Node of Hierarchical Temporal Memory."
7. Renish Dobaria, Thesis Topic: "16-bit Dual Threshold Voltage Conditional Carry Adder."
8. Tejas Dalal, Thesis Topic: "Multi-processor Implementation of MLP and RBF Neural Networks"
9. Jayendra Patel, Thesis Topic: "HDL Implementation of Pearl's Bayesain Belief Propagation Algorithm"
10. Jaydeep Rangani, Thesis Topic: "Using Associative Memories to Reduce Power in Microprocessors"
11. Nilay Mehta, Thesis Topic: "Study of Communication Schemes for Multiple Neural Processing Nodes"

BTP Guided (Completed)

[DAIICT]

1. Aakash Gupta, Project Topic: "Circuit Implementation of Best-Match CAM"
2. Mayank Jain, Project Topic: "Verilog Implementation of Spiking Neural Networks"
3. Akshat Garg, Project Topic: "Verilog Implementation of Self-Organizing Maps for Studying World Economies"

[Ahmedabad University]

4. Dharit Parikh, Project Topic: “Study of Computation Delay and Communication Delay in Nearest-Neighbor-Mesh of (Artificial Neural Network) Processing Nodes” (May 2016)
5. Dev Mehta and Pal Nikola, completed project on "Implementation of Palm Associative Memory onto Multiple FPGA Nexys4 Boards" (May 2017) [URGP Project]

- Extension/aplication of this work was done using Arduino Mega boards, by UGRP students: Dipen Kanjiya and Shivani Shah

6. Bhautik Pipaliya completed project on "Verilog/RTL Implementation of Winner Take All Hashing" (May 2017)
7. Raj Shah completed project on "Custom Communication Scheme for multiple Nexys4 FPGA boards, based on PMOD bus" (May 2018)

[Pandit Deendayal Petroleum University]

8. Mahima Soni completed project on “Implementation of 16-bit Brent Kung adder using DPL pass-transistor logic, based on 16 nm CMOS technology” (May 2020)

BTEP Administrative Mentoring (Completed)

[Ahmedabad University]

9. Harsh Patel (Industry project) (May 2023)
10. Kariravi Shah (Industry project) (May 2023)
11. Smit Shah (Industry project) (May 2023)
12. Nihal Agarwal (Industry project) (May 2023)
13. Dhruv Kabariya (Industry project) (May 2023)
14. Aniket Panchal (Industry project) (May 2024)
15. Pratham Lalwani (Industry project) (May 2024)
16. Ushmay Patel (Industry project) (May 2024)
17. Vatsal Barai (Industry project) (May 2024)
18. Yagnesh Patel (Industry project) (May 2024)
19. Milee Chandramauli Bajpai (May 2025)
20. Mihir Kotecha (May 2025)
21. Krutarth Sunil Vora (May 2025)
22. Deeprajsinh Digvijaysinh Gohil (May 2025)
23. Harsh Manojkumar Pandya (May 2025)

BTEP Technical Mentoring (Completed)

[Ahmedabad University]

24. Yashvi Navadiya completed project on “Road marking detection on UAV videos” (May 2023)

BTech UG Thesis (Completed)

[Ahmedabad University]

25. Utsav Vithlani “Verilog-RTL Implementation of Spatial-Pooler Components of Hierarchical Temporal Memory” (May 2024)
26. (Involved as Co-Evaluator) Preksha SunilMorbia “ Improving Offline TrackingAccuracy by Merging Broken Tracksin Traffic Surveillance” (May 2025)

Bachelor’s Level Capstone Projects (Completed)

[Ahmedabad University]

27. (Involved as Co-Evaluator) Title: Deep learning for stock price forecasting: potential and best techniques: Students: JainiRonak Chalishazar, Jaini Ronak Chalishazar, Dhruv Anant Tanna, Harsh Mukesh Bhalani, Hitanshu Deepak Mehta, Suthar Daksh Vijaykumar (May 2024) (Jointly with Prof. Jayendra Bhalodiya)
28. (Involved as Co-Evaluator) Title: Taxation on Individuals Based on DataUsage (Students: Shlok Nanjwani RhydhamShah Richa Vakharia Prakhya Shah AnmoulDesai Vrinda Chachan Abhiram Srikanth) (May 2025) (Jointly with Prof. Jinraj Joshipura)

Research Grants

Ongoing Utilization:

Name of the Project	Building Context-Specific Image/Video Repository for Indian Roads
Name(s) of faculty	PI: Mazad Zaveri, SEAS
	URB Code: URBSEASI21A3 Ahmedabad University: Seed Grant (November 2021 to November 2023) 2024, 2025: Ongoing use of the equipment (drone) for data collection and datasets are being analyzed with CV-ML techniques and professional data processing sites (https://datafromsky.com/)
Abstract:	• A novel comprehensive repository (of annotated images/videos) for Indian Roads, from the context of traffic-MVDR violations (surveillance and road safety) • This repository will be very suitable, so that computer vision and ML techniques can be easily leveraged to solve the sub-problems in the domain of traffic surveillance and road safety.
Publications under this project:	• Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "Vision-based Investigation of Road Traffic and Violations at Urban Roundabout in India using UAV Video: A Case Study", Transportation Engineering **(Elsevier)**, October 2023, DOI: https://doi.org/10.1016/j.treng.2023.100207 • Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "Evaluating defensive driving behaviour based on safe distance between vehicles: A case study using computer vision on UAV videos at urban roundabout", Multimodal Transportation, **(Elsevier), vol.** 4 (3), pp. 1-22, December 2024, DOI: https://doi.org/10.1016/j.multra.2025.100227 • Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, "U-UTM: A Cyber-Physical System for Road Traffic Monitoring Using UAVs," 18th IEEE InternationalConference on Vehicular Electronics and Safety (ICVES), Ahmedabad, India, December 2024, DOI: https://doi.org/10.1109/ICVES61986.2024.10927911 • Yagnik M Bhavsar, Mazad S Zaveri, Mehul S Raval, Shaheriar B Zaveri, (Poster) "Traffic investigation at roundabout using UAV", 18th IEEE InternationalConference on Vehicular Electronics and Safety (ICVES), Ahmedabad, India, December 2024.

Completed:

Name of the Project	Building a (programmable) hardware acceleration platform based on multiple boards (FPGA or Arduino boards), for emulating neural networks/algorithms (Initial case study: Palm Associative Memory)
Name(s) of faculty	PI: Mazad Zaveri, SEAS Co-PI: Anurag Lakhlani, SEAS
Sponsor(s)	Ahmedabad University AU/SG/SEAS/2016-17/05 Category: Seed Grant Duration: 2 years (Nov. 2016 – Nov. 2018) Rs. 1.6 lacs Involvement: Supervisor; Hardware resources were used for many BTP projects

Name of the Project	Development of Ultra Low Power and Low Voltage Time to Digital Converter (TDC) for Space Applications
Name(s) of faculty	PI: Biswajit Mishra, PhD, Professor, DAIICT, Gandhinagar Co-PI: Mazad Zaveri, SEAS
Sponsor(s)	Indian Space Research Organization, Dept. of Space, Govt. of India Category: ISRO RESPOND program ISRO-RES-3-717-2016-17 Duration: 2 years (Dec. 2016 – Nov. 2018) Rs. 11.4 lacs

Name of the Project	Processor RTL customization and development of Low Power Design Flow methodology
Name(s) of faculty	PI: Amit Bhatt, PhD, Associate Professor, DAIICT, Gandhinagar

	Co-PI: Mazad Zaveri, SEAS
Sponsor(s)	Gujarat Council on Science and Technology, DST, Govt. of Gujarat Category: Minor project GUJCOST/MRP/15-16/1079 Duration: 2 years (Sept. 2015 – August 2017) Rs. 2.5 lacs

Name of the Project	FPGA Hardware Implementation of Bio-inspired Computational Models
Name(s) of faculty	PI: Mazad Zaveri
Sponsor(s)	Dhirubhai Ambani Institute of Information and Communication Technology Category: Seed money Duration: 2011 – Nov. 2014 Rs. 50,000 Involvement: Supervisor; Hardware resources were used for MTech students Theses

ACADEMIC-ADMINISTRATION WORK EXPERIENCE

(Administrative/Academic Duties)

- **Current (at SEAS, Ahmedabad University):** December 2020 onwards
  - Member, SEAS Faculty Search Committee (July 2023 onwards)
  - Member, AU Student Grievance Committee (July 2023 onwards)
  - Member, (School Representative) AC Sub-Committee on Courses and Curriculum (Upto March 2024)
  - Member, (and Course Code Coordinator) School-level Academic Committee
  - Co-Chair, Intelligent Transportation Systems - Research Cluster (Upto Jan. 2023)
  - Member, BTP Evaluation Committee, (May 2022, May 2023, May 2024, May 2025)
  - Member, PhD Written Test and Interview Admissions Committee (Dec. 2020, June 2021, Dec.2022, May 2023, Nov. 2023, Nov. 2024, April 2025)
  - Member, MTech Written Test Committee (Jan. 2024)
  - Convener, PhD Written Test and Interview Admissions Committee (April 2024)
  - Member, CE sub-area: BTech CSE Curriculum Revision Committee (2024)
  - Convener, Curriculum Development Committee, New programme MTech in VLSI Design (June 2023 onwards)
  - Chair, MTech Microelectronics and Semiconductors programme (from Feb. 2025)
  - Nominated as the Nodal Officer (January 2025 onwards), for the GoI Visvesvaraya PhD Scheme for Electronics and IT
- **Previous (at Pandit Deendayal Petroleum University)** (2018-2020)
  - Convener, ICT Dept. - Curriculum committee
  - Member, ICT Dept. - Infrastructure committee
  - Faculty in-charge for development and procurement of *Embedded System & VLSI* Laboratory
  - Member and moderator, - ICT Dept. Faculty and staff search committee
  - Member, ICT Dept. - Industrial Internship and Comprehensive Project evaluation committee
  - Member, ICT Dept. - Admissions counselor (Summer 2019)
  - In-charge HoD, ICT Dept. (July – August 2020)
- **Previous (at SEAS, Ahmedabad University):** (2014-2018)
  - **Chair, PhD Program - SEAS:** Managing various academic-administrative tasks related to the PhD program; and PhD admissions process for Winter 2017-18, Monsoon 2017-18, Winter 2017-18, Monsoon 2018-19
  - Member, School Academic Committee
  - Member, School Level Examination Committee
  - Member, AU Examination Committee

- Member, Working Group of UG Dean; Convener, Sub-committee for Course feedback form
- Member, Committee for BTP evaluation (2018)
- Member, B.Tech. ICT Curriculum Revision Committee (2017)
- Convener - Group IV, Committee for BTP evaluation (2016, 2017)
- **UG Programs Coordinator, Member of Academic Committee and Convener of Grade Sub-Committee (at IET/SEAS)**: Managing various academic-administrative tasks such as: course registrations; coordination of exams; recording-keeping of grades and generation of marksheets and transcripts; record-keeping of program structure, course curricula and syllabus; drafting academic policies and guidelines, creating resource and capacity planning sheets, etc.

- **Previous (at DA-IICT):** (2010 - 2014)
  - **PhD Program Coordinator (at DA-IICT)**: Coordinating various exams/seminars related to the PhD program; Implementation of academic rules & requirements related to the PhD program; Suggesting and creating policies/processes for streamlining the PhD program; Record-keeping of PhD student information.
  - **Member of the Post-Graduate Academic Committee (at DA-IICT)**: Discussing and resolving issues with post-graduate programs; Implementation of academic rules & requirements related to the post-graduate programs.
  - **Member of PhD Admissions Committee (at DA-IICT)**: Coordinating and planning PhD online applications, entrance test and interview process.

PROFESSIONAL WORK – (As subject expert)

(Reviewing of Journal and Conference papers)

- IEEE Transactions on Nanotechnology
- IEEE Transactions of Neural Networks
- IEEE Access (2019, 2021)
- Arabian Journal for Science and Engineering (Springer)
- Member of Executive Committee, Network of Engineering Institutions (2011, 2012)
- International Conference on Advances in Electronics, Computers and Communications, Bangalore (2014)
- International Symposium on VLSI Design and Test, Ahmedabad (2015)
- International Conference on Advances in Computing, Communications and Informatics, Jaipur (2016)
- International Conference on Advances in Computing, Communications and Informatics, Manipal (2017)
- International Conference on Smart Systems, Innovations and Computing, Jaipur (2017)
- International Conference on Soft Computing and its Engineering Applications, CHARUSAT (2017)
- International Conference on Advances in Computing, Communications and Informatics, Bangalore (2018)
- International Conf. on Advances in Computing, Communication and Control, Mumbai (2011, 2013, 2015, 2017, 2019, 2020, Dec. 2021)
- IEEE India Council International Conference - INDICON19 (2019)
- Third International Conference on Advanced Computational and Communication Paradigms (ICACCP), Sikkim, (March 2021)
- Computers and Electrical Engineering, Elsevier (January 2022)
- IEEE Access (2022, Dec.2024)
- Electronics Journal (June 2023)
- Integration- The VLSI Journal (Oct. 2023, Oct. 2024
- ICCINS-2023 (Aug. 2023)
- IEEE Transactions on Circuits and Systems I (Oct. 2023, Jan. 2025)
- Journal of Supercomputing (June 2023)
- 18th IEEE International Conference on Vehicular Electronics andSafety (ICVES), Ahmedabad, Dec. 2024
- 3rd International Conference on Modelling, Simulation & Intelligent Computing, Oct. 2024
- IEEE 2nd International Conference on Artificial Intelligence andMachine Vision, Feb. 2025

- International Journal of Electronics Letters, April 2025

(Workshop Organizer)

- Administrative Organizer, Network of Engineering Institutions' 1st Workshop on "Analog CMOS Circuits", June 2012.
- Member, Organizing Committee (In-charge: Website and registration), for the conference "Foundations of Software Technology and Theoretical Computer Science (FSTTCS)", to be organized by, and held at SEAS, Ahmedabad University, during December 10-15, 2018.
- Organizing Committee member, for Workshop on "Developing Emerging Nuclear Security Practitioners", during November 2019.
- Nominated as Organizing Chair, for the 18th IEEE International Conference on Vehicular Electronics and Safety, December 2024.

(Invited Talks / Invited Instructor / Invited as Session-Chair)

- Delivered four-hours of lecture on "Digital Logic Design using Verilog" at The LNM Institute of Information Technology (LNMIIT), Jaipur, April 2012
- Invited as session-chair for the group presentations on: reconfigurable and digital designs, at the International Symposium on VLSI Design and Test (VDAT), Ahmedabad, June 2015
- Invited speaker/organizer, for student Workshop on Logisim, February 2019, under CSI banner.
- Invited speaker (topic: Systems Approach) at the Faculty Induction Program PDPU, July 2019.
- Invited co-instructor, for student Workshop on AVR based Robot programming, under eYantra Lab – nodal center at PDPU, August 2019.
- Faculty mentor for (PDPU Team ID 1295243) DST and Texas Instruments in India Innovation Challenge Design Contest 2019 anchored by NSRCEL@IIMB powered by AICTE mission and supported by MyGov: August 2019.
- Invited as mentor by PDPU IIC, for the first CS/ICT Hackathon, September 2019.
- Invited as Session Chair, in the Symposium on VLSI Design and Embedded System, part of CoCoNet19, IIITM-K (December 2019).
- Invited speaker/organizer, for student Workshop on Digital Design and Simulation using Logisim, under IEEE Student Chapter: February 2020 (57 participants).
- Invited speaker for student workshop on "Moore Finite State Machine Design using Logisim". under IEEE Student Branch, Ahmedabad; 24-November 2021.
- Invited moderator on ERTE panel discussion on "How to bring intelligence into the India Transportation System?". IEEE Emerging Research Topics in Engineering (ERTE) workshop, Ahmedabad ; September 25, 2022.
- (October 2023).Tutorial talk title: Safety Measures in two-wheeler mobility in Developing Countries. 11th IEEE Asia Pacific Region (R10) Humanitarian Technology Conference, 11th IEEER10 Humanitarian Technology Conference, Marwadi University, Rajkot; October 16-18.
- (December 2023).Invited talk title: Next Gen. Technologies for Investigating Road Traffic and Rule Violations at Roundabout. Indian Institute of Information Technology (IIIT) Sri City, SriCity, AP; December 07-09.
- (May 2025) Webinar: Digital CMOS VLSI: Circuits and Sub-systems, Ahmedabad University

(Invited as External Thesis Examiner)

- Master's Thesis evaluation at the Centre for Environmental Planning and Technology University, Ahmedabad (2013)
    - Master's Thesis Topic: Modelling consideration sets and brand choice using artificial neural networks
- PhD Dissertation review at Gujarat Technological University (2014)

- DA-IICT, Gandhinagar (2015, 2016)
  - RPS on Thesis Topic: Ultra Low Power Capacitive Management Unit in 0.18 um CMOS (by student: Sanjay Kasodniya, ISRO)
- ME Thesis review at VGEC, Gandhinagar, Gujarat Technological University (June 2018)
- Invitation as external expert - committee member for evaluating MTech (CSE) theses in VLSI domain, at IIT Vadodara, January 2022
- PhD Dissertation Committee member (as External Subject Expert) (September 2018, Dec 2018, June 2019, Dec 2019, June 2020, Dec 2020, June 2021, July 2022)
  - Student: Mr. Kirit Patel, (faculty at LD Engineering College, Ahmedabad)
    - Supevisor: Prof. Mihir Shah, (Head, Electronics/VLSI Dept., LD Engineering College, Ahmedabad)
- Invited as external expert to judge the BTech Final Year Projects at SEAS, Ahmedabad University, May 2019.
- PhD Dissertation Committee member (as External Subject Expert) (July 2019, Dec. 2019, June 2020, Dec 2020, June 2021, March 2022, July 2023)
  - Student: Mr. Punit Lathiya, (faculty at Govt. Engg. College, Rajkot)
    - Supevisor: Prof. Rajesh Thakker, (Principal, Govt. Engg. College, Rajkot)
- Member, Dissertation Advisory Committee for PhD student: Dipali Pattnayak (2023)
- Member, Dissertation Advisory Committee for PhD student: Prajakta Rathod (2023, 2024, 2025)

(External International Linkages)

- Initiated and jointly implemented: PBL pedagogy based course projects done by 8 student pairs from Sacred Heart University and PDPU (Oct. – Dec. 2019)
  - A paper publication related to this pedagogical experiment, was published in IEEE TALE 2020.
- (As an alumnus of ASU) Interactions with Arizona State University team, that eventually led to Summer Internship program for PDPU students at ASU. (2019)
- (As an alumnus of ASU) Interactions with Arizona State University Admissions team (April 2025)

SEMINAR/WORKSHOP/LECTURES/DISCUSSIONS/CONCLAVE/FDP ATTENDED

1. "Architectures for Silicon Nano-Electronics and Beyond: A Workshop to Chart Research Directions", sponsored by National Science Foundation (NSF), (Portland, OR), Sept. 2005.
2. "A NeuroSilicon Workshop", Sponsored by Office of Naval Research (ONR), (Portland, OR), Aug. 2006. Old URL: http://web.cecs.pdx.edu/~strom/onr_workshop/onr_workshop.html
3. "Technology Maturity for Adaptive Massively Parallel Computing: A Workshop to Chart Architectural Readiness of Real-World Applications", jointly sponsored and organized by Intel Corp., ONR, NSF, PSU (Portland, OR), Mar. 2009. URL: http://www.technologydashboard.com/adaptivecomputing/
4. Panel Discussion - "Traffic Discipline and Citizens Dialogue", organized and sponsored by the Ahmedabad Traffic Consultative Committee (ATCC), Ahmedabad, 3rd May 2014.
5. Summit on "National Traffic Technology", as part of program Vibrant Gujarat-2015, organized by Home Department, Govt. of Gujarat, at YMCA, Ahmedabad, 2nd January 2015.
6. Workshop on "Project based learning", conducted by Prof. Lynn Stein (from Olin College of Engineering), organized by Ahmedabad University, 10th October 2015.
7. FDP on "Technological trends and 21st century Digital learning", organized by Tata Consultancy Services, at Garima Park, Gandhinagar, 23rd-24th May 2016.
8. Conclave on "Transforming Higher Education Through: Quality, Governance, and Innovation", conducted as part of the program International Conclave on Higher Education, pre-Vibrant Gujarat -2017, organized by Education Department, Govt. of Gujarat, at Mahatma Mandir, Gandhinagar, 18th October 2016.
9. Conclave on "Smart Villages & Cities", organized by the Confederation of Indian Industry, Ahmedabad, 17th December, 2016.
10. FDP on "Advance VLSI and Electronic System Design", organized and sponsored by eInfoChips, Ahmedabad, 12th-16th June, 2017.
11. Conclave on "Vision and Explorations for Planetary Sciences in Decades 2020-60", organized by Physical Research Laboratory (Dept. of Space, Gov. of India), 8th-12th November, 2017.
12. Some sessions during the conference - Foundations of Software Technology and Theoretical Computer Science (FSTTCS), Ahmedabad University, December 10-15, 2018.
13. Sessions related to the "Trends and future of Networking", in Third International Conference on Computing and Network Communications (CoCoNet'19), IIITM-K Trivandrum, Kerala, December 18-21, 2019.
14. Webinar on "Semi-Custom Design flow Using Mentor Graphics EDA tools", 17-April-2020.
15. Webinar on "Exploring Tensorflow for Deep Learning", 17-April-2020.
16. Webinar on "VLSI based System Design Using FPGA/SoC", 17-May-2020.
17. Webinar on "Digital Transformation through Data Science and Cyber Security", 3-June-2020.
18. Webinar sessions on "Introduction to Big Data", " Introduction to Data Analytics", "Amazon Cloud Essentials", "Machine Learning Basics", organized by Amazon AWS, May 2021
19. Conference on "Ahmedabad Leading Dialogues", 14-15 may 2021, organized by Ahmedabad University.
20. Five-day FDP on "VLSI SYSTEMS - A DESIGNER'S POINT OF VIEW', organized by the Department of Electronics and Communication, Dharmsinh Desai University, Nadiad, Gujarat. (June/July 2021)
21. Workshop on IP Law, requirement and strategies for filing, conducted at Ahmedabad University (July 2021)
22. Training Program (20 hours) on "Design and Verification using Verilog - DV18", by Entuple Technologies Ltd. (May 2022)
23. Attended online technology sessions at the MATLAB EXPO 2023, May 10–11, 2023. (URL: https://www.matlabexpo.com/online/2023/proceedings.html)
24. Attended the IEEE ITSS Winter School on "Computing and IoT Technologies for Mobility in 2-Wheelers and Electric 2-Wheelers", at Indian Institute of Information Technology (IIIT) Sri City, during 7- 9 December 2023.
25. Attended the conference: 11th IEEE Asia-Pacific Region 10 (R10) Humanitarian Technology Conference, Marwadi University, Rajkot, 16-18 October 2023.

26. Attended (and was also one of the organizers for) the IEEE ITS Society Chapter Inaugural Event Workshop, at DA-IICT, Gandhinagar, on the Theme: Innovation in Motion -Shaping the Future of Transportation in Developing Countries, 16 March 2024.
27. Attended the sessions under IEEE Activity on "Semiconductors/VLSI: Foundation, Growth, and Challenges", Organized by: Joint Chapter of EDS and SSCS Gujarat Section & IEEE Education Activity(Gujarat Section) at DAIICT, on 27-Feb-2025; Speakers: Prof. Yash Agarwal and Mr. Nilesh Ranpura (industry expert)
28. Attended sessions at the conference: ISPEC2025 Indian Semiconductor and Packaging Ecosystem Conference (under Gujarat Semiconnect), 7 March 2025.

Scholarships

- 1st rank among all engineering branches and colleges (of Gujarat University) in the first year of B.E. degree program
- 1st rank in (IC Engg. branch) during four consecutive years of B.E. degree program, and four gold-medals for the same
- Arizona Board of Regents' Graduate Tuition-Scholarship during M.S.E degree program
- Research assistantships (including stipend and tuition-fees) for five years, supported in part by grants from U.S. National Science Foundation (NSF), U.S. Defense Advanced Research Projects Agency (DARPA), SyNAPSE program subcontract to HRL Laboratories (formerly Hughes Research Laboratories - USA), and Air Force Research Laboratory – USA (2005 – 2009)

RECOGNITION – As subject Expert

- Best paper award in Session 1-2: Nilay Mehta, Mazad Zaveri, "Investigation of Communication Schemes for ANN Implementation - Multiple Processing nodes (Based on FPGA/u-controller Boards)" in (ISTE, UGC merged scheme funded) *International Conference on Advances in Computing, Communication, and Informatics*, held on 25-Feb-2017, at the Dept. of CSE, Maharaja Sayajirao University.
- Invited as an expert for reviewing proposals/projects in the area of grassroots innovation, at the National Innovation Foundation-India, (an autonomous body of the DST, Govt. of India), January 2017 and July 2017.
- Invited and appointed by Gujarat Technological University (GTU) as subject expert on two Doctoral Program Committees, in the area of VLSI (from 2017 onwards).
- Invited as *Track Chair* for "Circuit Systems and Devices" track-12, of the IEEE 16th India Council International Conference - INDICON19 (May to September 2019).
- Invited as subject expert for review/appraisal of the progress of contractual staff (engineering team), at the National Innovation Foundation- India (NIF), DST, Govt. of India: May 2019.
- Interview (conversations as ITS Cluster Co-chair) featured in the newsletter- Research Horizons, published by Ahmedabad University (January 2022)
- Invited as subject expert (and DAC member) for the final open seminar (PhD) for Mr. Kirit Patel (July 2022)
- Invited expert (DPC member) at the PhD final viva-voce of Prof. Kirit Patel (LD College of Engineering) (July 2023)
- Invited as the Chair for the final PhD Defense of Mr. Sagar Kavaiya, Ahmedabad University (Oct. 2022).
- Our research on ITS was covered in the Newspaper - Times of India, Times City (Ahmedabad edition), Date:23-October-2023. Article title: "23% of vehicles squarely violate traffic rules at roundabouts:Study" Link: https://timesofindia.indiatimes.com/city/ahmedabad/23-of-vehicles-squarely-violate-traffic-rules-at-roundabouts-study/articleshow/104638011.cms
- Nominated by the IEEE ITSS as one of the experts to conduct tutorial at the 11th IEEE Asia-PacificRegion 10 (R10) Humanitarian Technology Conference, Rajkot, October 2023.
- Invited as the Vice Chair (Technical Activity) under the Executive Committee of the Gujarat Chapter, of the IEEE Intelligent Transportation Systems Society, for Year 2024.

- Invited as one of the expert panelists on the topic: Vehicle electronics and drive safety - ICT in 2-wheelers and different perspectives, at the IEEE ITSS Winter School, at Indian Institute of InformationTechnology (IIIT) Sri City, on 9 December 2023.
- 1st Position in Poster Presentation in Track3: Electronics and Communication, at IEEE SPS GS and IEEE PDEU SPSSB IGNITE Event, March 2024.
- Nominated as Organizing Chair, for the 18th IEEE International Conference on Vehicular Electronics and Safety, December 2024.
- Nominated as the Nodal Officer (January 2025 onwards) of the university, for the GoI Visvesvaraya PhD Scheme for Electronics and IT

SOCIAL CONTRIBUTION / COMMUNITY SERVICE / WORKING for SOCIETAL BENEFIT

- Invited by ASU Alumni Liaison, to help and interact with prospective applicants of Arizona State University (ASU), Ahmedabad, September 2019.
- Invited to USA University Alumni Fair, to help and guide prospective students and their parents, applying to US universities, organized by Indo-American Education Society (which is supported by and part of the US Department of State), Ahmedabad, November 2019.
- Working towards road traffic safety and road accident prevention
    a. Vice Chair (Technical Activity) under the Executive Committee of the Gujarat Chapter, ofthe IEEE Intelligent Transportation Systems Society, for year 2024;
    b. Our research on ITS was covered in the Newspaper - Times of India, Times City (Ahmedabad edition), Date: 23-October-2023. Article title: “23% of vehicles squarely violate traffic rules at roundabouts:Study”
    Link: https://timesofindia.indiatimes.com/city/ahmedabad/23-of-vehicles-squarely-violate-traffic-rules-at-roundabouts-study/articleshow/104638011.cms
    c. Youtube link to our video: https://www.youtube.com/watch?v=3NYZnBAcPuY
    d. Link to our work on defensive driving and road safety covered in university news: https://ahduni.edu.in/academics/schools-centres/school-of-engineering-and-applied-science/news/rethinking-defensive-driving-in-indian-cities/