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ECE 325
Individual Project 1

Abstract:

The purpose of this project was to design an interconnect consisting of a single trace route across three FR4 layers characterized for a quasi-PCI Express 7.0 serial data link. The PCIe 7.0 signal is routed through the trace and analyzed under realistic conditions from the SIE standpoint in this report. A combination of on-chip trace (OCT), on-chip bonding pad (OCP), and a gold bond wire connected to the opposing PCB Bonding pad are used to route the signal out of the chip. All traces are copper.

To better optimize the interconnect design I chose to make all of the traces similarly sized and streamlined with a consistent width of 20 mil. I made my two required 90 degree turns as small in length as possible so that the traces were as close to one straight line as possible as they pass through the interconnect. Each separation was similar in size and length in hopes of decreasing the reflections and jitter during the simulation and analysis.

It was found that the resultant eye diagrams for the given start pulse width of 50 ps caused too much jitter and could not form a proper eye diagram at the UI of 62.5 ps. With more testing it became clear that the simulation had a better result for a pulse width of 400 ps which gives a UI of 412.5 ps. The jitter values for 1000 and 10000 bit sequences stayed below 25ps and 30ps respectively and passed all compliance testing.

PCIe 7.0 Overview:

The PCIe 7.0 is an upgrade of PCIe which is a high speed serial data interconnect framework used for things such as graphics communications. The PCIe bus consists of 16 lanes, where each lane contains two different signal pairs for a total of four signal traces per lane for transmitting and receiving. The scenario of this project focuses on signal propagation through one of the halves of the signal pairs, so ¼ of a lane or 1/64 of the full PCIe bus. The data transfer speed of the PCIe 7.0 is 16 GB/sec, yielding a single unit interval of 62.5 ps.

Problem Overview:

The task was to route a test trace carrying the PCIe 7.0 signal and analyze it under realistic conditions. To better optimize the interconnect design I chose to make all of the traces similarly sized and streamlined between 500 mil and 700 mil in length with a consistent width of 20 mil. I made my two required 90 degree turns as small in length as possible so that the traces were as close to one straight line as possible as they pass through the interconnect. Each separation was similar in size and length in hopes of decreasing the reflections and jitter during the simulation and analysis. It was found that the resultant eye diagrams for the given start pulse width of 50 ps caused too much jitter and could not form a proper eye diagram at the UI of 62.5 ps. With more testing it became clear that the simulation had a better result for a pulse width of

400 ps which gives a UI of 412.5 ps. The jitter values for 1000 and 10000 bit sequences stayed below 25ps and 30ps respectively and passed all compliance testing.

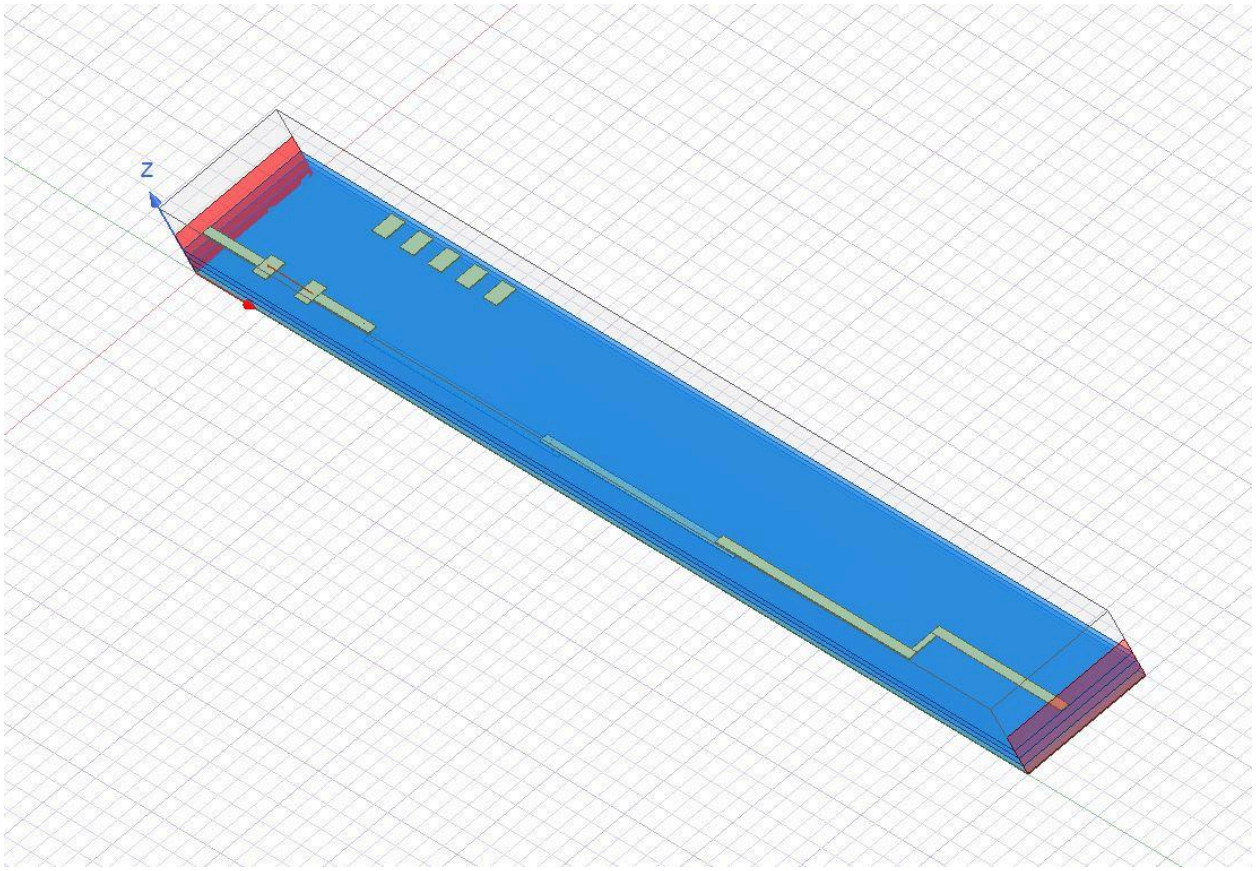
Solution Outline:

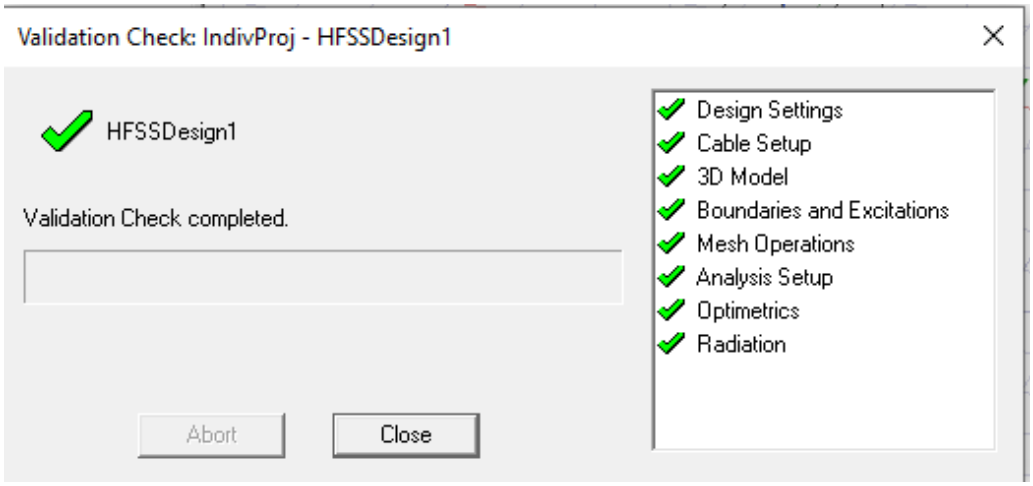
a. HFSS Model Creation

To streamline this design and optimize it I attempted to make all of the trace portions similar sizes in length and the exact same width. Each trace section was between 500 mil and 700 mil in length and they are all 20 mil in width. The two required 90 degree turns were made as small as possible in attempts to not create too many reflections from nearby traces. The goal was to make all of the connections one big long trace with as little deviation as possible.

b. HFSS Model

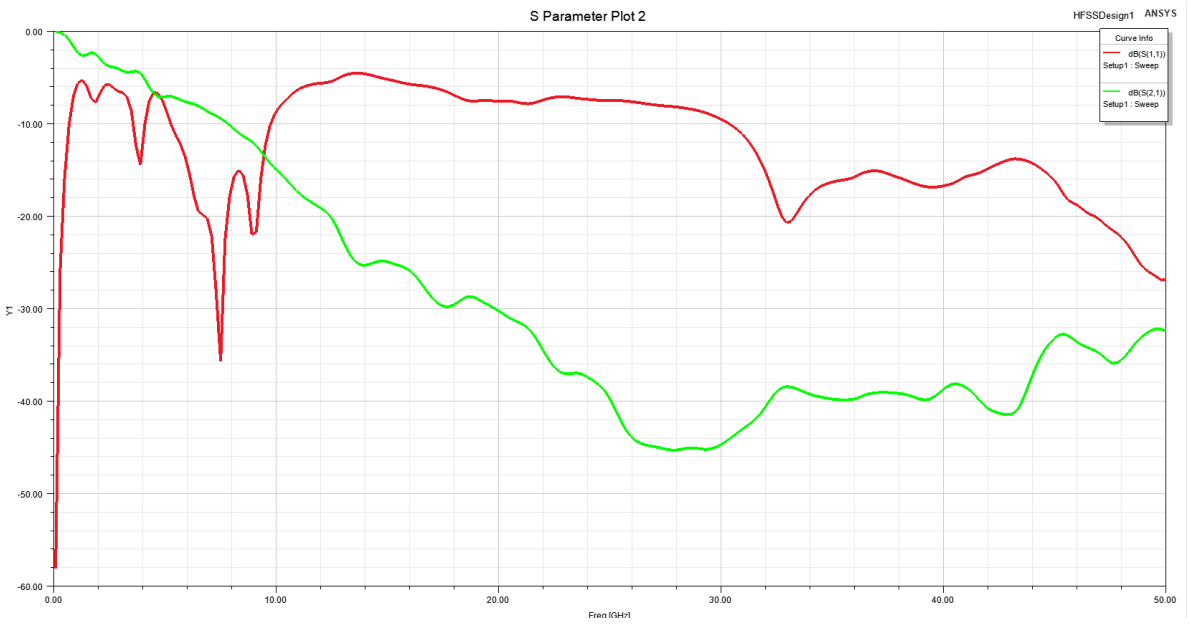
These images show my complete interconnect and the proper validation check of the design. It combines the use of on-chip trace (OCT), on-chip bonding pad (OCP), and a gold bond wire connected to the opposing PCB Bonding pad to route the signal out of the chip. All traces are copper and the blue dielectric is FR4.





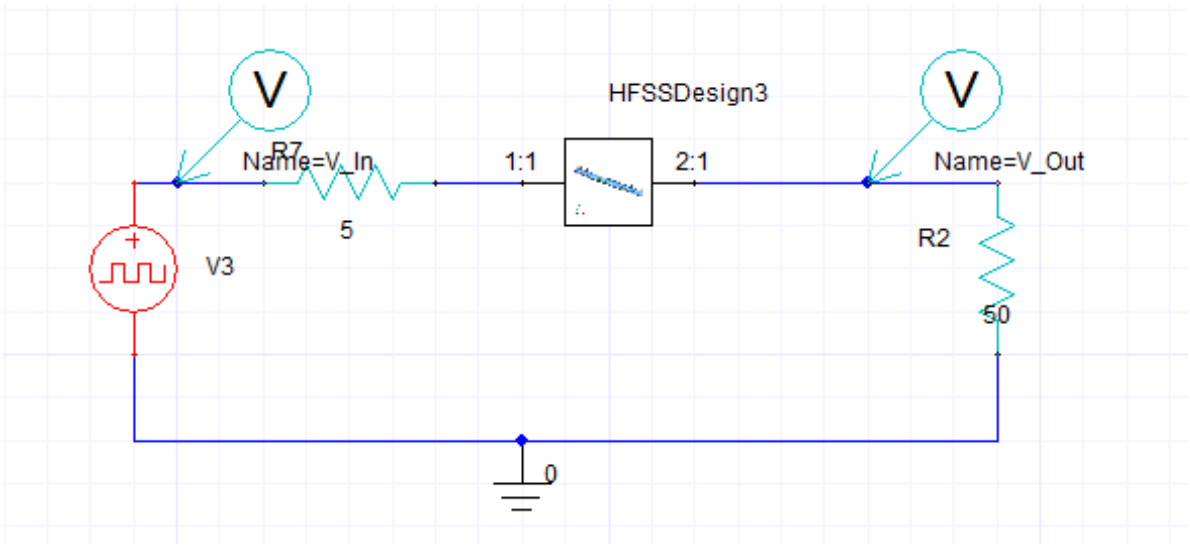

c. HFSS results

These S21 and S11 graph results are correct and represent a properly built and simulated design because S21 starts at 0 dB on the graph. The optimal frequency would be below ~1 GHz because that is where the S(1,1) aligns with the value of -10. S(2,1) crosses -6 at ~4 GHz and continues to decrease after so the optimal range for S(2,1) would be <4 GHz. Another point where the frequency could work is between ~5 and ~10 GHz where S(1,1) once again passes the benchmark of -10. I believe that below ~1 GHz would still be the optimal frequency for S(1,1) because there would be less distortion.



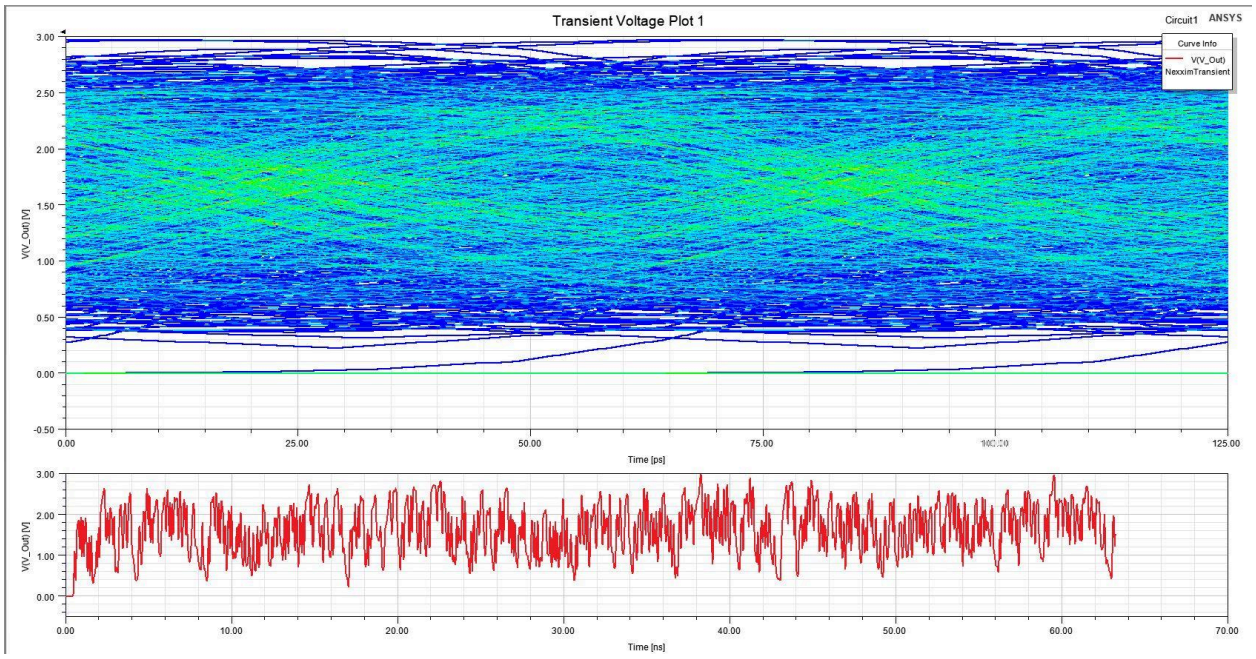

d. Circuit Model

The image below shows the complete circuit model that includes a V_PRBS, a 5 ohm resistor, a 50 Ohm resistor, and the HFSS Design.

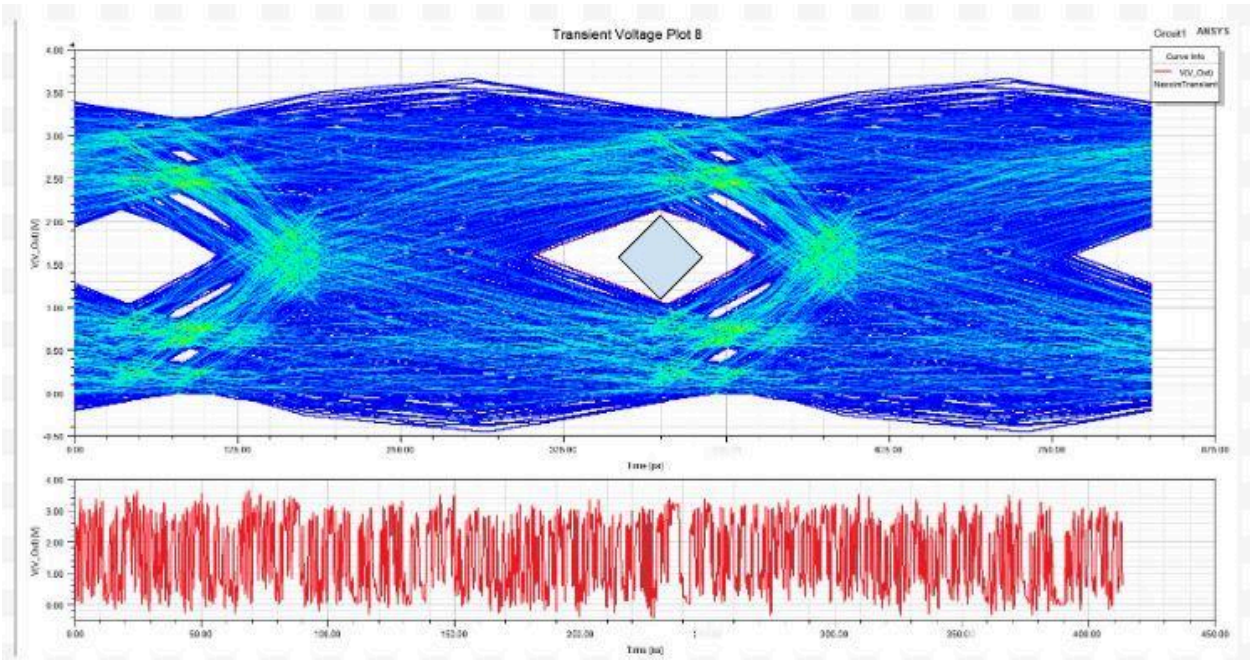



e. Circuit Simulation results

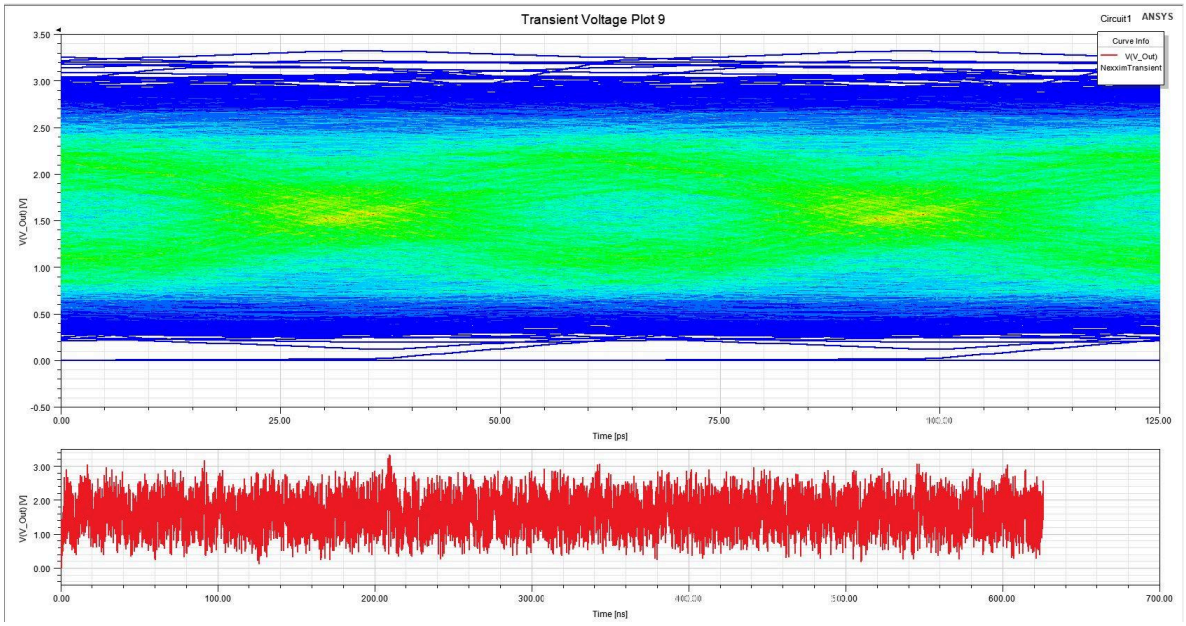
Below is the first image using 50 ps PW for a 1000 bit spec. It is clear from this simulation that this eye diagram is not clear and there is no sense in spec compliance testing or jitter testing. It appears that there is no start or end to the jitter in this simulation. In this case the UI was 62.5 ps and the PW was 50 ps for the 1000 bit spec.




Below is the second image using 4000 ps PW. It is clear from this simulation that this eye diagram is more obvious and passes the spec compliance test but not the jitter test. The jitter was exceeding 25ps during compliance testing which was followed here. In this case the UI was 412.5 ps and the PW was 4000 ps for the 1000 bit spec.

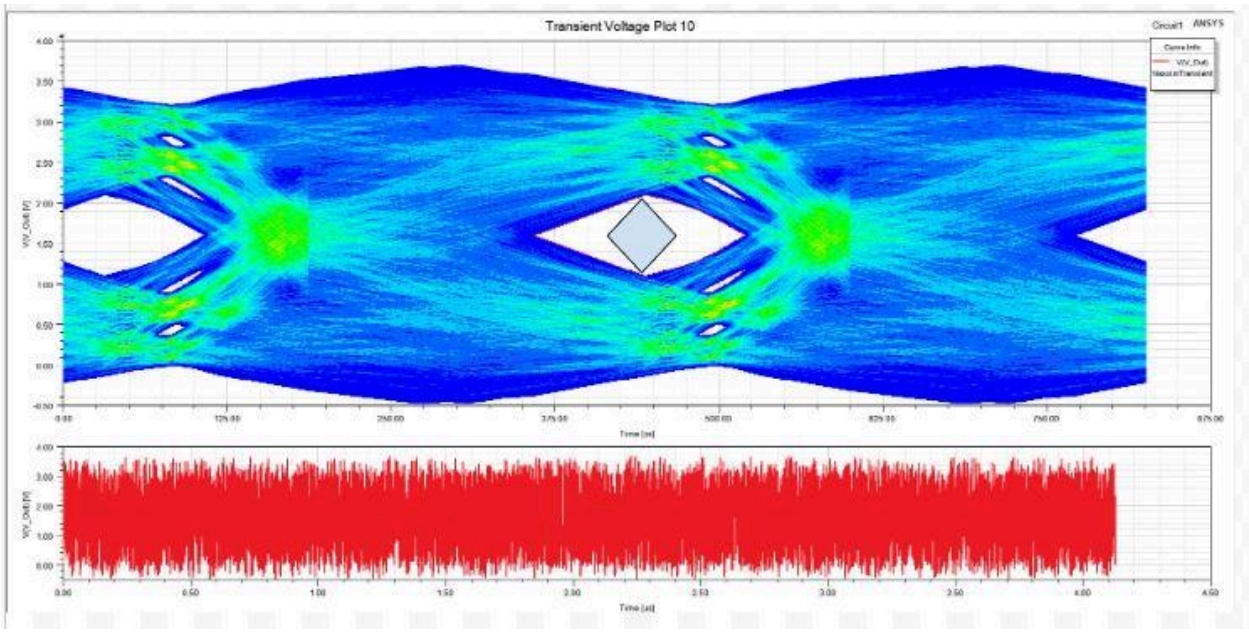



Below is the third image using 50 ps PW for the 10000 bit spec. It is clear from this simulation that this eye diagram is not clear and there is no sense in spec compliance testing or jitter testing. It appears that there is no start or end to the jitter in this simulation. In this case the UI was once again 62.5 ps and the PW was 50 ps for the 10000 bit spec.




Below is the fourth image using 400 ps PW for the 10000 bit spec. It is clear from this simulation that this eye diagram follows spec compliance testing and the jitter test. The jitter was exceeding

30ps during compliance testing which is followed here. In this case the UI was once again 412.5 ps and the PW was 4000 ps for the 10000 bit spec.




Summary:

In this project an interconnect was built with a single trace route to carry a PCIe 7.0 signal in order to analyze it under realistic conditions. This was achieved with an interconnect containing on-chip trace (OCT), on-chip bonding pad (OCP), and a gold bond wire connected to the opposing PCB Bonding pad to route the signal out of the chip. All traces are copper and the blue dielectric is FR4. The simulation of this interconnect and its circuit yielded observations that a PW of 50 ps is not large enough to pass compliance checks for spec tests and jitters. A PW of 400 ps is needed to better analyze and visually represent the signal and its interactions. Though this interconnect was the third draft that finally became reality, it is the most optimized version created due to its similarly sized trace sections and streamlined architecture even with two 90 degree turns.

Conclusion:

This project was very educational and required demonstration of a lot of laboratory skills used throughout the semester. The project naturally increases familiarity with the software due to its complex nature. After working through many challenges in this intricate project, the final result of a complex interconnect with a single trace route was created and used for successful analysis. A better understanding of signals, 3D design, and model architecture and simulation was gained through this experience.