

# Basics of Flip Flop

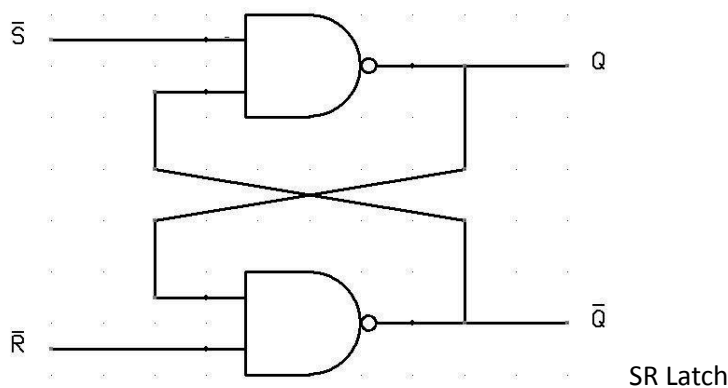
A circuit that has two stable states is treated as a **flip flop**. These stable states are used to store binary data that can be changed by applying varying inputs. The flip flops are the fundamental building blocks of the digital system. Flip flops and latches are examples of data storage elements. In the sequential logical circuit, the flip flop is the basic storage element. The latches and flip flops are the basic storage elements but different in working. There are the following types of flip flops:

## Flip flop v/s Latch

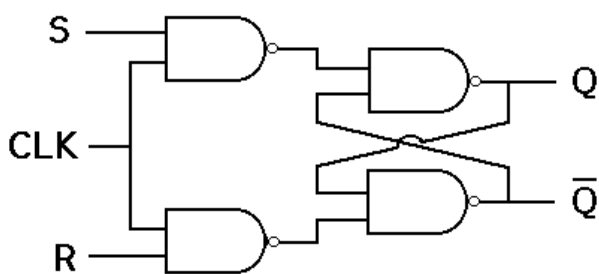
The basic difference between a latch and a flip-flop is a gating or clocking mechanism.

In Simple words. Flip Flop is edge-triggered and a latch is level triggered.

For example, let us talk about SR latch and SR flip-flops. In this circuit when you Set S as active the output Q would be high and Q' will be Low. This is irrespective of anything else. (This is an active-low circuit so active here means low, but for an active high circuit active would mean high)



A flip-flop, on the other hand, is **synchronous** and is also known as a gated or clocked SR latch.



SR Flip-Flop

In this circuit diagram, the output is changed (i.e. the stored data is changed) only when you give an active clock signal. Otherwise, even if the S or R is active the data will not change. Let's look at the types of flip-flops to understand better.

## SR Flip Flop

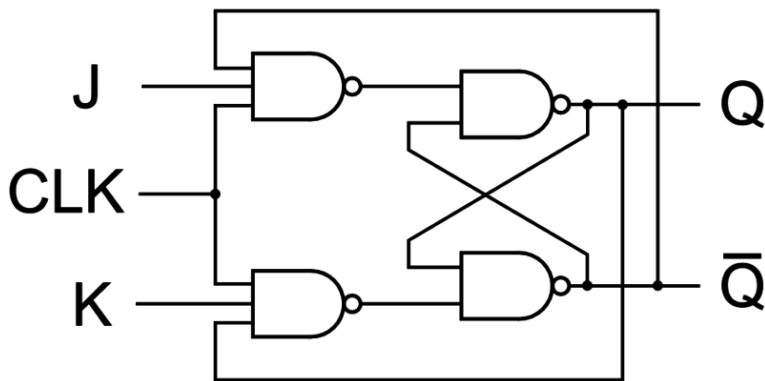
There are many types of flip-flops, with the most common one being SR flip-flop. This simple flip-flop circuit has a set input (S) and a reset input (R). In this system, when you Set "S" as active the output "Q" would be high and "Q'" will

be low. Once the outputs are established, the wiring of the circuit is maintained until “S” or “R” go high, or power is turned off. As shown above, it is the simplest and easiest to understand. The two outputs, as shown above, are the inverse of each other. The truth table of SR Flip-Flop is highlighted below.

S	R	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

## JK Flip-flop

Due to the undefined state in the SR flip-flop, another flip-flop is required in electronics. The JK flip-flop is an improvement on the SR flip-flop where S=R=1 is not a problem.



JK Flip-Flop

The input condition of J=K=1, gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

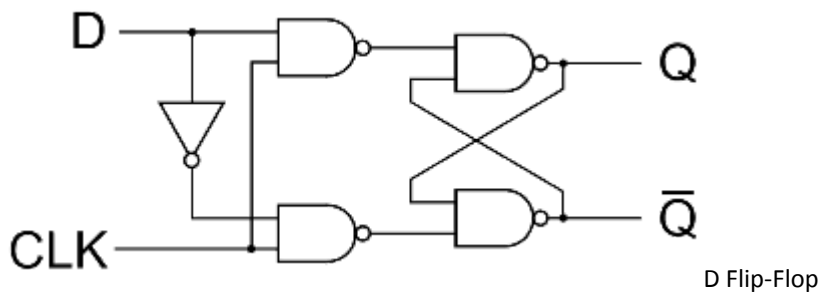
In simple words, If J and K data input are different (i.e. high and low) then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge then the output will toggle from one state to the other. JK Flip-Flops can function as Set or Reset Flip-flops

J	K	Q	Q'
0	0	0	0
0	1	0	0

1	0	0	1
1	1	0	1
0	0	1	1
0	1	1	0
1	0	1	1
1	1	1	0

## D Flip Flop

D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift-registers and input synchronisation.



In this, the output can be only changed at the clock edge, and if the input changes at other times, the output will be unaffected.

Clock	D	Q	Q'
↓ » 0	0	0	1
↑ » 1	0	0	1
↓ » 0	1	0	1
↑ » 1	1	1	0

The change of state of the output is dependent on the rising edge of the clock. The output (Q) is same as the input and can only change at the rising edge of the clock.