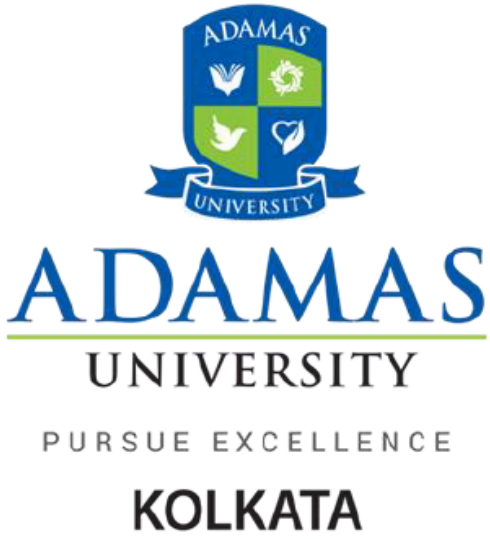

ADAMAS UNIVERSITY

SCHOOL OF ENGINEERING & TECHNOLOGY

Department of Computer Science and Engineering

B.Tech in Computer Science and Engineering

Course File (Theory)

Course Code & Name: CSE11004 &Switching Circuits and Logic Design
Course Coordinator: Mr. Nirmal Das

THEORY COURSE FILE CONTENTS

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Check list Course Outcomes Attainment

S. No.	Contents	Available (Y/N/NA)	Date of Submission	Signature of HOD
1.	Authenticated Syllabus Copy	Y	03.09.21	
2.	Individual Time Table	Y		
3.	Students' Name List (Approved Copy)	Y		
4.	Course Plan, PO, PSO, COs, CO-PO Mapping, COA Plan, Session Plan and Periodic Monitoring	Y		
5.	Previous Year End Semester Question Papers	N		
6.	Question Bank (All Units - Part A, Part B & C)	Y		
7.	Dissemination of Syllabus and Course Plan to Students	Y		
8.	Lecture Notes - Unit I, II & III	Y		
9.	**Sample Documents and Evaluation Sheet for Internal Assessment I** – Tutorials / Assignments / Class Test / Open Book Test / Quiz / Project / Seminar / Role Play if any	Y	08.11.21	
10.	**Mid Term Examination** A. Question Paper / Assessment Tools Used B. Sample Answer Scripts (Best, Average, Poor) if required C. Evaluation Sheet D. Slow Learners List and Remedial Measures	Y		
11.	Lecture Notes – Unit IV & V	Y	08.11.21	
12.	Tutorial with Solutions - Unit IV & V	N		
13.	**Sample Documents and Evaluation Sheet for Internal Assessment II** – Tutorials / Assignments / Class Test / Open Book Test / Quiz / Project / Seminar / Role Play if any	N		
14.	**End Term Examination** A. Question Paper & Answer Key B. Sample Answer Scripts (Best, Average, Poor) if required C. Evaluation Sheet D. Slow Learners List and Remedial Measures.	Y		

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das **Course Code: CSE11004**
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15.	Content Beyond the Syllabus (Proof)			
16.	Innovative Teaching Tools Used for TLP			
17.	Details of Visiting Faculty Session / Industry Expert / Guest Lecture / Seminar / Field Visit / Webinars / Flipped Class Room / Blended Learning / Online Resources etc.			
18.	Consolidated Mark Statement	Y		
19.	Course End Survey (Indirect Assessment) & Consolidation	Y	8.11.21	
20.	CO Attainment (Mid Term + Class Assessment + End Term)	Y		
21.	Gap Analysis & Remedial Measures	Y		
22.	CO - PO Attainment	Y		
23.	Class Record (Faculty Logbook)	Y		

Nirmal Das

Signature of HOD/ Dean **Signature of Faculty**

Date: **Date: 14.11.21**

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das **Course Code: CSE11004**
7. Course : Switching Circuits And Logic Design **L: 3**
8. Program : B.Tech **T: 0**
9. Target : 60% **P: 0**
C: 3

CSE11004	Switching Circuits And Logic Design	L	T	P	C
Version 1.0	Contact Hour -45	3	0	0	3
Pre-requisites/Exposure	Basic Idea of Digital Electronics and Number System				
Co-requisites	Knowledge of Logical Reasoning and Analysis				

Syllabus Copy

Course Objectives

1. To introduce an overview of logic families.
2. To develop students for building k-map.
3. To provide the students a detailed analysis of sequential circuit.
4. To introduce the students to formalize with ASM chart.

Course Content

Unit I: **6 lecture hours**

Switching Circuits: Logic families: TTL, nMOS, CMOS, dynamic CMOS and pass transistor logic (PTL) circuits, inverters and other logic gates, area, power and delay characteristics, concepts of fan-in, fan-out and noise margin.

Unit II: **10 lecture hours**

Switching theory: Characters used in C, Identifiers, Keywords, Data type & sizes, Constants & Variables, Various Operators used such as Arithmetic Operators, Relational & Logical Operators, Increment & Decrement Operators, Assignment Operators, Conditional or Ternary Operators, Bitwise Operators & Expressions; Standard Input & Output, formatted input scanf( ), formatted output printf( ); Flow of Control, if-else, switch-case, Loop Control Statements, for loop, while loop, do-while loop, nested loop, break, continue, goto, label and exit( ) function

Unit III: **10 lecture hours**

Combinational logic circuits: Realization of Boolean functions using NAND/NOR gates, Decoders, multiplexers. logic design using ROMs, PLAs and FPGAs. Case studies, fault diagnosis of combinational circuits

Unit IV **15 lecture hours**

Year: 2021
Semester:III

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7. Course : Switching Circuits And Logic Design **L: 3**
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9. Target : 60% **P: 0**
C: 3

Sequential circuits: Clocks, flip-flops, latches, counters and shift registers, finite-state machine model, Mealy and Moore machines, synthesis of synchronous sequential circuits, Conversion of Mealy m/c to Moore m/c and vice-versa, minimization and state assignment, Incompletely specified m/c's, asynchronous sequential circuit synthesis.

Unit V **4 lecture hours**

ASM charts: Representation of sequential circuits using ASM charts, synthesis of output and next state functions, data path control path partition-based design.

References:

Text Books

1. Morris Mano: Digital Logic Design, PHI.
2. S. Salivahanan and S. Arivazhagan: Analog and Digital Electronics, McGraw-Hill.

Reference Books

1. A Anand Kumar: Fundamentals of Digital Circuits, PHI
2. R P Jain: Modern Digital Electronics, McGraw-Hill.

Web Resource

https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
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8. Program : B.Tech — T: 0
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C: 3

Faculty Individual Time Table

ADAMAS UNIVERSITY									
SCHOOL OF ENGINEERING AND TECHNOLOGY									
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING									
Routine of Mr. Nirmal Das for Odd Semester 2021-22									
DAY	**09:40-10:30**	**10:30-11:20**	**11:20-12:10**	**12:10-01:00**	**01:00-01:50**	**01:50-02:40**	**02:40-03:30**	**03:30-04:20**	**04:20-05:10**
Monday	-								
Tuesday	Switching Ckts CSE B(2003)		Switching Ckts CSE A (2002)						
Wednesday	-								
Thursday					Switching Ckts CSE B (2003)	Switching Ckts CSE A (2002)			
Friday		Switching Ckts CSE A (2002)	Switching Ckts CSE B (2003)						

Nirmal Das

Signature of HOD — **Signature of Class Coordinator**

Date: — **Date:**

Students Name List

Roll Number	Registration Number	Name of the Student
UG/02/BTCSE/2020/014	AU/2020/0004474	Abhishek Thakur

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

UG/02/BTCSE/2020/016	AU/2020/0004476	Rhythm Sen
UG/02/BTCSE/2020/019	AU/2020/0004480	Sagar Ghosh
UG/02/BTCSECSF/2020/007	AU/2020/0005551	Md. Dawood Khan
UG/02/BTCSE/2020/021	AU/2020/0004491	Swapnodip Das
UG/02/BTCSE/2020/024	AU/2020/0004512	Aditya Kumar
UG/02/BTCSE/2020/029	AU/2020/0004531	Rohan Sutradhar
UG/02/BTCSE/2020/030	AU/2020/0004532	Prathama Sarkar
UG/02/BTCSE/2020/037	AU/2020/0004571	Arpan Maity
UG/02/BTCSE/2020/038	AU/2020/0004576	Animesh Dutta
UG/02/BTCSE/2020/039	AU/2020/0004577	Aritra Biswas
UG/02/BTCSE/2020/040	AU/2020/0004579	Soumik Das
UG/02/BTCSE/2020/043	AU/2020/0004584	Atanu Chowdhury
UG/02/BTCSE/2020/044	AU/2020/0004586	Subhadeep Kar
UG/02/BTCSE/2020/045	AU/2020/0004591	Priyesh Chanda
UG/02/BTCSE/2020/013	AU/2020/0004473	Vishesh Mohanty
UG/02/BTCSE/2020/015	AU/2020/0004475	Subhendhu Roy
UG/02/BTCSE/2020/017	AU/2020/0004477	Ashish Kumar Singh
UG/02/BTCSE/2020/031	AU/2020/0004537	Brinta Deb
UG/02/BTCSE/2020/023	AU/2020/0004506	Subrata Hazra
UG/02/BTCSE/2020/048	AU/2020/0005466	Pragati Kedia
UG/02/BTCSEAIML/2020/005	AU/2020/0004544	Dron Guin
UG/02/BTCSEAIML/2020/010	AU/2020/0004567	Srijita Saha
UG/02/BTCSEAIML/2020/012	AU/2020/0004574	Sahid Alam
UG/02/BTCSEAIML/2020/014	AU/2020/0004581	Sayanik Sutradhar
UG/02/BTCSEAIML/2020/003	AU/2020/0004528	Biswajit Chakrobarty
UG/02/BTCSEAIML/2020/007	AU/2020/0004559	Debrup Dey
UG/02/BTCSEAIML/2020/001	AU/2020/0004518	Surya Chakraborty
UG/02/BTCSE/2020/025	AU/2020/0004516	Anushka Khatua
UG/02/BTCSEAIML/2020/004	AU/2020/0004538	Pritom Saha
UG/02/BTCSECSF/2020/001	AU/2020/0004508	Shibsankar Saw
UG/02/BTCSECSF/2020/005	AU/2020/0004558	Nilanjana Roy

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

UG/02/BTCSECSF/2020/004	AU/2020/0004554	Ayush Kr. Singh
UG/02/BTCSECSF/2020/002	AU/2020/0004527	Mayank Pareek
UG/02/BTCSE/2020/020	AU/2020/0004490	Deeptanu Saha
UG/02/BTCSEAIML/2020/002	AU/2020/0004519	Rishav Ghosh
UG/02/BTCSE/2020/050	AU/2020/0005525	Jit Chatterjee
UG/02/BTCSE/2020/008	AU/2020/0004464	Arkadeep Chatterjee
UG/02/BTCSE/2020/012	AU/2020/0004472	Sougata Dutta
UG/02/BTCSE/2020/032	AU/2020/0004540	Alnas Hossain
UG/02/BTCSE/2020/001	AU/2020/0004250	Alok Dutta
UG/02/BTCSECSF/2020/006	AU/2020/0004587	Sabyasachi Paul
UG/02/BTCSEAIML/2020/015	AU/2020/0004588	Chandrachur Majhi
UG/02/BTCSE/2020/033	AU/2020/0004549	Vivek Raj
UG/02/BTCSEAIML/2020/013	AU/2020/0004578	Md. Sohail Irfan
UG/02/BTCSE/2020/007	AU/2020/0004462	Suraj Majumder
UG/02/BTCSE/2020/022	AU/2020/0004494	Indranil Das
UG/02/BTCSE/2020/034	AU/2020/0004562	Soyata Saha
UG/02/BTCSE/2020/002	AU/2020/0004275	Sunanda Jana
UG/02/BTCSE/2020/009	AU/2020/0004466	Ritushna Roy
UG/02/BTCSE/2020/011	AU/2020/0004468	Prima Giri
UG/02/BTCSE/2020/047	AU/2020/0004596	Shiuli Mahata
UG/02/BTCSE/2020/036	AU/2020/0004569	Nandini Roy
UG/02/BTCSE/2020/052	AU/2020/0005542	Anirban Roy
UG/02/BTCSE/2020/046	AU/2020/0004593	Hritik Kumar Dutta
UG/02/BTCSE/2020/028	AU/2020/0004530	Ayan Kumar Das
UG/02/BTCSE/2020/018	AU/2020/0004479	Protyush Kumar Chatterjee
UG/02/BTCSE/2020/041	AU/2020/0004580	Raja Banik
UG/02/BTCSE/2020/042	AU/2020/0004583	Arshad Raza
UG/02/BTCSEAIML/2020/011	AU/2020/0004572	Subarno Bhowmik
UG/02/BTCSE/2020/035	AU/2020/0004565	Nikhil Kumar Jha
UG/02/BTCSEAIML/2020/006	AU/2020/0004557	Soumyadwip Maity
UG/02/BTCSE/2020/003	AU/2020/0004276	Supratim Tarun Nath
UG/02/BTCSE/2020/004	AU/2020/0004451	Abhipsit Bhattachajee
UG/02/BTCSEAIML/2020/009	AU/2020/0004563	Rohit Kumar Roy

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

	AU/2021/0006008	Pratiksha Singha
	AU/2021/0006404	Anaita Pal
	AU/2021/0006331	Sagardeep Das

Nirmal Das

Signature of HOD/Dean **Signature of Class Coordinator**

Date: **Date:**

COURSE PLAN

Target	60% (marks)
Level-1	50% (population)
Level-2	60% (population)
Level-3	70% (population)

1. Method of Evaluation

UG	**PG**
Internal Assessment (30%) (Quizzes/Tests, Assignments & Seminars etc.)	Internal Assessment (30%) (Quizzes/Tests, Assignments & Seminars etc.)
Mid Semester Examination (20%)	Mid Semester Examination (20%)
End Semester Examination (50%)	End Semester Examination (50%)

*Keep as per Program (UG/PG)

2. Passing Criteria

Scale	**PG**	**UG**
Out of 10 Point Scale	CGPA – "5.00" Min. Individual Course Grade – "C" Passing Minimum – 40	CGPA – "5.00" Min. Individual Course Grade – "C" Passing Minimum – 35

*Keep as per Program (UG/PG)

3. Pedagogy

- **Direct Instruction**
- Kinesthetic Learning
- **Flipped Classroom**
- Differentiated Instruction
- Expeditionary Learning
- Inquiry Based Learning
- Game Based Learning
- Personalized Learning

4. Topics introduced for the first time in the program through this course

- (New Topic – Content Beyond Syllabus – Lean Construction)

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
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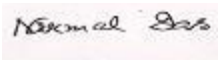
9. **Target : 60%** **P: 0**
C: 3

5. References:

Text Books	Web resources	Journals	Reference books
2	1	0	2



Signature of HOD/Dean **Signature of Faculty**

Date: **Date: 14.11.21**

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das **Course Code: CSE11004**

7. Course : Switching Circuits And Logic Design **L: 3**

8. Program : B.Tech **T: 0**

9. Target : 60% **P: 0**

C: 3

GUIDELINES TO STUDY THE SUBJECT

Instructions to Students:

1. Go through the 'Syllabus' in the LMS in order to find out the Reading List.
2. Get your schedule and try to pace your studies as close to the timeline as possible.
3. Get your on-line lecture notes (Content, videos) at Lecture Notes section. These are our lecture notes. Make sure you use them during this course.
4. check your LMS regularly
5. go through study material
6. check mails and announcements on blackboard
7. keep updated with the posts, assignments and examinations which shall be conducted on the blackboard
8. Be regular, so that you do not suffer in any way
9. C**ell Phones and other Electronic Communication Devices:** Cell phones and other electronic communication devices (such as Blackberries/Laptops) are not permitted in classes during Tests or the Mid/Final Examination. Such devices MUST be turned off in the class room.
10. **E-Mail and online learning tool:** Each student in the class should have an e-mail id and a pass word to access the LMS system regularly. Regularly, important information – Date of conducting class tests, guest lectures, via online learning tool. The best way to arrange meetings with us or ask specific questions is by email and prior appointment. All the assignments preferably should be uploaded on online learning tool. Various research papers/reference material will be mailed/uploaded on online learning platform time to time.
11. **Attendance:** Students are required to have minimum attendance of 75% in each subject. Students with less than said percentage shall NOT be allowed to appear in the end semester examination.

This much should be enough to get you organized and on your way to having a great semester! If you need us for anything, send your feedback through e-mail nirmal1.das@adamasuniversity.ac.in Please use an appropriate subject line to indicate your message details.

There will no doubt be many more activities in the coming weeks. So, to keep up to date with all the latest developments, please keep visiting this website regularly.

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
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9. **Target : 60%** **P: 0**
C: 3

RELATED OUTCOMES

1. The expected outcomes of the Program are:

PO1	Engineering Knowledge.
PO2	Problem analysis.
PO3	Design/development of solutions.
PO4	Conduct investigations of complex problems.
PO5	Modern tool usage.
PO6	The engineer and society.
PO7	Environment and sustainability.
PO8	Ethics.
PO9	Individual and team work.
PO10	Communication.
PO11	Project management and finance.
PO12	Life-long Learning.

2. The expected outcomes of the Specific Program are: (up to 3)

PSO1	Adequate strong skills in learning new programming environments, analyse and design algorithms for efficient computer-based systems of varying complexity.
PSO2	The ability to understand the evolutionary changes in computing, apply standard practices and strategies in software project development using open-ended programming environments to deliver a quality product for business success, real.
PSO3	Ability to analyse the impact of Computer Science and Engineering solutions in the societal and human context, design, model, develop, test and manage complex situations.

Year: 2021
Semester:III

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9. **Target : 60%** **P: 0**
C: 3

3. **The expected outcomes of the Course are: (minimum 4 and maximum 6)**

CO1	**Understand** and construct the basic design principles of logic gate.
CO2	**Understand** the different fabrication techniques used in Bipolar, CMOS and PLA.
CO3	**Formalize** with mealy and Moore machine.
CO4	**Construct** ROM design.

4. Co-Relationship Matrix
Indicate the relationships by 1- Slight (Low) 2- Moderate (Medium) 3-Substantial (High)

Program Outcomes / Course Outcomes	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
CO2	3	1	-	-	3	2	-	-	-	-	-	-	-	-	-
CO3	3	1	-	-	3	2	1	-	-	-	-	-	-	-	-
CO4	3	-	-	-	3	-	-	-	-	-	-	-	-	-	-
Average	**3**	**1**	-	-	**3**	**2**	**1**	-	-	-	-	-	-	-	-

5. Course Outcomes Assessment Plan (COA):

Course Outcomes	Internal Assessment* (30 Marks)		Mid Term Exam (20 Marks)	End Term Exam (50 Marks)	Total (100 Marks)
	Before Mid Term	Before End Term			
CO1	5	NA	10	10	25
CO2	5	NA	5	15	25
CO3	10	NA	5	15	30
CO4	NA	10	NA	10	20
Total	20	10	20	50	100

* Internal Assessment – Tools Used: Tutorial, Assignment, Seminar, Class Test etc.

Year: 2021
Semester:III

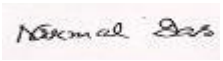
6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

OVERVIEW OF COURSE PLAN OF COURSE COVERAGE

Course Activities:

S. No.	Description	Planned			Actual			Remarks
		From	To	No. of Session	From	TO	No. of Session	
1.	Switching Circuits	03.09.21	17.09.21	8	03.09.21	17.09.21	8	
2.	Switching theory	21.09.21	02.11.21	10	21.09.21	29.10.21	10	
3.	Combinational logic circuits	09.11.21	30.11.21	10	09.11.21	-	10	
4.	Sequential circuits	02.12.21	30.11.21	12	-	-	12	
5.	ASM charts	22.12.21	30.12.21	5	-	-	5	

Total No. of Instructional periods available for the course: 45 Sessions



Signature of HOD/Dean

Date:

Signature of Faculty

Date: 14.11.21

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
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C: 3

SESSION PLAN

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	03.09.21	Logic families.	CO1	1	03.09.21	Logic families.	CO1
2	07.09.21	System Applications TTL, nMOS, CMOS	CO1	2	07.09.21	System Applications TTL, nMOS, CMOS, dynamic CMOS and pass transistor logic (PTL) circuits.	CO1
3	09.09.21	Dynamic CMOS and pass transistor logic (PTL) circuits.	CO1	3	09.09.21	Dynamic CMOS and pass transistor logic (PTL) circuits.	CO1
4	10.09.21	Inverters and other logic gates.	CO1	4	10.09.21	Inverters and other logic gates.	CO1
5	14.09.21	Area, power and delay characteristics	CO1	5	14.09.21	Area, power and delay characteristics	CO1
6	16.09.21	Concepts of fan-in, fan-out and noise margin.	CO1	6	16.09.21	Concepts of fan-in, fan-out and noise margin.	CO1
7	17.09.21	Overall Summary	CO1	7	17.09.21	Overall Summary	CO1

UNIT-I

Remarks:

Signature of Faculty

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Date: 14.11.21

Year: 2021
Semester:III

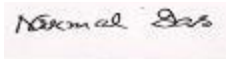
6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

SESSION PLAN
UNIT-II

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	21.09.21	Switching algebra, logic gates.	CO2	1	21.09.21	Switching algebra, logic gates.	CO2
2	23.09.21	Switching functions, truth tables.	CO2	2	23.09.21	Switching functions, truth tables.	CO2
3	24.09.21	Switching expressions, minimization of completely and incompletely specified switching functions.	CO2	3	24.09.21	Switching expressions, minimization of completely and incompletely specified switching functions.	CO2
4	28.09.21	Karnaugh map.	CO2	4	28.09.21	Karnaugh map.	CO2
5	30.09.21	Karnaugh map.	CO2	5	30.09.21	Karnaugh map.	CO2
6	01.10.21	Quine-McCluskey method	CO2	6	01.10.21	Quine-McCluskey method	CO2
7	05.10.21	Quine-McCluskey method	CO2	7	05.10.21	Quine-McCluskey method	CO2
8	26.10.21	Multiple output minimization, representation.	CO2	8	26.10.21	Multiple output minimization, representation.	CO2
9	28.10.21	Manipulation of functions using BDD's	CO2	9	28.10.21	Manipulation of functions using BDD's	CO2
10	02.11.21	Two-level and multi-level logic circuit synthesis.	CO2	10	02.11.21	Two-level and multi-level logic circuit synthesis.	CO2

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3



Remarks:

Signature of Faculty

Date: 14.11.21

Year: 2021
Semester:III

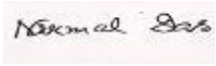
6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

SESSION PLAN
UNIT-III

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	09.11.21	Realization of Boolean functions using NAND/NOR gates.	CO2	1	09.11.21	Realization of Boolean functions using NAND/NOR gates.	CO2
2	11.11.21	Combinational Design Principal.	CO2	2	11.11.21	Combinational Design Principal.	CO2
3	12.11.21	Design of Half Adder, Full Adder	CO2	3	12.11.21	Design of Half Adder, Full Adder	CO2
4	16.11.21	Design of Half Subtractor, Full Subtractor.	CO2	4	16.11.21	Design of Half Subtractor, Full Subtractor.	CO2
5	18.11.21	Design of Full adder using Half Adder, Design of Adder cum Subtractor circuit.	CO2	5	18.11.21	Design of Full adder using Half Adder, Design of Adder cum Subtractor circuit.	CO2
6	19.11.21	Design Principle of Decoder.	CO2	6	19.11.21	Design Principle of Decoder.	CO2
7	23.11.21	Design of Multiplexer.	CO2	7	23.11.21	Design of Multiplexer.	CO2
8	25.11.21	Design of De-Multiplexer.	CO2	8	25.11.21	Design of De-Multiplexer.	CO2
9	26.11.21	Design of PLA and PAL.	CO2	9	26.11.21	Design of PLA and PAL.	CO2
10	30.11.21	Parity Bit, Check Bit, Parity Generator.	CO2	10	30.11.21	Parity Bit, Check Bit, Parity Generator.	CO2

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3



Remarks: **Signature of Faculty**

Date:

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

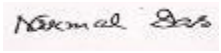
SESSION PLAN
UNIT-IV

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	02.12.2021	Introduction to sequential circuits and types of sequential circuits	CO3				
2	03.12.2021	Discussion on synchronous and asynchronous sequential circuits.	CO3				
3	07.12.2021	Clocks, Flip-flops and Latches	CO3				
4	09.12.2021	S R Latches, S R Flip-flop	CO3				
5	10.12.2021	D Flip-flop	CO3				
6	14.12.2021	T Flip-flop	CO3				
7	16.12.2021	Miscellaneous discussion on Latches and Flip-flops.	CO3				
8	17.12.2021	Counters and shift registers	CO3				
9	21.12.2021	Finite-state machine model, Mealy and Moore machines	CO3				

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

10	23.12.2021	Conversion of Mealy m/c to Moore m/c and vice-versa.	CO3				
11	26.12.2021	Minimization and state assignment	CO3				
12	30.12.2021	Incompletely specified m/c's, asynchronous sequential circuit synthesis.	CO3				



Remarks:

Signature of Faculty

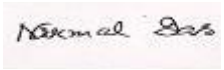
Date: 14.11.21

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

SESSION PLAN
UNIT-V

Session Plan				Actual Delivery			
Lect.	Date	Topics to be Covered	CO Mapped	Lect.	Date	Topics Covered	CO Achieved
1	04.01.2022	ASM Chart	CO4				
2	06.01.2022	Representation of sequential circuit using ASM Chart	CO4				
3	07.01.2022	Synthesis of output and next state function	CO4				
4	11.01.2022	Data Path, Control Path partition-based design	CO4				
5	13.01.2022	Overall discussion with application area and example.	CO4				



Remarks:

Signature of Faculty

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Date:14.11.21

Year: 2021
Semester:III

6.	**Name of the Faculty: Nirmal Das**		**Course Code: CSE11004**
7.	**Course**	**: Switching Circuits And Logic Design**	**L: 3**
8.	**Program**	**: B.Tech**	**T: 0**
9.	**Target**	**: 60%**	**P: 0**
			C: 3

Lecture Notes

Lecture notes are available in One Drive

(https://riceindia-my.sharepoint.com/:f:/g/personal/nirmal1_das_adamasuniversity_ac_in/EpCSQRrzvzhAj_yAHnmzEO0BhCLFQDRcYD_20STxTxpz3g?e=KVSSoR).

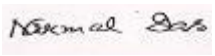
Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

PERIODIC MONITORING

Actual date of completion and remarks, if any

Components		From	To	From	To
Duration (Mention from and to Dates)					
Percentage of Syllabus covered					
Lectures	Planned				
	Taken				
Tutorials	Planned				
	Taken				
Test/Quizzes/ Mid Semester/ End Semester	Planned				
	Taken				
	CO's Addressed				
	CO's Achieved				
Assignments	Planned				
	Taken				
	CO's Addressed				
	CO's Achieved				
Signature of Faculty					
Head of the Department					
OBE Coordinator					



Signature of HOD/ Dean

Date

Signature of Faculty

Date: 14.11.21

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

PERIODIC MONITORING

Attainment of the Course (Learning) Outcomes:

Components	Attainment level	Action Plan	Remarks
Assignment	CO1:		
	CO2:		
	CO3:		
	CO4:		
	CO5:		
Quiz/Test etc.	CO1:		
	CO2:		
	CO3:		
	CO4:		
	CO5:		
Mid Semester	CO1:		
	CO2:		
	CO3:		
	CO4:		
	CO5:		-
End Semester	CO1:		
	CO2:		
	CO3:		
	CO4:		
	CO5:		
Any Other	CO1:		
	CO2:		
	CO3:		
	CO4:		
	CO5:		

Nirmal Das

Signature of HOD/ Dean

Date

Signature of Faculty

Date 14.11.21

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

Evaluation Sheet – Mid Semester

	ADAMAS UNIVERSITY **MID-SEMESTER EXAMINATION** (Academic Session: 2020 – 21)		
Name of the Program:	B.Tech in CSE	**Semester:**	II
Paper Title:	Switching Circuit and Logic Design	**Paper Code:**	CSE11004
Maximum Marks:	20	**Time Duration:**	2 Hrs
Total No. of Questions:	8	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)	**1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

Group A **Answer All the Questions (5 x 1 = 5)**			
1			
2			
3			
4			
5			
Group B **Answer All the Questions (3 x 5 = 15)**			

Year: 2021

Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0

C: 3

Roll Number	Registration Number	Name of the Student	Marks (20)

Nirmal Das

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

Signature of HOD/Dean — **Signature of Faculty**

Date: — **Date: 14.11.21**

Planning for Remedial Classes – Mid Semester

Sl. No.	Name of Student	Roll No.	Reg. No.	Mid Sem Marks	Remedial Classes Held							Class test on the basis of Remedial Classes	End Sem Marks	Improvement (Y/N)
					Date									
					Venue									
					Time									
1.														
2.														

Signature of HOD/ Dean — **Signature of Faculty**

Date: — **Date:**

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**

C: 3

Evaluation Sheet (End Semester)

Roll Number	Registration Number	Name of the Student	Marks (50)

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

Nirmal Das

Signature of HOD/Dean — **Signature of Faculty**

Date: — **Date: 14.11.21**

End Semester Question Papers – Set 1

ADAMAS UNIVERSITY PURSUE EXCELLENCE	**ADAMAS UNIVERSITY** **END SEMESTER EXAMINATION** (Academic Session: 2020 – 21)		
Name of the Program:	B.Tech in CSE	**Semester:**	III
Paper Title:	Switching Circuit and Logic Design	**Paper Code:**	CSE11004
Maximum Marks:	50	**Time Duration:**	3 Hrs
Total No. of Questions:	**17**	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)	**1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

Group A **Answer All the Questions (5 x 1 = 5)**			

Year: 2021

Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0

C: 3

End Semester Question Papers – Set 2

ADAMAS UNIVERSITY PURSUE EXCELLENCE

ADAMAS UNIVERSITY

END SEMESTER EXAMINATION

(Academic Session: 2020 – 21)

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Name of the Program:	B.Tech in CSE	**Semester:**	III
Paper Title:	Switching Circuit and Logic Design	**Paper Code:**	CSE11004
Maximum Marks:	50	**Time Duration:**	3 Hrs
Total No. of Questions:	**17**	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)	**4.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **5.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **6.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

Group A **Answer All the Questions (5 x 1 = 5)**			
Group B **Answer All the Questions (5 x 2 = 10)**			
Group C **Answer All the Questions (7 x 5 = 35)**			

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Planning for Remedial Classes – End Semester

Sl. No.	Name of Student	Roll No.	Reg. No.	End Sem Marks	Remedial Classes Held							Class test on the basis of Remedial Classes	Supple Exam Marks	Improvement (Y/N)
					Date									
					Venue									
					Time									
1.														

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

2.														

Signature of HOD/ Dean — Signature of Faculty

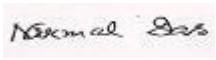
Date — Date

Consolidated Mark Statement

Roll Number	Registration Number	Name of the Student	Marks			
			Mid Semester (20)	Internal Assessment (30)	End Semester (50)	Total (100)

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3



Signature of Dean/HOD **Signature of Faculty**

Date: **Date: 14.11.21**

COURSE END SURVEY

INDIRECT ASSESSMENT

Sample format for Indirect Assessment of Course outcomes:

NAME: xxxxx
ENROLLMENT NO: -
REG. No.: -
COURSE: Switching Circuit and Logic Design
PROGRAM: B.Tech in CSE

Please rate the following aspects of course outcomes of

Use the scale 1-3*

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

Course Outcomes	Statement	1	2	3
CO1	**Understand** and construct the basic design principles of logic gate.			3
CO2	**Understand** the different fabrication techniques used in Bipolar, CMOS and PLA.			3
CO3	**Can formalize** with mealy and Moore machine.			3
CO4	**Can construct** ROM design.			3

* 1 WEAK 2 MODERATE 3 STRONG

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

INDIRECT ASSESSMENT CONSOLIDATION

ADAMAS UNIVERSITY, KOLKATA
SCHOOL OF
DEPARTMENT OF
CO Indirect Assessment

Programme: B.Tech in CSE — **Academic Year:2020-21**
Batch: 2020-22

Course Code & Name: Switching Circuit and Logic Design CSE11004

Course Outcome	Students Feed Back	Attainment
CO1		
CO2		
CO3		
CO4		

Signature of HOD/Dean
Date:

Nirmal Das
Signature of Faculty
Date: 14.1121

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

CO ATTAINMENT – GAP ANALYSIS & REMEDIAL MEASURES

ADAMAS UNIVERSITY, KOLKATA
SCHOOL OF
DEPARTMENT OF
CO ATTAINMENT - GAP ANALYSIS & REMEDIAL MEASURES

Batch :	2020-22				Academic Year:	2020-21
Course Code & Name		Name of the Coordinator			Year & Semester	
CSE11004 Switching Circuit and Logic Design		Nirmal Das			I & II	

CO	Direct Assessment	Indirect Assessment	CO Attainment	Target	CO Attainment Gaps	Action for Bridge the Gap	Target Modification
CO1							
CO2							
CO3							
CO4							

Nirmal Das

Signature of HOD/Dean

Date:

Signature of Faculty

Date: 14.11.21

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das — Course Code: CSE11004
7. Course : Switching Circuits And Logic Design — L: 3
8. Program : B.Tech — T: 0
9. Target : 60% — P: 0
C: 3

CO-PO ATTAINMENT

ADAMAS UNIVERSITY, KOLKATA
SCHOOL OF
DEPARTMENT OF
CO-PO ATTAINMENT

Programme:B.Tech In CSE	Year & Sem: I & II	Academic Year: 2020-21	Batch:2020-22

Course Code	Course Name	CO-PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
		Relationship															
		Mapping Value									-	-	-	-	-	-	-
		Attainment									-	-	-	-	-	-	-

Signature of HOD/Dean

Signature of Faculty

Date:

Date:14.11.21

Year: 2021
Semester:III

6. **Name of the Faculty: Nirmal Das** **Course Code: CSE11004**
7. **Course : Switching Circuits And Logic Design** **L: 3**
8. **Program : B.Tech** **T: 0**
9. **Target : 60%** **P: 0**
C: 3

PO ATTAINMENT OF THE COURSE

Nirmal Das

Signature of HOD/Dean

Date:

Signature of Faculty

Date: 14.11.21

Year: 2021
Semester:III

6. Name of the Faculty: Nirmal Das **Course Code: CSE11004**

7. Course : Switching Circuits And Logic Design **L: 3**

8. Program : B.Tech **T: 0**

9. Target : 60% **P: 0**

C: 3

INSTRUCTIONS FOR FACULTY

Instructions for Faculty

- Faculty should keep track of the students with low attendance and counsel them regularly.
- Course coordinator will arrange to communicate the short attendance (as per University policy) cases to the students and their parents monthly.
- Topics covered in each class should be recorded in the table of RECORD OF CLASS TEACHING (Suggested Format).
- Internal assessment marks should be communicated to the students twice in a semester.
- The file will be audited by respective Academic Monitoring and Review Committee (AMRC) members for theory as well as for lab as per AMRC schedule.
- The faculty is required to maintain these files for a period of at least three years.
- This register should be handed over to the head of department, whenever the faculty member goes on long leave or leaves the Colleges/University.
- For labs, continuous evaluation format (break-up given in the guidelines for result preparation in the same file) should be followed.
- Department should monitor the actual execution of the components of continuous lab evaluation regularly.
- Instructor should maintain record of experiments conducted by the students in the lab weekly.
- Instructor should promote students for self-study and to make concept diary, due weightage in the internal should be given under faculty assessment for the same.
- Course outcome assessment: To assess the fulfilment of course outcomes two different approaches have been decided. Degree of fulfillment of course outcomes will be assessed in different ways through direct assessment and indirect assessment. In Direct Assessment, it is measured through quizzes, tests, assignment, Mid-term and/or End-term examinations. It is suggested that each examination is designed in such a way that it can address one or two outcomes (depending upon the course completion). Indirect assessment is done through the student survey which needs to be designed by the faculty (sample format is given below) and it shall be conducted towards the end of course completion. The evaluation of the achievement of the Course Outcomes shall be done by analyzing the inputs received through Direct and Indirect Assessments and then corrective actions suggested for further improvement.
- **Submission Targets of Course Contents:**
  - **S. No. 1 to 8 : Before Starting the Course**
  - **S. No. 9 & 10 : After Mid Semester Examination**
  - **S. No. 11 to 18 : Immediately After End Semester Examination**
  - **S. No. 19 to 23 : After Declaration of Result of the Course**