Al-Balqa' Applied University

Faculty of Engineering Technology

Department of Computer Engineering

جامعة البلقاء التطبيقية
كلية الهندسة التكنولوجية

قسم هندسة الحاسوب

تأسست سنة 1997

Course Name: Computer Architecture and Organization	**Course No.:** 302007232
Credit hours: 3	**Pre-requisites:** Logic Design
Instructors: Dr. Jamil AL-Azzeh Email: randa.dallah@fet.edu.jo	

Text Book and References :

- **A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, 3rd Edition, Revised Printing, Morgan Kaufmann Publishing Co., Menlo Park, CA., June 2007.**
- **د. زياد القاضي، معمارية (هيكلية) وتنظيم الحاسوب، الطبعة الاولى 1994، دار صفاء للنشر و التوزيع**
- **J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 4th Edition, Morgan Kaufmann Publishing Co., Menlo Park, CA. 2006.**
- **William Stallings. *Computer Organization and Architecture: Designing for Performance*. Prentice Hall Publishers.**
- **R. Y. Kain, *Advanced Computer Architecture: A System Design Approach*, Prentice Hall, 1996.**
- **Instructor handouts, homework assignments and white board notes.**

Course Description : Evaluation of different computer architectures performance with respect to price/performance and its relation to architectural design choices. Instruction set design, Arithmetic Unit design, memory hierarchy, input/output, interrupts and exceptions, microprocessor design, pipelining & multiprocessing, and MIPS assembly language programming.

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Learning Outcomes : Upon successful completion of this course, students:

- Should be able to know basic terms associated with Computer Architecture, such as MIPS, Throughput, Performance, Pipelining, Structure hazards, Control hazards, Data hazards, etc.
- Should be able to design the datapath and control of the MIPS architecture.
- Should be able to measure performance of different architectures.
- Should be able to understand the design of the pipelined datapath and pipelined control of the MIPS architecture.
- Should be able to design cache memory using direct mapping, set associative, and fully associative.

Grading Policy :

First Exam	:	20 %
Second Exam	:	20 %
Activities (Quizzes)	:	10%
Final Exam	:	50 %

Course Outline :

1- Computer Abstraction and Technology:

- Introduction.
- Below your Program (Level of Abstraction).
- Basics of Computer Architecture.
- RISC and CISC Architecture.

2- Instructions: Language of the Machine (Instruction Set Architecture ISA for MIPS):

- Introduction.
- Operations of the Computer Hardware.
- Operands of the Computer Hardware.
- Representing Instructions in the Computer.
- Logical Operations.
- Instructions for making Decisions.
- MIPS Addressing for 32-Bit Immediates and Addresses.

3- The Role of Performance

- Measuring Performance and Relating the Metrics.
- How to Improve Performance.
- Comparing and Summarizing Performance.
- Real Stuff: Two SPEC Benchmarks and the Performance of Recent Intel Processors.

4- Arithmetic for Computers:

- Introduction.
- Signed and Unsigned Numbers.
- Addition and Subtraction.
- Multiplication.
- Division.

5- The Processor Design: Datapath and Control

- ALU Design.
- Designing MIPS Processor (Single_Cycle).
  - Datapath.
  - Control Unit.
  - Problems with single cycle Datapath.
- Designing MIPS Processor (Multi_Cycle).
  - Datapath.
  - Control Unit.
- Microprogramming: Simplifying Control Design.

6- Enhancing Performance with Pipelining:

- An Overview of Pipelining.
- A Pipelined Datapath.
- Pipelined Control.
- Data Hazards and Stalls.
- Branch Hazards.

7- Cache Memory Design

- The Basics of Caches.
- Measuring and Improving Cache Performance.
- A Common Framework for Memory Hierarchies.
- Mapping Methods:
  - Direct Mapping.
  - Set Associative Mapping.
  - Full Associative Mapping.