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संगणक विज्ञान एंव अभियांत्रिकी विभाग / DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
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No:- Date:

CSX4164: Computer System Parallelism

L-T-P-Cr: 3-0-0-3

Prerequisites: Computer Organization.

Course Overview: The purpose of this course is to impart fundamental concepts of parallelism in computer architecture and microarchitecture, relating to contemporary parallel processing systems.

Course Outcomes – After completing this course, students should be able to:

CO-1. *recall* computer system parallelism terminologies, as well as fundamental concepts, operating principles and methods about structures and functions of parallel processing systems and their components;
[Bloom level: *Remember*; Mapped to: PO-1]

CO-2. *explain* concepts and techniques in functioning of instruction-level, data-level and thread-level, request-level and application-specific parallelism of computer systems;
[Bloom level: *Understand*; Mapped to: PO-1, PO-2]

CO-3. *solve* problems on principles of instruction pipelining, vector pipelining, multithreading and cache coherency, as well as performances of superscalar microprocessor, supercomputer, symmetric multiprocessor and NUMA systems;
[Bloom level: *Apply*; Mapped to: PO-1, PO-2, PO-3]

CO-4. *implement* specified program objectives in parallel processing system for given ISA;
[Bloom level: *Apply*; Mapped to: PO-1, PO-2, PO-3]

CO-5. *determine* degree of parallelism, parallelism hazards, instruction issue scheduling, vectorizable sequence and vector/graphics pipelined schedule that are supported in a specific parallel processing system for given execution sequence;
[Bloom level: *Analyze*; Mapped to: PO-1, PO-2, PO-3]

CO-6. *evaluate* protocols of branch prediction, predication, static and dynamic multi-issue scheduling, and cache coherence in parallel processing systems.
[Bloom level: *Evaluate*; Mapped to: PO-1, PO-2, PO-4, PO-5]

Syllabus:

Unit I: (Computer System Parallelism) Lectures: 10

(Module-1) *Introduction*: Introduction to computer system parallelism; CISC and RISC systems; Instruction set architecture (ISA); Instruction cycle; Addressing modes; Computer system data path for ISA; Memory hierarchy; I/O techniques; Control logic sequencing.
(Module-2) *Processing Parallelism*: Computer system performance metrics; Processing system classification; Forms of Parallelism; SISD, SIMD, MIMD.

Unit II: (Pipelined Datapath) Lectures: 11

(Module-1) *Instruction-level Parallelism*: Nature of instruction-level parallelism (ILP); RAW, WAW, WAR dependencies; Scalar pipeline; Pipeline hazards and remedy techniques.
(Module-2) *Superscalar Pipelining*: Superscalar pipelining; Instruction issue policy; Dynamic multi-issue scheduling; Scoreboard; Tomasulo's algorithm; Loop unrolling; Hardware speculation; Speculative Tomasulo's algorithm.
(Module-3) *Static ILP*: Static multi-issue scheduling; VLIW; EPIC; Predication; Pipelines in CISC, RISC and VLIW/EPIC systems.

Unit III: (Data/Thread Parallelism) Lectures: 11

(Module-1) *Data-level Parallelism*: Nature of data-level parallelism; Vector architectures; Vector processor pipelining; Pipeline constraints; Convoy; Scalar expansion/reduction; Array processors; GPU architectures; Graphics pipeline; Streaming processor unified architecture.
(Module-2) *Thread-level Parallelism*: Nature of thread-level parallelism; Simultaneous multithreading; Shared-memory architectures; SMP systems; Cache coherence; Directory, snoopy, MSI protocols; NUMA, CC-NUMA systems; Multicore processor architectures; Amdahl's law.

Unit IV: (Request/Application-specific Parallelism) Lectures: 10

(Module-1) *Warehouse-scale Computing*: Request-level parallelism, Distributed-memory multiprocessor systems; Multicomputer systems; Clusters; MPPs; Warehouse and data center computers.
(Module-2) *Domain-specific Architecture*: Application specific integrated circuits (ASIC); Deep neural network core; Tensor processing unit.

Text/ Reference Book(s):

1. John L. Hennessy, David A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, Sixth edition, 2019.
2. David A. Patterson, John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufmann, Sixth edition, 2021.
3. William Stallings, *Computer Organization and Architecture: Designing for Performance*, Pearson Education, Eleventh edition, 2019.
4. Sarah L. Harris, David M. Harris, *Digital Design and Computer Architecture: ARM® Edition*, Morgan Kaufmann, 2016.
5. Barry B. Brey, *The Intel Microprocessors: Architecture, Programming, and Interfacing*, Pearson Education, Eighth edition, 2009.
6. Hesham El-Rewini, Mostafa Abd-El-Barr, *Advanced Computer Architecture and Parallel Processing*, John Wiley & Sons, 2005.