

Libre Silicon Token (LST)

Bridge the Open-Source Semiconductors and Hardware Markets

July 8, 2017

Abstract

Free and open-source (FOS^{1,2}) software development, for example the development of the Linux³ operating system, has already changed the economics of innovation. The Global Semiconductor Alliance reported that 80% of companies worldwide run FOS software. But this supercharging effect of openness is yet to be fully reached in the field of hardware, especially the semiconductor integrated circuit⁴ (aka chip) level, due to various hurdles. First, the intellectual property (IP) of chip design through FOS is not commercially available without verification of silicon through wafer fabrication⁵, which is time-consuming and costly even for low-volume prototyping production. It does not make economic sense for FOS chip developers to take such huge risks for a common good. Moreover, current inefficient IP license models and limited choice of proprietary Electronic Design Automation (EDA)⁶ tools raise market entry hurdles as well.

As the semiconductor industry's first solution to provide a missing link between FOS IP developers and hardware markets, Lanceville Technology, with FOS communities support, propose the Libre Silicon⁷ token (LST) networks aiming to make FOS chips commercially available and acceptable. This objective is accomplished via the LST "one-stop shop" networks that comprises a rapid prototyping minifab, FOS EDA tool sets, IP marketplace as well as our know-how in chip manufacturing.

¹ The term "free" or "Libre" in this paper means freedom to study, redistribute, change and improve. It doesn't mean free of charge or free of defects. Freedom is the goal while open source is the means to that goal.

² The term "open source" refers to something such as source code of software people can inspect, modify, enhance and share because its design is publicly accessible.

<https://opensource.com/resources/what-open-source>

³ As of June 2017, Linux powers the top 492 of the world's 500 most powerful supercomputers, most of the servers powering the Internet and tens of millions of Linux-based Android mobile phones and consumer devices. <https://www.linuxfoundation.org/>

⁴ Integrated circuit is an electronic circuit on one plate of semiconductor silicon wafer, material like compounds of silicon. Most computers and modern technology depend on it.

⁵ IP, IP core or IP block, which is short for "semiconductor intellectual property core", is a reusable unit of integrated circuit layout design that is the intellectual property of one party.

⁶ EDA, the software used to design new chips.

⁷ Compounds of silicon, with semiconductor properties, on which an integrated circuit has been built, are the most widely used in electronic devices.

The LST networks, with the support of a public smart contract⁸, is able to track the commercial usage of a particular IP entity, thus providing sustainable financial incentives for corresponding IP developers via distributed tamper-proof ledger(s).

WARNING

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By viewing this document, you acknowledge, accept and agree with LANCEVILLE TECHNOLOGY GROUP CO., LIMITED(hereinafter referred to as “Lanceville”) that:

(a)this document is only for the purpose of providing information about the operation of LST network, introducing LST as the right to access and use the LST network, and not for any other purposes.

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⁸ e.g., ERC20 and ERC223 are well-known Ethereum token standard which is used for Ethereum smart contracts.

Disclaimer

The LST is not a security of any kind in any jurisdiction. The LST is a digital token only for participation and use of the open-source circuitry development and exchange network and does not confer ownership of a stake in any business of Lanceville or any of its affiliates, partners, vendors, or advisors. It is generally to be used to buy and/or sell integrated circuit design or related prototype manufacturing services on LST network by the hardware makers, silicon chip designers, original equipment manufacturers, academics and researchers who are a part of the LST network, described herein.

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1 Current Problem: A Closed Fabless-Foundry⁹ Market

Before entering the market with competitive chip products, a fabless semiconductor company (“fabless”), or any chip design enthusiast from FOS communities, has to verify and/or redesign its silicon chip designs through at least one time, or maybe even more, of prototype process, that is low-volume test production in a semiconductor foundry (“fab”).

A fully equipped fab will require a significant capital inputs and this fact will only facilitate a positive-feedback-loop and only a couple of major players, such as Apple(a fabless)-TSMC(a fab), monopoly the whole industry.

Based on this fact, some of the fabless startups or chip enthusiasts will need to face some challenges when they deal with a fab. Some of the examples are listed as follows:

1.1 Entry barriers are high for a fabless

1.1.1 Un-controllable time lag in Multi-Project-Wafer shuttle services (MPW)

One of the common ways to get a small batch of chip prototypes is via the Multi-Project-Wafer shuttle services (MPW), which is provided by a fab to allow customers to share costs with other customers by processing multiple chip designs on a single photomask.

A typical chip production will involved 10-25 pieces of photomask. And because the photomask set is very expensive, starts in the five digits, to maximize the usage of one production run, the MPW shuttle will only be started until it has been fully booked. Some of extreme cases show that MPW would be eventually cancelled as the capacity is not fully loaded. Normally, it takes 4-6 months to run an MPW cycle, which is too long and too uncertain.

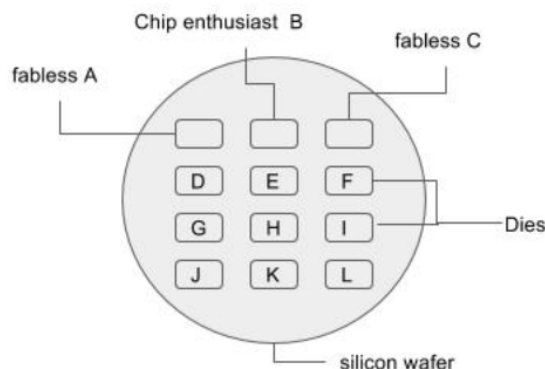


Figure 1.1 Book a MPW

Note: how many dies can be cut on one wafer depends on the size of the wafer. This figure just an example to show what is MPW.

⁹ A fabless company only focuses on chip designing and sales while a semiconductor foundry focuses on manufacturing the chips designed by fabless firms.

1.1.2 High price of IP block and EDA tools

Since a closed market will demotivate competition, the pricing of IP block, normally closed-source, and EDA tools will tend to be higher than the actual balanced prices. This is illustrated by a chart as below:

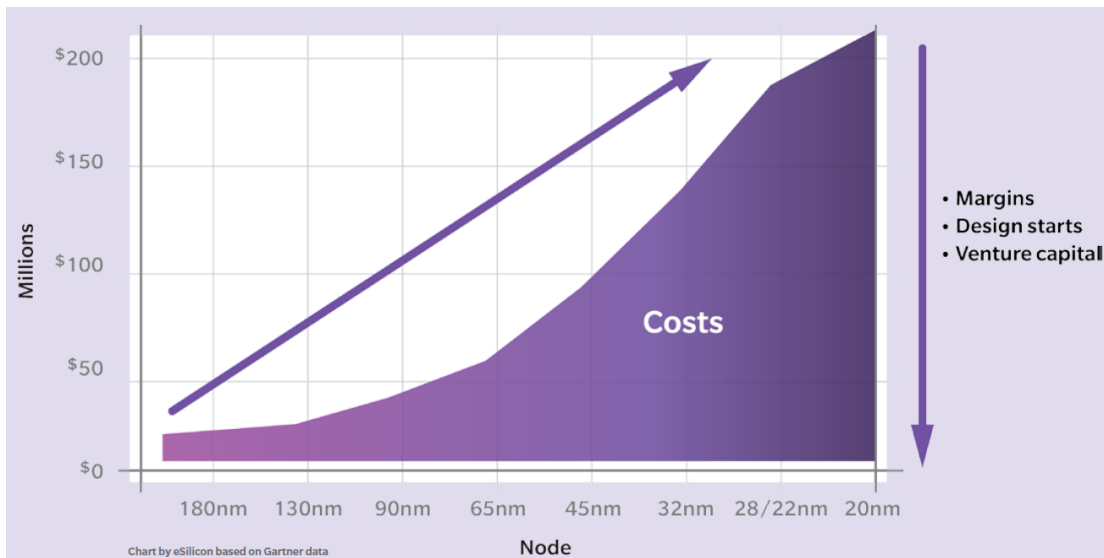


Figure 1.2 Growing costs for entering the semicon market¹⁰

1.2 Innovation impeded by closed source silicon

Besides costly and time-consuming prototyping process, rigidly closed source design libraries and IP blocks, which results in difficult access to leading-edge manufacturing process, has been slowed down the pace of fabless startups and discouraged talents or interesting parties to enter this field.

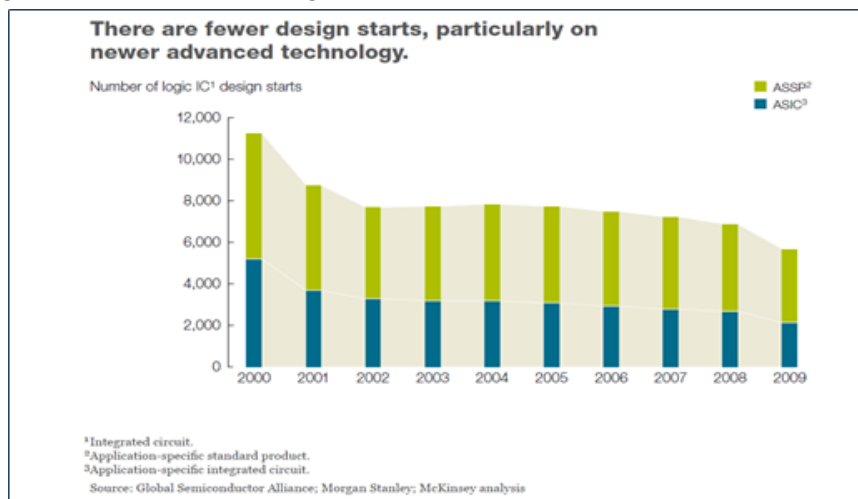


Figure 1.3 IC design innovation held up¹¹

¹⁰ Chart by eSilicon based on Gartner data.

¹¹ Source: McKinsey & Company, *The evolution of business models in a disrupted value chain*.

1.3 Security concerned over closed source silicon chip

With threats of potential “backdoor” enclosed, global open source communities have always been vigorously pushing for a totally open source computer. So far, while open source software and hardware prevalent around the world, a physical open source silicon chip hasn't yet to be produced.

1.4 High risk, low return for FOS chip developers

For FOS software developers, if the software doesn't work as expected, he or she can just rewrite it by putting more time into it. If it works, the developers could make money on it by delivering it directly to users online.

In contrast, if the prototype chip doesn't work, chip developers have to spend another 6 months, and tens of thousands of dollars more on a MPW run in order to fix bugs.

Hence, FOS chip developers always end their efforts with Verilog¹² source code of some projects published to the communities, then the source code, or IP blocks, stays where it's developed without a chance into the hands of hardware makers, let alone ordinary users. It's such a waste of global chip talents.

This is to some extent evidenced by the comparison between the Github¹³ or OpenCores¹⁴. While there are millions of open source software projects, 24 million developers, and 117 thousand businesses on GitHub, there are only 1208 open source hardware projects (different IP-blocks, mostly without silicon proven) at OpenCores. However, there is huge demand for open source hardware IP cores that 279'423 users registered at this community.

¹² A hardware description language, most commonly used in the design and verification of digital circuits.

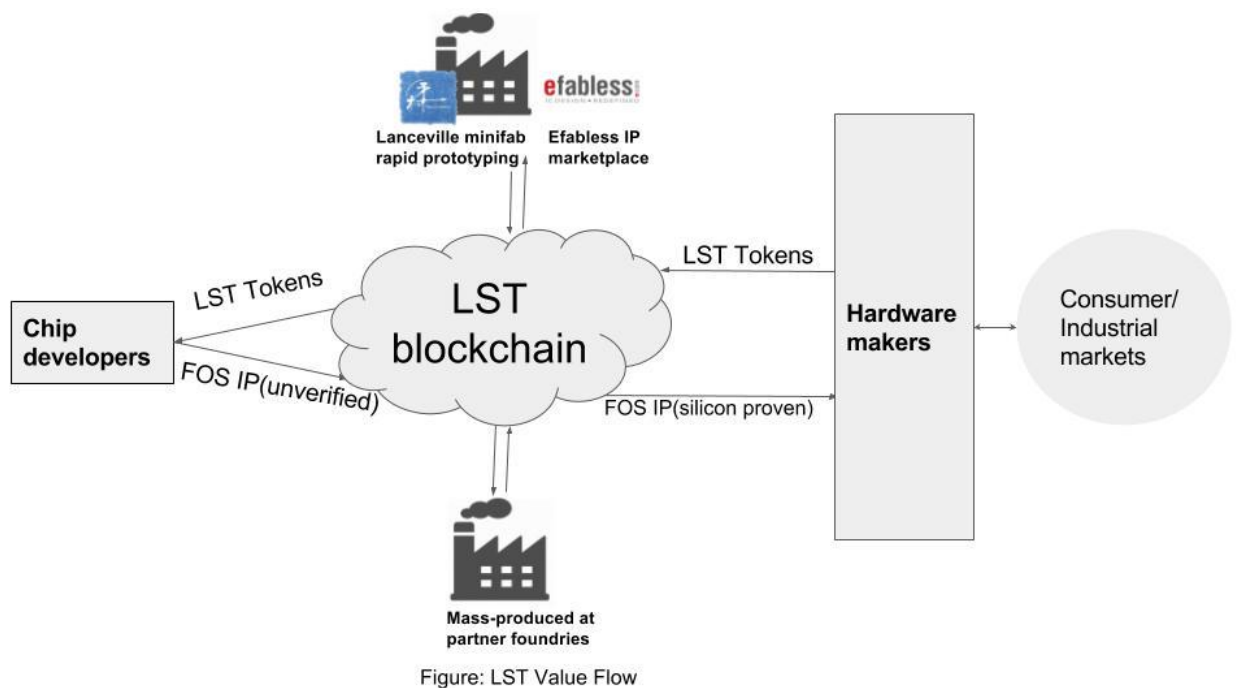
¹³ The world's largest open source software community. <https://github.com/>

¹⁴ The world's largest community for development of hardware IP cores as open source. <https://opencores.org>

2 How we solve the problem

We provide solutions to the above major obstacles restricting commercialization of open source chip.

2.1 A blockchain-based IP transaction network



Open-Source-Communities-Friendly LST Network

The network combines the openness of the open-source communities with the decentralization, transparency and security of blockchain technology to establish trust for chip IP transactions.

2.1.1 Libre Silicon Token("LST") & Smart Contracts

We propose the LST as a token of exchange in the blockchain system, a tamper-proof ledger of permanently-recorded transaction, among participants of the the LST network, enabling a faster, safer way to sell or buy chip IPs or related prototyping services.

The LST is one of the very first ERC20 smart-contracts-based tokens which represent physical goods and the very first which accesses physical chip products and related chip design and test production services at LST network.

The system lets participants set personal preferences for the distribution of the intellectual property they developed. One developer might decide to sell all IPs for maximum profit, for example, while another could choose to donate a portion to the open-source communities. These parameters will then be used to initialize a smart contract based on a basic contract class. This new smart contract contains the hash

of the new design IP and the desired return value. The value will be shown also on the catalog for IPs on the webpage of eFabless¹⁵, our design house partner, when hardware makers, for example, choosing IP blocks there.

2.1.2 Providing sustainable incentives for FOS IP developers

By contributing a certain amount of IP blocks, microchip engineers can earn a certain amount of LST of which each represents the right to prototype a certain fixed amount of silicon chips. The developers then can sell the tokens to hardware makers who need silicon proven chips to be integrated in their products, or pay the tokens to test produce the IP in the Lanceville minifab.

When using up the right the developers or hardware makers give back the tokens to Lanceville which then in turn makes the token available over the LST network to give out again in return for additional community contribution.

Technically, the IP payment process is linked to a smart contract which will be executed that cryptocurrencies be transferred from the wallet of a hardware maker to the wallet of the engineer who designed the IP block.

For each IP that is silicon proven and to be used in commercial products, the smart contract will help the hardware maker to give a fair share of profit in LST tokens to every engineer involved into the design parts. Thus, the LST network encourages more and more talented chip developers and startups worldwide to join the open-source hardware development movement.

2.1.3 Bug bounty program

After reporting a bug on the bug tracker for the relevant IP block, it will be peer reviewed by multiple other engineers. When the bug has been confirmed and fixed by the open source community or even better by the reporter. Everyone involved will get LST tokens as a fair financial reward for the engineering effort.

2.2 An instant prototyping services on demand

As part of the effort to address current “pain-point” related to entry hurdles for fabless startups, Lanceville minifab introduces the direct imaging process which utilizes Electron Beam Lithography (E-Beam) in test production stage.

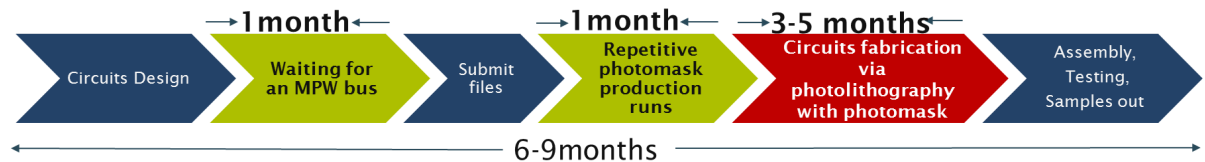
Derived from the early scanning electron microscopes, the E-Beam technique in brief consists of scanning a beam of electrons across a surface covered with a resist film sensitive to those electrons, thus depositing energy in the desired pattern in the resist film. The main attributes of the technology are:

- It is capable of very high resolution, down to 20nm.
- It is a flexible technique that can work with a variety of materials for various customized chips.

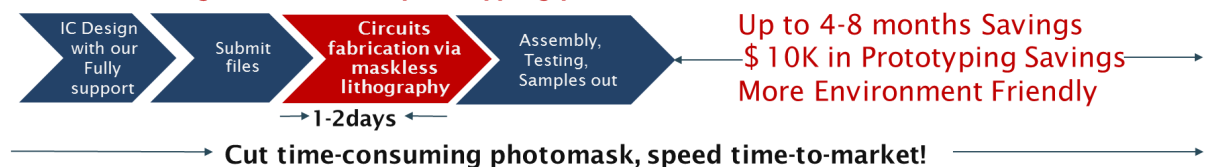
¹⁵ https://marketplace.efabless.com/ip_catalog

- No longer required traditional costly lithographic mask¹⁶ in patterning process.
- The layout of the chips wiring design can be revised almost immediately.
- No burden of minimum quantity so as to leverage the cost of the mask.

Traditional prototyping, with molds developed first:



Our 3D-Printing like maskless prototyping process:



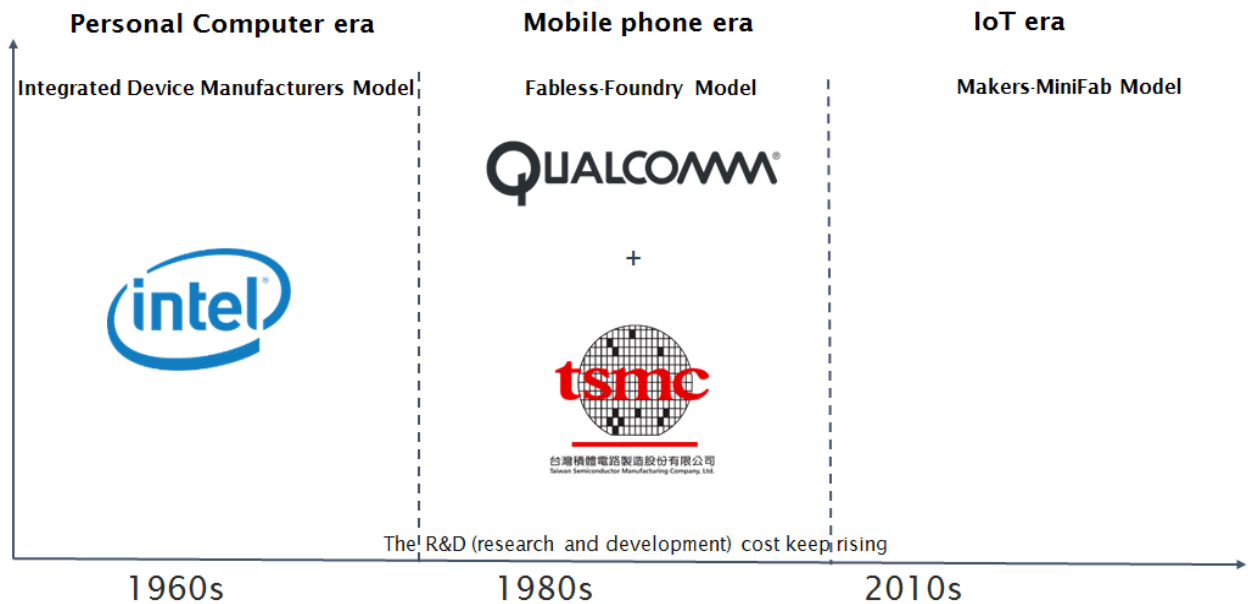
Break the mold, or “photomask”, of traditional prototyping

Traditional prototyping service for a fabless is like “a tour bus”, for which you gotta wait for all other passengers to get on, then go together. Our minifab prototyping service on-demand is like “an Uber”, which is instantly available as you ordered, with one-to-one ‘driver’ (engineering service).

However the E-Beam technique focusing process development case by case is not suitable for mass production. Since for a pure-play fab, it is profitable only when used at full capacity. That’s why mature big fabless is favored by current foundries. It’s time for a maker-communities-friendly minifab.

¹⁶ While a photomask as a mold is indispensable and offers the benefit of economies of scale for mass production, it’s costly for low volume test production, provided that a typical IC wafer is involved 10-25 pieces of expensive mask. So we create a 3D-Printing like maskless process to address this pain point in prototype stage.

A third business model facing IoT revolution



(Integrated Device Manufacturers are involved in both designing and manufacturing)

For more detail of Lanceville semiconductor manufacturing technologies, please go check the Appendix.

2.3 Value-added chip design services

Backed by open-source community projects¹⁷, including Open Circuit Design and Yosys, we are dedicated to develop and maintain QtFlow¹⁸, a free and open source Electronic Design Automation (EDA) tool, as a free alternative to existing costly EDA tools in collaboration with PCONAS GmbH, a German software development company. QtFlow will provide our targeted customers easy access to chip manufacturing and publishing.

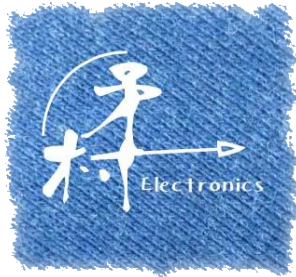
Besides, we cooperate closely with Efabless, an American chip design solution provider, to assist R&D for fabless startups or any other chip designers before and at the test production stage.

¹⁷ For details, please go check section 3.3 of this paper.

¹⁸ <https://github.com/foshardware/qtflow>.

3 Team members and Partners

3.1 Team members of Lanceville MiniFab



Lanceville is headquartered in Hong Kong. We started out as the initial initiator of the Libre Silicon Alliance, aims to build an open source chip prototyping facility, making use of already existing infrastructure available in Hong Kong. Here's the key team members.

Prof. Dr. Junho Lee



- With more than 30 years' experience in Semicon industry, Dr Lee is competent to oversee the whole wafer fabricating process, from pre-treatment, patterning, to interconnection formation and assembly.
- Former General Manager of chip group in Samsung, South Korea.
- The University of Alabama in Huntsville, PhD, Materials Science. Former professor of Changwon National University, South Korea.
- Former NASA scientist, participated in Atlantis Space Shuttle Mission in USA.

Dr. Danny Cheung



- With more than ten years' experience in Semiconductor \Chemical industry, Dr Cheung's extensive exposure to photo-active material application in the electronic industry is another outstanding competitive edge from our team. The application of photo and electron-beam based patterning technology is a vital part to delivery our approach.
- The University of Hong Kong, PhD in Organometallic Chemistry. Author of *Syntheses and Luminescence Studies of Di- and Polynuclear Gold(1) and Copper(1) Complexes*, *Design Strategies Towards Metalloreceptors and Mixed-metal Complexes*
- Former senior expert of Rohm & Haas Electronic (a Fortune 500).

David Lanzendörfer



- Involved passionately into Linux kernel, RepRap and open-source chip design projects.
- Developing open-source chips and QtFlow EDA tool set.
- Studied electrical engineering at universities of ETH Zurich and ZHAW including semiconductor and solid state physics.
- Cofounder of LanceVille technologies

Andy Kong



- FPGA and robotics senior engineer.
- Winner of IEEE international robotic competitions.
- Founder of Hong Kong Maker Faire.
- Speaker of 2016 TED Talk in Hong Kong.
- The University of British Columbia, Electrical and Computer Engineering.

Victor Lee



- In a fully automatic processing line, the control and coordination of individual equipment and instrumentation is one of critical factors that ensure good productivity. This complicated task can be achieved by Victor who is specialized in system engineering and process control.
- Graduated from Hong Kong Polytechnic University.
- Master of Engineering from University of Technology, Sydney
- Surface finishing process engineer (over 10 years)
- Designer of Smart manufacturing process (Industry 4.0)

Andreas Westerwick



- Application developer from PCONAS GmbH, Germany, works on a QtFlow EDA tool together with Lanceville.
- Developing open source EDA with C, Haskell and Qt
- Designing domain-specific languages based on category theory.
- UNIX programmer.

3.2 Partners

3.2.1 efabless, a chip design solutions provider



Member of the Libre Silicon Alliance

Efabless, a fabless located in Silicon Valley in U.S., develops IP blocks and wants to make community designed IC's commercially viable across a wide range of applications.

They have a marketplace where engineers can log in and start using IP blocks of other engineers as well as publishing their own IP blocks if they want to.

The marketplace can be found here https://marketplace.efabless.com/ip_catalog

3.2.2 PCONAS, an open-source software developer



Member of the Libre Silicon Alliance

PCONAS GmbH is a German software development company which has been in business since 1989 and creating database-driven applications and web services for valuable companies worldwide.

At the moment, in partnership with Lanceville, PCONAS helps further develop the QtFlow, a free and open source EDA for ASICs, a value-added service for open-source chip designers.

3.2.3 G,,Coin

G,,Coin is a Hong Kong based crypto exchange, based on Ethereum and BitCoin crypto currency.

They can sell or buy BitCoin and Ethereum in exchange for multiple fiat currencies like for example Hong Kong Dollar.

3.2.3 Bloq

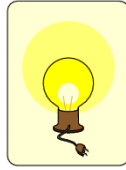


Bloq is a financial cryptography and blockchain technology provider that delivers enterprise grade blockchain technology to leading companies worldwide.

3.3 Key Open-Source community projects

Community projects are open source projects which are not part of a company effort but instead private/personal initiatives of open source developer communities. As a dedicated community-friendly company, Lanceville has been supporting open-source community projects all the time. The following are two key projects we are and will continue supporting, or the projects supporting us.

3.3.1 Open Circuit Design



Open Circuit Design

Open Circuit Design is a project started by [Tim Edwards](#), a former senior staff engineer at the Johns Hopkins University Applied Physics Laboratory. It includes multiple free and open source tools required to design semiconductors.

The project page of Open Circuit Design can be found under the following URL:
<http://opencircuitdesign.com>

Its main task will be to:

- Help developing advanced technology node for the new machines in the Lanceville future Minifab.
- Developing on QRouter and Graywolf which are required tools for the process of placing and routing during the final synthesis step.
- Help develop QtFlow which is ment as a replacement for the mainly script based and difficult to use QFlow which has been done mainly by Tim himself.

3.3.2 Yosys

Yosys Open SYNthesis Suite

Yosys, a framework for Verilog synthesis and formal verification, is a project initiated by [Clifford Wolf](#), who's teaching electronics at University of Applied Arts Vienna, Department of Digital Arts.

The purpose of Yosys is to synthesize Verilog code into the BLIF format from which it then can be further used with GrayWolf and QRouter after being converted into the DEF file format.

The project page of Yosys can be found under the following URL:
<http://www.clifford.at/yosys>

3.4 Members of the Advisory Board

To be determined.

4 Value Propositions and Market Prospects

4.1 Value propositions

The block-chain based LST system enables the interested individual to set up and enforce contracts with automatic transaction support, thus it provides a way for engineers to demand a payment for every manufactured piece of silicon making use of their IP block they publish on the marketplace. For example, the system allows a personalized ARM-like¹⁹ license scheme, in the sense that an engineer can make money just by “selling out licenses”, which means in this context to trust the execution of the license to a smart contract which will be automatically executed every time one of his/her IP blocks is being put into commercialized silicon. Specifically, the LST system provides:

4.1.1 Contributors

- Including chip developers and those who discover and report bugs
- Non-repudiation IP ownership
- Accessible prototyping services
- A bridge to the market and a way to start up fabless business
- A share of tokens

4.1.2 Hardware makers

- Global open-source chip solutions without vicious backdoor concern
- Rapid prototyping services on-demand
- Less expensive continual maintenance services
- Time-to-market advantages
- Access to global chip talents

4.1.3 Education institute

By offering an inexpensive and quick solution for manufacturing low volume of semiconductors it's perfectly suited for educational purposes as well. Scholars could be given the opportunity in grade school to design their own semiconductor if they wish so.

Development contest of chips/devices design can also be set up for young talents (future entrepreneurs) as well. It will offer a pathway to the industry and allow them to contribute their efforts to the community.

¹⁹ British company ARM Holdings develops the architecture and licenses it to other companies. It's the largest chip IP vendor. https://en.wikipedia.org/wiki/ARM_architecture

4.2 Simple, secure open-source hardware development

There are several successful stories in Hardware open source, and that limits to Consumer system hardware, Enterprise system hardware and Circuit boards and there is yet to be reached in the field of Semiconductor level for Backend Design and Fabrication, especially for physical hard cores of a SoC and FPGA design.

Hardware Stack Layers:	Examples:
(3a) Consumer System Hardware	Novena, GoPro, Fetch Robotics, Fitbit, Pebble Watch
(3b) Enterprise System Hardware	Open Compute Project Open Power
(2) Circuit Boards	TinyCircuits, Arduino
(1) Semiconductor Devices (IP, Cores, Tools)	???

Lanceville is also committed to level the playing field for open source hardware development all across the globe, which will encourage students, hobbyists, independent developers, interesting parties, or “makers” to enter into this field which will eventually, support the community of IC industry, lead to wider community participation, low-cost development and quick adoption of new device-level technological breakthrough.

With the high transparency in the semiconductor devices’ design and the IP block, it’s virtually impossible to implant any spying backdoor or alike is being smuggled into a chip design or IP block. For that reason, this LST platform will allow to design trustworthy microchips which can be verified by a global community, unlike several instances of commercial chip families which have had recent disclosures of potential backdoors.

4.3 Market prospects of open-source hardware

Michael Cooney of Network World²⁰ describes the state of open-source hardware today as roughly where open-source software was during the mid-1990s – waiting for commercial suppliers to provide higher levels of support. “What made open-source software acceptable for many businesses was the arrival of support for it, such as Red Hat²¹,” he says, adding, “Something similar may take place with the hardware.” That what we are doing for.

²⁰<http://www.networkworld.com/article/2990138/security/gartner-risk-relentless-data-center-demand-opensource-and-other-tech-trends-it-needs-to-know.html>.

²¹Red Hat: the First \$2 Billion Revenue Open Source Software Solutions Provider.

Statistics²² that reveal the size and scope of our target market:

There are currently 2192 hackerspaces worldwide, 1358 of them are marked as active and 351 as planned.

In 2017, over 190 “Mini Maker Faires” plus over 30 Featured Maker Faires will have taken place around the world.

There are 1362 fabless in Mainland China in 2016.

There are 279'423 users registered in Opencores, the open-source hardware IP community.

There are 135 million adult Makers in the United States, according to the Atmel Corporation.

Millions Arduinos, an open-source platform for developing microcontroller-based prototypes have been sold so far.

5 Estimated Roadmap

On the top of using free and open source based technology, the deployment of our proposed value-chain will also require capital inputs for manufacturing equipment as well as the block chain service provided by commercial companies mentioned above.

The required infrastructure for running this initiative successfully is listed below in subchapters.

5.1 Roadmap of token sale

5.1.1 Token presale

We will organize a Token presale in which buyers are given a chance to buy the LST for a reduced price before the general public. The discount will be between 10% up to 25%.

5.1.2 Token sale

With the financial capital raised from the Token sale we will be able to rent an actual laboratory office in which in a later phase the manufacturing and test equipment is supposed to go.

Also the benefits from the Toke sale will allow Lanceville and other companies to pay its employees a reasonable salary and to hire more employees like additional engineers and UX designers. Of course all of the development steps will be documented on our official website and social media, because of the nature of the used finances.

²² Source: collected by Lanceville.

5.1.3 Setup phase 1

In this phase all the required renovation of the factory building is being finalized, and the clean room prepared for receiving the manufacturing equipment later on.

Also in this phase more engineers will be hired as well as UX designers and other staff required for the overall operation of the company.

5.1.4 Token release phase

In this phase we will just release the rest of the tokens over a certain time period, until we have enough crypto currency cashed in for buying all the machines we need to actually manufacture the promised microchips

5.1.5 Setup phase 2

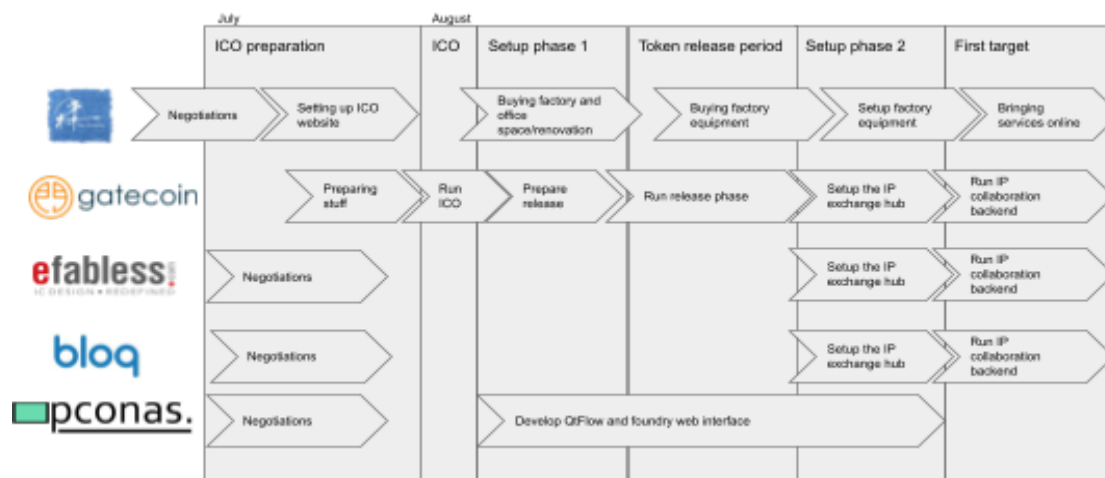
Here we actually set up all the machines we have bought during the token release phase, make sure that the output is actually micro chips, and that the whole process from submitting a design file to an actual semiconductor in the mail of the customer actually works smoothly.

Also we'll work closely with our partners over here for a few months in order to get the 28nm node working properly and so on.

5.1.6 First target

That's the goal. We start actually making microchips on demand with free and open source IP libs and tools. What counts for open-source developers is the quality of our provided service and getting paid for doing the one job he or she is good at: Making Application-specific integrated circuits(ASICs).

5.2 Roadmap of open-source chip solutions



5.2.1 Electron beam (E-beam) machine

The electron beam machine is the core equipment for leading the whole project to success, by eliminating the need for the time consuming and expensive process of manufacturing photolithographic masks for every single MPW shuttle run.

Instead the electron beam machine will allow us to individually and totally flexibly cluster individual prototype designs next to each other on the fly, shoving them through the rest of the normal manufacturing process and being able to ship a prototype after a few days for a fraction of the usual MPW costs required.

The main target of our endeavors is to setup up a E-beam based rapid prototyping facility for semiconductor chip making. The facility will include some typical small scale wafer making processes and our major focus of the patterning technology. However, such a machine usually costs around 5 million USD or more and require competent personnel to operate.

5.2.2 Additional chip manufacturing equipment

For the rest of the setup we will rely on the usual depositing, etching and infusion equipment, commonly used within the semiconductor industry, since only the exposure is usually the showstopper when trying to time and cost efficiently tape out a prototype for customers.

5.2.3 Server space from GateCoin

GateCoin wants 10% share on our cryptocurrency revenue done over their infrastructure.

5.2.4 BLOQ

Bloq will provide (internally or through partners) marketing and Token sale smart-contract design services for XX% of 10 million LST ISO sale.

Additional????, for XX LST per month: Needs review

Sponsors engineer(s) to develop a version of the q3ube open-hardware system specification that will run Bloq-Router with the following:

- Debian Free software guidelines source code for software, firmware, silicon layout designs, and design software that produces silicon layouts
- optional open-source hardware blockchain proof-of-work mining chip for SHA-256, SHA-3, Scrypt, and Ethereum proof-of-work (Dagger-Hashimoto)
- Bit-for-bit and transistor-for-transistor reproducible from source system that comes pre-installed with software to modify any system component and recompile, or create design files for circuit boards, silicon, and CNC machined and/or 3-d printed components

6 Token Launch

6.1 Token launch Summary

Our goal is to raise a minimum of \$20 million USD for the factory equipment as well additional money for offices and employees (additional \$5 million USD).

Based on the volatility of the market, both fiat to crypto currency and cryptocurrency to LST, it is very difficult to predict the maximum capital possible to be raised through the token sales.

Some of the numbers may change with ETH/USD exchange rates and volatility, but the following numbers are best estimates as of July 8, 2017. (to be discussed)

Maximum financing: 100 million ETH -this WILL change with exchange rates.

Minimum financing: 500'000 ETH.

Exchange rate: 1 ETH = 1 LST -this may change with ETH exchange rates.

(Good estimate is 1 ETH is around 210 USD)

Token contract address: TBD (Published through various channels 48hrs before crowdsale launch date).

Launch date and time: TBD

Token launch time-frame: TBD.

Token launch completion: Token launch will end when either the maximum number of ETH are raised or block number XXX is reached. If less than the minimum ETH are raised, ETH can be retrieved by holders of LST.

6.2 Strategic calculation

6.2.1 Toke sale

Since LanceVille technologies receives 79% of the token sale run (10% of all tokens) the equation for the best case scenario is seen below:

$$0.1 \cdot 10^8 \cdot 0.79 \cdot 0.9 = 711 \cdot 10^4 = 7'110'000$$

As can be seen, it is possible that the return of the Toke sale results in a little bit more than 7 million USD or above.

eFabless receives 6% of the pre-sale run (10% of all tokens). The equation for the best case scenario is seen below:

$$0.1 \cdot 10^8 \cdot 0.06 \cdot 0.9 = 54 \cdot 10^4 = 540'000$$

As can be seen, it is possible that the return of the Toke sale results in 540 thousand USD, nearly a million USD or above.

Open Circuit Design receives 5% of the pre-sale run (10% of all tokens). The equation for the best case scenario is seen below:

$$0.1 \cdot 10^8 \cdot 0.05 \cdot 0.9 = 45 \cdot 10^4 = 450'000$$

As can be seen, it is possible that the return of the Toke sale results in 450 thousand USD, nearly a million USD or above.

GateCoin receives 10% of the pre-sale run (10% of all tokens). The equation for the best case scenario is seen below:

$$0.1 \cdot 10^8 \cdot 0.1 \cdot 0.9 = 9 \cdot 10^5 = 900'000$$

As can be seen, it is possible that the return of the Toke sale results in 900 thousand USD, nearly a million USD or above.

6.2.2 Token release

Since LanceVille technologies receives 79% of the Toke sale run (65% of all tokens) the equation for the average case scenario is seen below:

$$0.65 \cdot 10^8 \cdot 0.79 \cdot 0.9 = 46'215 \cdot 10^3 = 46'215'000$$

As can be seen, it is possible that the return of the Toke sale results in around 64 million USD or above.

eFabless receives 6% of the Toke sale run (65% of all tokens). The equation for the average case scenario is seen below:

$$0.65 \cdot 10^8 \cdot 0.06 \cdot 0.9 = 351 \cdot 10^4 = 3'510'000$$

As can be seen, it is possible that the return of the Toke sale results in nearly 5 million USD or above.

Open Circuit Design receives 5% of the Toke sale run (65% of all tokens). The equation for the average case scenario is seen below:

$$0.65 \cdot 10^8 \cdot 0.05 \cdot 0.9 = 405 \cdot 10^4 = 2'925'000$$

As can be seen, it is possible that the return of the Toke sale results in around 4 million USD or above.

GateCoin receives 10% of the Toke sale run (65% of all tokens). The equation for the average case scenario is seen below:

$$0.65 \cdot 10^8 \cdot 0.1 \cdot 0.9 = 585 \cdot 10^4 = 5'850'000$$

As can be seen, it is possible that the return of the Toke sale results in around 8 million USD or above.

By stretching the overall sale over 13 months, the factory equipment can most likely be financed within 4 months. A 13 month release period with a sale of 5 million tokens every month is the best practice based on the suggestions from Vitalik Buterin within his analysis of past token sales:

<http://vitalik.ca/general/2017/06/09/sales.html>

6.3 Token Distribution: 100 million LST available

Toke launch sale: 10% of max; 10 million LST.

Lanceville & Efabless: 10% of max; 10 million LST.

Contributor incentive pool: 25% of max 25 million LST.

Token available to public over 13 month sale period: 54% of max 54 million LST (corresponding to the Hong Kong dollars raised at token launch).

6.4 Contributor incentive Pool

Contributor award fund is used to incentivize developers to participate in the LST ecosystem.

6.5 Budget Allocation

LST Team: 7 million USD

Administration:

Marketing:

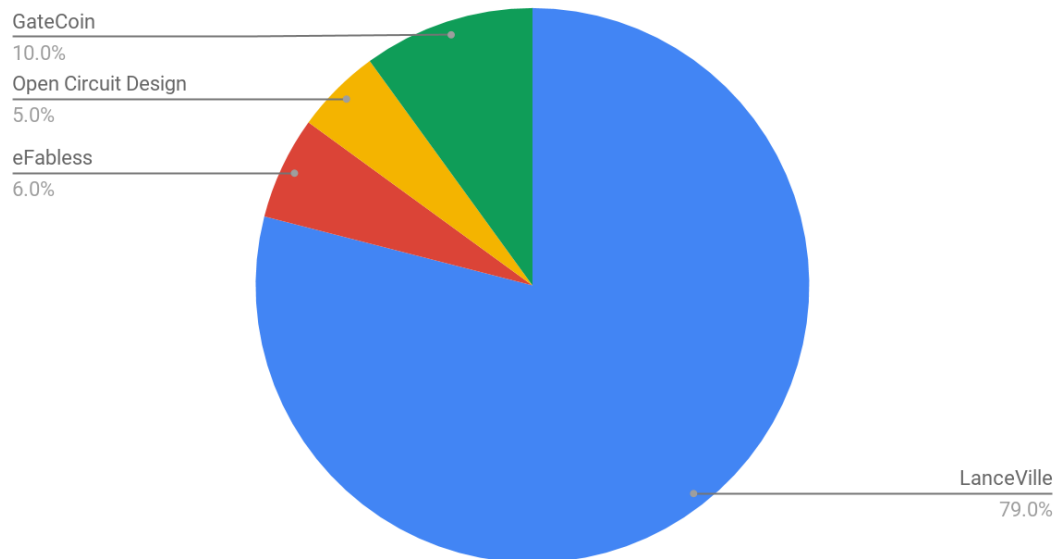
Contractors:

Contingency:

Infrastructure: 30 million USD

Below there can be seen the distribution of financial return to all of the involved partners in a pie diagram.

Token share



The pre-sale will offer 10% of the overall 100 million tokens at a floor price of 0.9 USD each, the rest of the 90% will be continuously released into the market over a time period of N months.

7 LST FAQs

Is it meant to be used as a new cryptocurrency?

No.

It's a standard ERC20 Ethereum standard contract, which will only represent a certain silicon area as soon as we reach the final phase.

These chips can all be identical or variate from each other.

What counts is the amount of orderable chips, a single LST ensures.

8 Appendix: Overview of fabricating technology by Lanceville minifab

9.1 Targeting fabricating technology

Currently, the industrial standard with scale for Lithographic step is using UV source and artwork to produce a position image onto a photomask which have both the limitation of low yield, high cost and limited in the resolutions. The UV source is not stable overtime and will give uncertainty to the manufacturing process. The artwork is expensive, needs time to prepare, easy to damage, subject to contamination and will deform upon usage or storage.

The utilization of E-Beam technology by Lanceville is comparatively new and not heard in the mass manufacturing level, which utilize an electron gun to shoot out electron beam on the wafer and make a positive image. It is actual, software-controlled and the image produced is stable over time.

Electron Beam Lithography is a specialized technique for creating extremely fine patterns (~ 28 nm). Derived from the early scanning electron microscopes, the technique in brief consists of scanning a beam of electrons across a surface covered with a resist film sensitive to those electrons, thus depositing energy in the desired pattern in the resist film. The main attributes of the technology are:

- 1) it is capable of very high resolution;
- 2) it is a flexible technique that can work with a variety of materials;

The basic idea behind electron beam lithography is identical to optical or any other lithography. The substrate is coated with a thin layer of resist (in analogy with photoresist we use the word e resist), which is chemically changed under exposure to the electron beam (Fig 2.1), so that the exposed (non-exposed) areas can be dissolved in a specific solvent (positive (negative) lithography). This process is called development (in analogy with development of photographic films) (Fig 2.2).

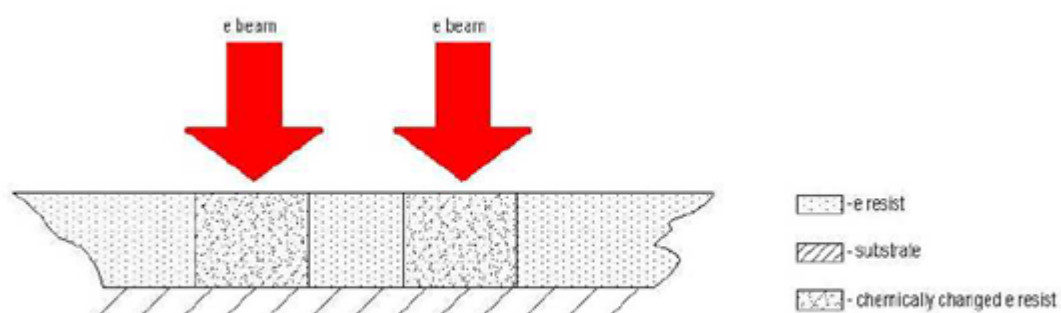


Figure 2.1 E resist crosssection: The electron beam causes chemical changes in the exposed areas

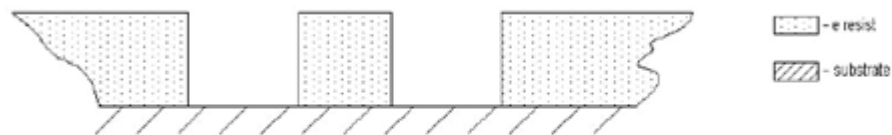


Figure 2.2 E resist crosssection: Only the chemically changed e resist can be dissolved in a specific solvent (positive lithography)

After the removal of the exposed resist a thin metallic layer is deposited on the substrate. On the areas exposed to the electron beam the deposited metal sticks to the substrate, while on the unexposed areas the metal sticks to the resist surface (Fig. 2.3).

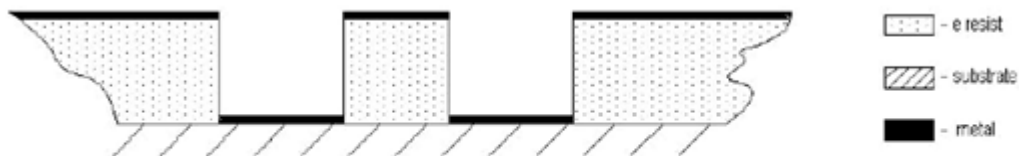


Figure 2.3 E resist crosssection after metal deposition

After metal deposition the remaining (unexposed) e resist is dissolved in an aggressive solvent (lift off). The metal sticking to the resist loses “footing” and so only the metal sticking to the substrate remains. (Fig 2.4)



Figure 2.4 Circuit crosssection: Final result

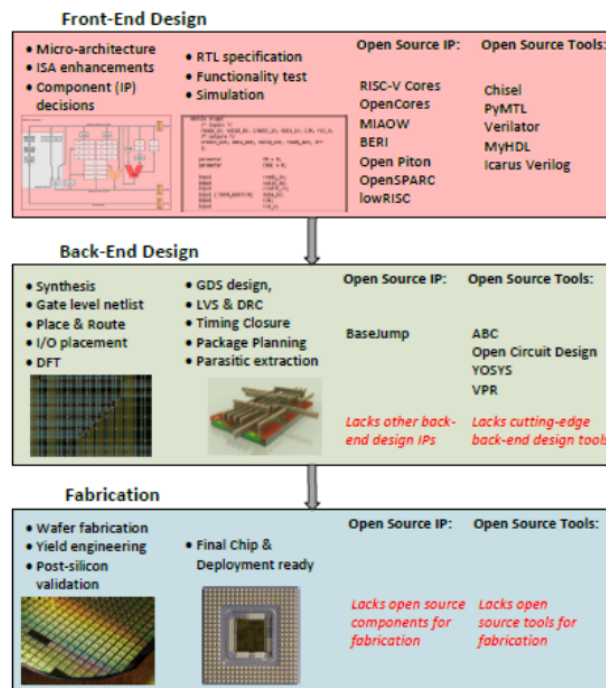
The EBeam is based on Scanning Electron Microscope (SEM); the image is formed in a SEM microscope by scanning an electron beam across a sample and collecting some signal from the beam-sample interaction, which is used to control the intensity of the spot on a television monitor that is scanning in synchronization with the beam on the sample. To convert a standard SEM microscope into a basic electron beam lithography writer, only one modification is absolutely necessary, that is to change the signal feed to the scanning coils (which guide the beam over the sample surface) so that instead of “drawing” a square (like a CRT) the coils will guide the beam to draw an arbitrary pattern.

Our roadmap of manufacturing development is divided into 3 phases; all are surrounding the utilizing of the E-Beam technology:

- Phrase 1. To utilization the E-Beam technology level from laboratory scale, to pilot scale and eventually to manufacturing scale and the target line is 35 nm,
- Phrase 2. To lower the resolution or line to 28 nm for manufacturing scale
- Phrase 3. To lower the line width further for laboratory scale.

9.2 Open source silicon chip

Open source “Designing chips is complex and follows three broad steps as outlined in Figure 2.5 : front-end design, back-end design, and fabrication. An array of EDA (Electronic Design Automation) tools are used at each step. During front-end design, a solution is architected and is implemented, typically in RTL (Register Transfer Logic). The design may incorporate pre-existing components like memory and bus controllers. Some components, e.g, SRAMs and I/O pads, may only be behaviorally modeled in RTL. Once developed, the RTL is extensively tested and verified. Verification often dominates the effort and cost of front-end design. Back-end design transforms the RTL into a physical design. The RTL is first synthesized into a gate-level netlist. Physical counterparts of components that were only modeled in RTL, e.g., the SRAMs and I/O pads, are incorporated in the netlist. The netlist is made testable. Then the gates are physically placed and wires connecting them are laid out. The physical design must adhere to strict design guidelines to ensure integrity and manufacturability. Hence, the physical design is also verified at different stages by performing timing, thermal, power, EM/IR (Electromigration and Voltage drop), ESD (Electrostatic Discharge), parasitic, test vector, LVS (Layout vs Schematic), and DRC (Design Rule Checking) analysis. Complex components, e.g., processor cores and SRAMs, also referred to as IP (intellectual property), are typically designed by experts and reused. In the final, fabrication step, masks are made from the physical design in the form of GDSII (Graphical Database System II) and the design is fabricated on silicon wafers. The silicon wafer is cut into die pieces and tested. Functional die is packaged and tested again, before being shipped. Specialized EDA tools are needed in each step. For example, simulators are needed to verify the RTL, synthesis tools to generate the netlist, and place-and-route tools to place and lay out the design. Physical design verification tools are needed to check the design’s integrity. Fabrication and packaging are highly specialized processes, often performed by experts other than the designers.



(Fig 2.5)

9.3 How we improve the existing technology

Although electron beam lithography tools are capable of forming extremely fine probes, things become more complex when the electrons hit the workpiece. As the electrons penetrate the resist, they experience many small angle scattering events (forward scattering), which tend to broaden the initial beam diameter. As the electrons penetrate through the resist into the substrate, many of them will experience large angle scattering events (backscattering). The backscattered electrons cause the proximity effect, where the dose that a pattern feature receives is affected by electrons scattering from other features nearby. During this process the electrons are continuously slowing down, producing a cascade of low energy electrons called secondary electrons with energies from 2 to 50 eV. They are responsible for the bulk of the actual resist exposure process. Since their range in resist is only a few nanometers, they contribute little to the proximity effect. Instead the net result can be considered to be an effective widening of the beam diameter by roughly 10nm. This largely accounts for the minimum practical resolution of 20 nm observed in the highest resolution electron beam systems. In basic SEM conversion systems the proximity effect caused by the backscattered electrons limits the resolution, to some 100 nm. This resolution level can be increased using some sort of dose correction method. The main effect of proximity effect is that small features are exposed less than the larger features, which causes significant distortion in very small features (that is also the reason why the exposition rate may depend on pattern geometry and size). The simplest dose correction method is simply the use of double layer e-resist, but this only works for quite large features

(~1 μ). The other dose correction methods usually consist of calculating the cumulative exposition rate that a feature receives directly from the beam and also from other features, and then compensating for the excess dose by adapting the beam current (from feature to feature), the speed with which the beam scans over the sample, or the shape of the drawn features.

9 References

- [1] U.S.SECURITIES AND EXCHANGE COMMISSION. *Report of Investigation Pursuant to Section 21(a) of the Securities Exchange Act of 1934-The DAO*. <https://www.sec.gov/litigation/investreport/34-81207.pdf>, 2017
- [2] Abhijit Mahindroo, Nick Santhanam, Bob Sternfels. *Trend spotting Qualcomm executives consider the next wave of growth in semiconductors*. McKinsey on Semiconductors, 2014.
- [3] Peter Van Valkenburgh. *Framework for Securities Regulation of Cryptocurrencies*. <https://coincenter.org/entry/framework-for-securities-regulation-of-cryptocurrencies>, 2016.
- [4] William Mougayar. *Best Practices in Transparency and Reporting for Cryptocurrency Crowdsales*. <http://startupmanagement.org/2015/02/15/best-practices-in-transparency-and-reporting-for-cryptocurrency-crowdsales/>, 2015.

- [5] Satoshi Nakamoto. *Bitcoin: A peer-to-peer electronic cash system*. <https://bitcoin.org/bitcoin.pdf>, 2008.
- [6] Vitalik Buterin. *Ethereum: A next-generation smart contract and decentralized application platform*. <https://github.com/ethereum/wiki/wiki/White-Paper>, 2013.
- [7] An initiative of Coinbase, Coin Center, Union Square Ventures and Consensys. *A Securities Law Framework for Blockchain Tokens*. <https://www.coinbase.com/legal/securities-law-framework.pdf>, 2016.
- [8] McKinsey & Company. *McKinsey on Semiconductors*, Winter 2015.
- [9] McKinsey & Company. *Industry 4.0: How to navigate digitization of the manufacturing sector*, 2015.
- [10] Abhijit Mahindroo, Nick Santhanam, and Dmitry Skurt. *The potential shake-up in semiconductor manufacturing business models*. McKinsey on Semiconductors, 2013.
- [11] Michaela D. Platzer; John F. Sargent Jr.. *U.S. Semiconductor Manufacturing: Industry Trends, Global Competition, Federal Policy*. Congressional Research Service, 2016.
- [12] AZoNano. *Lithography, Photolithography, Electron Beam Lithography and XRay Lithography – Nano Fabrication Techniques*. Institute of Nanotechnology, 2004.
- [13] Da-Yin Liao. *Automation and Integration in Semiconductor Manufacturing*. Applied Wireless Identifications (AWID) U.S.A., 2010.
- [14] J.H. Oh, et al., *Full Integration of Highly Manufacturable 512Mb PRAM Based on 90nm Technology*. IEDM, 2006.
- [15] Global Asset Protection Services LLC. *SEMICONDUCTOR MANUFACTURING*, 2015.
- [16] Eli Greenbaum. *OPEN SOURCE SEMICONDUCTOR CORE LICENSING*. Harvard Journal of Law & Technology, Volume 25, Number 1 Fall 2011.
- [17] Krste Asanović; David A. Patterson. *Instruction Sets Should Be Free: The Case For RISC-V*. Electrical Engineering and Computer Sciences UC Berkeley, Technical Report No. UCB/EECS-2014-146.
- [18] Global Semiconductor Alliance. *Charting a New Course for Semiconductors*. <http://www.rambus.com/future-of-semiconductors>, 2016.
- [19] "Open collaboration powers everything" • <http://www.linuxfoundation.org/>.
- [20] Demerjian, C. "A long look at how ARM licenses chips: Part 1 of 2," <https://semiaccurate.com/2013/08/07/a-long-look-at-how-arm-licenses-chips/>, 2013.
- [21] *High-level Guidance from Kumar Thangudu*. <https://medium.com/@datarade/criterion-for-high-fidelity-token-sales-1391ff20af20>.
- [22] Goldman Sachs. *Blockchain: The New Technology of Trust*. <http://www.goldmansachs.com/our-thinking/pages/blockchain/index.html>.