Chapter 1 Introduction

Overview

1. The Domino 4DELI2H motherboard is standard baby-sized, fully Personal Computer (PC)/ Advanced Technology (AT) compatible and offers outstanding performance and features.

2. With 64 kilobyte (kB), 128kB or 256kB cache memory on board option, this system board is really a high-speed machine that is well suited for building advanced personal computers or workstations.

3. The 4DELI2H is designed with Hint's CS8001 (4L05F2605) and CS8002 Caesar chipset which are highly integrated, which on their own create a Super Industry Standard Architecture (ISA). In addition, there is a Silicon Integrated Systems (SIS) 85C206 integrated peripheral controller[1] and further external logic (i.e., TTL circuits, external 16-bit data buffer)[2] support, turn this motherboard into a Pragmatic Extended Industry Standard Architecture (P-EISA) system[3].

4. HiNT's P-EISA architecture is unique in its design such that we harness the performance of EISA at cost like that of Industry Standard Architecture (ISA). The P-EISA includes functions found within standard EISA motherboards such as[4]:

   a. Edge triggered (non-sharable) interrupts

   b. ISA (16 data, 24 address) DMA

   c. Full 32 bits for address and data allow bus mastering devices access to the complete range of main memory

   d. Burst mode transfers allowing 33MB a second

5. be scaled from 4 megabyte (MB) to 128MB

6. The 4DELI2H provides options to accommodate the Weitek 4167 Numeric Processor Unit (NPU) also known as Floating Point Unit (FPU) to further enhance system performance.

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[1] http://66.113.161.23/~mR_Slug/chipset/chipsets-v1.00.pl?big=29368,*85C310/320/330%20&1=29352&2=29368#29368
[2] https://groups.google.com/g/comp.sys.ibm.pc.hardware/c/1FbH7-aizTU/m/PPtwUGwV6H4J
[3] https://stason.org/TULARC/pc/pc_hardware_faq/2_43_What_disadvantages_are_there_to_the_HiNT_EISA_chip_set.html
[4] https://groups.google.com/g/comp.os.ms-windows.programmer.win32/c/uDh7RWrEltc

Features

7. Support for Intel 80486SX, 80487SX at 25/ 33 megahertz (MHz), 80486DX at 25/ 33/ 40 MHz and Intel 80486DX2 at 25/ 33 MHz microprocessors can be used on the 4DELI2H.

8. Down-shift master and 32-bit master Direct Memory Access (DMA) capable of bursting to 33MB a second transfer rate.

9. HiNT Caesar Chipset, CS8001 and CS8002, which contain[5]:

   a. Extended Industry Standard Architecture (EISA) specification configuration

   b. Refresh

   c. Extended Non-Maskable Interrupt (NMI) status and controls

   d. EISA bus master and command timeout

   e. Software NMI generation

   f. Direct map cache and write back or write through scheme, up to 256kB

   g. Support Weitek 4167 NPU

   h. Two memory banks on board, supports 4MB up to 128MB memory size, Dynamic Random-Access Memory (DRAM) speed: Fast Page Mode (FPM), 80 nanosecond (ns) or 100ns

   i. Four dedicated 16-bit ISA slots

   j. Three 32-bit EISA slots

   k. One 32-bit Video Electronics Standards Association (VESA)[6] Local Bus (VLB) slot

   l. Real Time Clock (RTC)

   m. Hardware turbo switch

   n. Light Emitting Diode (LED) connections for power and turbo mode

Chapter 2 Installation

RAM Installation

10. Either 1MB, 4MB or 16MB Single In-line Memory Module (SIMM) types can be used on the 4DELI2H motherboard.

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[5] https://groups.google.com/g/comp.os.ms-windows.programmer.win32/c/uDh7RWrEltc

[6] An United States based organisation that defines formats for displays and buses used in computers.

11. The 4DELI2H supports two DRAM banks, Bank 0 and Bank 1, in SIMM sockets on board.

12. With the use of 1MB x 9, 4MB x 9 or 16MB x 9 DRAM modules, 4MB and up to 128MB of local memory can be attained. Please refer to Table 1 for details.

Bank 0	Bank 1	Memory Size (MB)
(4) 1MB x 9	NONE	4
(4) 1MB x 9	(4) 1MB x 9	8
(4) 4MB x 9	NONE	16
(4) 1MB x 9	(4) 4MB x 9	20
(4) 4MB x 9	(4) 1MB x 9	20
(4) 4MB x 9	(4) 4MB x 9	32
(4) 16MB x 9	NONE	64
(4) 16MB x 9	(4) 16MB x9	128

Table 1. RAM Configuration.

13. The corresponding part reference are as below:

a. Bank 0: SIM1, SIM2, SIM3, SIM4 (SIMM SOCKET)

b. Bank 1: SIM5, SIM6, SIM7, SIM8 (SIMM SOCKET)

NPU Installation

14. The 4DELI2H motherboard provides options to accommodate the Weitek 4167, a high performance NPU for the Intel 80486 family of microprocessors.
PGA142
Frequency 25/ 33

Connector Functions

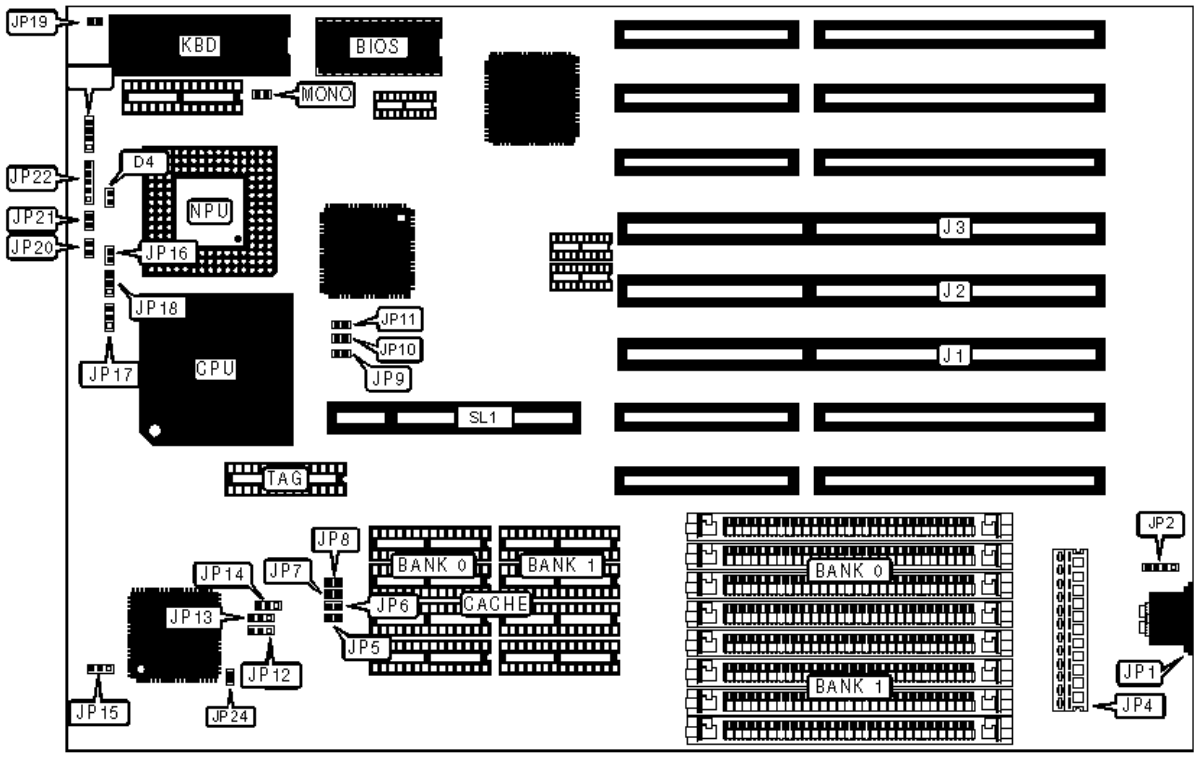

Figure 1. Motherboard Connectors[7].

15. The 3DELI2H provides many functions which can be selected or adjusted by switching some jumpers.

Keyboard Connector (**JP1**)

JP1 is a 'Deutsches Institut für Normung' (DIN) 5, AT keyboard connector, used to connect the keyboard to the rear of the system panel. Please refer to Table 2 and Figure 2 for details.

Jumper	Usage	Pins	Assignment	Note(s)
JP1	DIN Keyboard Connector	1	Keyboard Clock (KBDCLK)	Voltage Common Collector (VCC).
		2	Keyboard Data (KBDTA)	
		3	No Connection (KBRST)	
		4	Ground (GND)	
		5	+5V/ VCC	

Table 2. Keyboard Connector.

[7] Modified version of G486HVL Motherboard Settings and Configuration (stason.org) and Amptron DX-8100C (win3x.org)

AT keyboard connector (DIN5)

Connector Pin #	Purpose
Pin 1	KBDCLK (clock)
Pin 2	KBDAT (data)
Pin 3	KBRST (reset, not used)
Pin 4	GND
Pin 5	VCC (+5V)

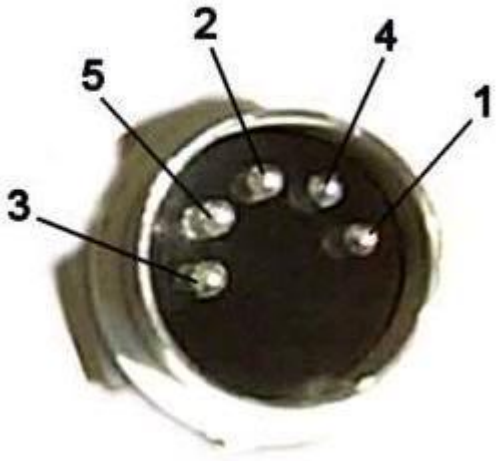

Figure 2. AT Keyboard Connector (DIN5)[8].

16. The following data format is used for keyboard communication, one start bit, eight data bits, one parity bit (odd) and one stop bit. The keyboard reset works via a command string.

External Battery Connector (**JP2**)

17. JP2 uses the external battery when the on-board battery is not being used for operation (JP2 is always open, i.e., without shorting any pin). Pin one shall be used as the positive lead and pin four shall be used as the negative lead. Please refer to Table 3 for details.

Jumper	Usage	Pins	Assignment	Notes
JP2	External Battery	1	Battery +VCC	Pin 1 used as positive lead, pin 4 as negative lead
		2	No Connection	
		3	Ground	
		4	Ground	

Table 3. External Battery Connector.

18. **Note**. To clear the CMOS (including EISA NVRAM) short pins 1 and 4 briefly.

Power Supply Connector (**JP4**)

19. JP4 is used to connect the power supply. It is very important to select a power supply which provides a power good signal. Please refer to Table 4 for details.

Jumpe	Usage	Pin	Assignment	Colour[9]	Note(s)

[8] https://helloacm.com/wp-content/uploads/2014/11/at-keyboard-connector.jpg
[9] Hilman Industries - AT Motherboard Power Cable Pinout

r		s			
JP3	Power Supply Connector	1	Power Good	Orange	
		2	+5V	Red	
		3	+12V	Yellow	
		4	-12V	Blue	
		5	Ground	Black	
		6	Ground	Black	
		7	Ground	Black	
		8	Ground	Black	
		9	-5V	White	
		10	+5V/ VCC	Red	
		11	+5V/ VCC	Red	
		12	+5V/ VCC	Red	

Table 4. Power Supply Connector.

20. Please, Industry standard PC, XT, AT, Baby-AT, and LPX motherboards all use the same type of main power supply connectors. These supplies feature two main power connectors (P8 and P9), each with 6 pins that attach the power supply to the motherboard. All standard PC power supplies that use the P8 and P9 connectors have them installed end to end so that the two black wires (ground connections) on both power cables are next to each other. Some power supplies have them labelled as P1/P2 instead.

21. Because these connectors usually have a clasp that prevents them from being inserted backward on the pins on the motherboards, the major concern is getting the two connectors in the correct orientation side by side and not missing a pin offset on either side. Following the black-to-black rule keeps you safe[10].

22. You must take care, however, to make sure that no remaining unconnected motherboard pins exist between or on either side of the two connectors after you install them. A properly installed connector connects to and covers every motherboard power pin. If any power pins are showing on either side of the connectors, the entire connector assembly is installed incorrectly, which can result in catastrophic failure for the motherboard, including everything plugged into it at the time of power-up. Figure 3 shows the P8 and P9 connectors (sometimes also called P1/P2) in their proper orientations when connecting[11].

[10] Motherboard Power Connectors | PC Repair and Maintenance: In-depth Look at Power Supply | InformIT
[11] Motherboard Power Connectors | PC Repair and Maintenance: In-depth Look at Power Supply | InformIT

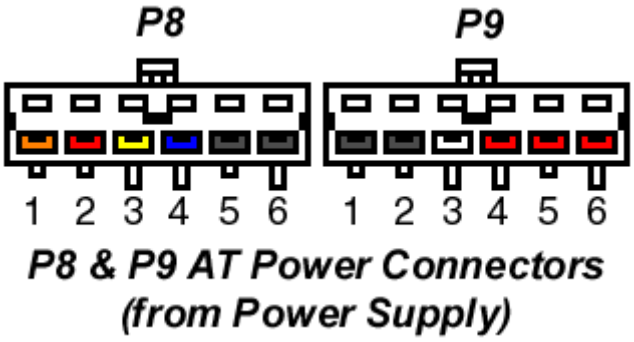

Figure 3. Connector[12].

Cache RAM Size Selection (JP5 ~ JP8 and JP12 ~ 14)

23. JP5 to JP8 and JP12 to JP14 are used to set the cache memory sizes. Table 5 shows the pins should be shorted for different sizes of cache memory.

Size (kB)	JP5	JP6	JP7	JP8	JP12	JP13	JP14
64	Open	Open	Open	Open	1 and 2	1 and 2	1 and 2
128	Closed	Open	Open	Short	2 and 3	2 and 3	1 and 2
256	Short	Short	Short	Short	2 and 3	2 and 3	2 and 3

Table 5. Cache RAM Size Selection.

Cache RAM Configuration

24. The 4DELI2H supports two banks of SRAM provides, 64kB, 128kB or 256kB of cache memory. Please refer to Table 6 for details.

Size (kB)	Bank 0	Bank 1	TAG
64	(4) 8K x 8	(4) 8K x	(1) 8K x 8
128	(4) 32K x 8	None	(1) 32K x 8
256	(4) 32K x 8	(4) 32K x 8	(1) 32K x 8

Table 6. Cache RAM Configuration.

25. The corresponding bank to part reference is as follows:

a. Data RAM Bank 0: U27, U28, U29, U30

b. Data RAM Bank 1: U16, U17, U18, U19

[12] Hilman Industries - AT Motherboard Power Cable Pinout

c. TAG RAM: U38

VESA Wait State Configuration (**JP10 and JP11**)

26. Assessed[13]:

Bus Speed	Wait States	JP10	JP11	Note(s)
< 33MHz	0	Open	Open	
> 33MHz	1	Short	Short	

Table 7. VESA Wait State Configuration.

BUS Speed Configuration (**JP15** – **JP18**)

27. JP15 selects the bus speed which can either be 50 or 33 MHz. Please refer to Table 8 for details.

Bus Speed	JP15	Note(s)
50MHz	1 and 2	
33MHz	2 and 3	

Table 8. Bus Speed Configuration.

CPU Configuration (**JP16 ~ JP18**)

28. FF

Type	JP15	JP16	JP17	JP18
80486SX-25/ 33	2 and 3	Open	Open	2 and 3
80487SX-33	2 and 3	Short	2 and 3	1 and 2
80486DX-25/ 33	2 and 3	Short	1 and 2	1 and 2
80486DX-50	1 and 2	Short	1 and 2	1 and 2
80486DX2-25/ 33	2 and 3	Short	1 and 2	1 and 2

Table 9. CPU Configuration.

Reset Switch Connector (**JP20**)

29. JP20 is used to connect the reset switch to restart the system. You may connect the reset switch cable on the case with JP20. Please refer to Table 10 for details.

[13] Amptron DX-8100C (win3x.org)

Jumper	Usage	Pin	Assignment	Note(s)
JP20	Reset Switch Connector	1	Reset Control	
		2	Ground	

Table 10. Reset Switch Connector.

Turbo Switch Connector (**JP21**)

30. JP21 is used to select the system board's system clock. Please refer to Table 11 for details.

Jumper	Usage	Pins	Assignment	Note(s)
JP21	Turbo Switch Connector	1	Pull Up (+5V)	
		2	Turbo Control	

Table 11. Turbo Switch Connector.

Key-lock Connector (**JP22**)

31. JP22 is used to connect the key-lock connector on the front panel of the case. Please refer to Table 12 for details.

Jumper	Usage	Pins	Assignment	Note(s)
JP22	Key-lock to enable/ disable keyboard and Power LED.	1	LED Power	Key-lock is used to enable or disable the keyboard for security use.
		2	No Connection	
		3	Ground	
		4	Keyboard Lock	
		5	Ground	

Table 12. Key-lock Connector.

Speaker Connector ()

32. ?? is used to connect the speaker to the system board. Please refer to Table 13 for details.

Jumper	Usage	Pins	Assignment	Notes(s)
	Speaker Connection	1	Speaker Data	
		2	No Connection	
		3	Ground	
		4	+5V	

Table 13. Speaker Connector.

Colour/ Monochrome Display Selection (**MONO**) – assessed

33. JP32 allows users to choose the type of display card used. Please refer to Table 14 for details.

Jumper	Usage	Pins	Function	Note(s)
JP32	Display Selection	1 - 2 Open	Monochrome	
		1 - 2 Short	Colour	

Table 14. Display Selection.

Turbo LED Connector (**D4**)

34. D4 is used to connect the turbo LED cable of the case. If the system board is in turbo mode, the turbo LED should light. Please refer to Table 15 for details.

Jumper	Usage	Pins	Assignment	Note(s)
D4	Turbo LED Connector	1	Pull UP (+5V)	
		2	Turbo Control	

Table 15. Turbo LED Connector.

Chapter 4 Operation

35. This chapter tells the user how to use the setup for the 4DELI2H motherboard. Please note that any improper use of this setup can cause damage to your system. Therefore, please make sure you understand thoroughly before making any change or you may contact your dealer for more detailed information.

36. This chapter will briefly describe the Basic Input/ Output System (BIOS) written by AMI (American Megatrends Inc.). In the meantime, do not use another BIOS other than the one used on this board as it will cause functional incompatibility.

AMI BIOS Register Setup

37. The setup program is used to configure the system. These system options are stored in the Complementary Metal Oxide Semiconductor (CMOS). If the CMOS is good, the system is configured with the values stored in the CMOS. If the CMOS is bad, the system is configured with the default values stored in the Read Only Memory (ROM) file. There are two sets of BIOS values stored in the ROM file: the BIOS SETUP PROGRAM default values and the Power-On default values.

38. The BIOS SETUP PROGRAM default values are the default values which should provide optimum performance for the system. They are the best-case default values.

39. The Power-On default values, which are the worst-case defaults, are the stable values for the system. They are to be used if the system is performing erratically because of hardware problems.

40. Listed below is an explanation of the keys displayed at the bottom of the screens accessed through the BIOS SETUP PROGRAM:

a. **ESC**. Exit to previous screen

b. **Arrow keys**. Use arrow keys to move the cursor to desired selection.

c. **Pg Up**/ **Pg Dn**/ **Ctrl** + **Pg Up**/ **Ctrl** + **Pg Dn**. Modify the default value of the options for the highlighted feature. If there are less than ten available options, the Ctrl + Pg Up and Ctrl + Pg Dn keys function the same as Pg Up and Pg Dn keys.

d. **F1**. Displays help screen for selected features.

e. **F2**/ **F3**. Change background and foreground colours.

f. **F5**. Retrieves the values which were resident when the current setup session was started. These values will be CMOS values if the CMOS was uncorrupted at the start of the session, or they will be the BIOS SETUP PROGRAM default values.

g. **F6**. Loads all features in the ‘Advanced CMOS Setup’ and ‘Advanced Chipset Setup’ with the BIOS SETUP PROGRAM defaults.

h. **F7**. Loads all features in the ‘Advanced CMOS Setup’ and ‘Advanced Chipset Setup’ with the Power-On defaults.

i. **F10**. Saves all changes made to Setup and exits the program.

41. **Note**. The default value for the prompts which occur when the ‘F5’, ‘F6’ and ‘F7’ are pressed is always ‘N’ (No). Executing these options requires changing the ‘N’ to ‘Y’ (Yes) and pressing ‘ENTER’.

Standard CMOS Setup

42. The ‘Standard CMOS Setup’ utility is used to configure the following features:

a. **Date**. Month, Day and Year. Ranges for each value are listed below in the prompt box in the lower right corner of the CMOS Setup Screen.

b. **Time**. Hour, Minute and Second. Uses 24-hour clock format.

c. **Daylight Savings**. ‘Disabled’ or ‘Enabled’.

d. **Hard Disk C and Hard Disk D**. Hard disk types from 1 to 46 are standard ones; type 47 is user definable. The user must enter the hard disk parameters for each drive. The drive types are identified by the following characteristics:

(1) **Type**. The number designation for a drive with certain identification parameters.

(2) **Cyl**[14]. The number of cylinders found in the specified drive type.

(3) **Heads**. The number of heads found in the specified drive type.

(4) **WPCOM**[15]. The read delay circuitry considers the timing differences between the inner and outer edges of the surface of the disk platter. The number designates the starting cylinder of the signal.

(5) **LZONE**[16]. The Landing Zone of the heads. This number determines the cylinder location where the heads normally park when the system is shutdown.

(6) **Capacity**. The formatted capacity of the drive based on the formula:

$$(of heads)x(of cylinders)x\left(of\frac{sectors}{cylinders}\right)x\left(\frac{512}{sectors}\right)$$

(7) ‘Not Installed’ is available for use as an option. This option could be used for diskless workstations and Small Computer System Interface (SCSI) hard disks. Type 47 may be used for both hard disks C and D. The parameters for type 47 under Hard Disk C and Hard Disk D may be different.

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[14]Cylinders (Cyl).
[15]Write Pre-Compensation (WPCOM).
[16]Landing Zone (LZONE).

(8) Please see table x for further details[17]:

Type	Cylinders	Heads	Sectors	WPCOM	LZONE	Note(s)
1	396	4	17	128	305	
2	615	4	17	300	615	
3	615	6	17	300	615	
4	940	8	17	512	940	
5	940	6	17	512	940	
6	615	4	17	-1	615	
7	462	8	17	256	511	
8	733	5	17	-1	733	
9	900	15	17	-1	901	
10	820	3	17	-1	820	
11	855	5	17	-1	855	
12	855	7	17	-1	855	
13	306	8	17	128	319	
14	733	7	17	-1	733	
15						Reserved
16	612	4	17	0	633	
17	977	5	17	300	977	
18	977	7	17	-1	977	
19	1024	7	17	512	1023	
20	733	5	17	300	732	
21	733	7	17	300	732	
22	733	5	17	300	732	
23	306	4	17	0	336	
24	925	7	17	0	925	
25	925	9	17	-1	925	
26	724	7	17	754	754	
27	754	11	17	-1	754	
28	699	7	17	256	699	
29	823	10	17	-1	823	
30	918	7	17	918	918	

[17]https://www.win.tue.nl/~aeb/linux/hdtypes/hdtypes-3.html

31	1024	11	17	-1	1024	
32	1024	15	17	-1	1024	
33	1024	2	17	1024	1024	
34	612	2	17	128	612	
35	1024	9	17	-1	1024	
36	1024	8	17	512	1024	
37	615	8	17	128	615	
38	987	3	17	987	987	
39	987	7	17	987	987	
40	820	6	17	820	820	
41	977	5	17	977	977	
42	981	5	17	981	981	
43	830	7	17	512	830	
44	830	10	17	-1	830	
45	917	15	17	-1	918	
46	1224	15	17	-1	1223	
47						Not used or user defined.

Table 16. Hard Disk Types

e. **Floppy Drive A and Floppy Drive B**: The options are 360kB 5 1/4", 1.2MB 5 1/4", 720kB 3 1/2", 1.44MB 3 1/2" and Not Installed. Not installed could be used as an option for diskless workstations.

f. **Primary Display**. Options are Monochrome, Colour 40x25, VGA/ PGA/ EGA, Colour 80x25 and Not Installed. Not installed could be used for network file servers.

g. **Keyboard**. Options are installed or not installed.

Advanced CMOS Setup

43. The 'Advanced CMOS Setup' is equipped with a series of help screens. accessed by the F1 key, which will display the options available for a particular configuration feature and special help for some of the options.

44. The following is a short description for each of the options on the 'Advanced CMOS Setup' Screen:

a. **Typematic Rate Programming**. By enabling this option, the user can adjust the rate at which a keystroke is repeated. The options 'Typematic Rate Delay (msec)' and 'Typematic Rate (Chars/sec)' affect this rate. When a key is pressed and held down, the character appears on the screen and after a delay set by the Typematic Rate Delay, it keeps on repeating at a rate set by the Typematic Rate value. When two

or more keys are pressed and held down simultaneously, only the last key pressed will be repeated at the Typematic rate. This stops when the last key pressed is released, even if other keys are depressed.

b. **Typematic Rate Delay** (**msec**). Available options are: 250, 500, 750 and 1000.

c. **Typematic Rate** (**Chars**/**Sec**). Available options are: 30.0, 26.7, 24.0, 21.8, 20.0, 18.5, 17.1, 16.0, etc. until 2.0.

d. **Above 1 MB Memory Test**. This feature, when enabled, will invoke the Power-On Self-Test (POST) memory routines on the Random-Access Memory (RAM) above 1MB (if present on system). If disabled, the BIOS will only check the first 1MB of RAM.

e. **Memory Test Tick Sound**. This option will enable (turn on) or disable (turn off) the 'ticking' sound during the memory test.

f. **Memory Parity Error Check**. If the motherboard does not have parity RAM, the user may disable the memory parity error checking routines in the BIOS.

g. **Hit <DEL> Message Display**. Disabling this option will prevent the message 'Hit <DEL> if you want to run SETUP' from appearing on the screen when the system boots up.

h. **Hard Disk Type 47 RAM Area**. The AMI BIOS SETUP features two user definable hard disk types. Normally, the data for these disk types are stored at 0:300 in lower system RAM. If a problem occurs with other software, this data can be located at the upper limit of the Disk Operating System (DOS) Shell (640kB). If the option is set to 'DOS 1 KB', the DOS Shell is shortened to 639kB, and the top kB is used for the hard disk data storage.

i. **Wait For <F1> If Any Error**. Before the system boots up, the BIOS will execute the POST routines, a series of system diagnostic routines. If any of these tests fail, but a non-fatal error has occurred and the system can still function, the BIOS will respond with an appropriate error message followed by the statement 'Press <F1> to continue'. If this option is disabled, any non-fatal error which occurs will not generate the above statement, but the BIOS will still display the appropriate error message. This will eliminate the need for any user response to a non-fatal error condition message.

j. **System Boot Up Num Lock**. The user may turn off the 'Num Lock' option on their Enhanced Keyboard' when the system is powered on. This will allow them to use the arrow keys on the numeric keypad instead of using the other set of arrow keys on the Enhanced Keyboard. The BIOS will default to turning the 'Num Lock' on.

k. **Weitek Processor**. Available options are Absent or Present.

l. **Floppy Drive Seek At Boot**. The default for this option is 'Disabled' to allow a fast boot and to decrease the possibility of damage to the heads.

m. **System Boot Up Sequence**. The AMI BIOS will normally attempt to boot from floppy drive A (if present) and if unsuccessful, it will attempt to boot from hard disk C.

n. **CPU Frequency**. Auto

o. **System Boot Up CPU**[18] **Speed**. This option can set the microprocessor speed during POST. 'High' means the microprocessor is running at full speed. 'Low' means the microprocessor is running 1/2 of the microprocessor for better reliability.

p. **External Cache Memory**. This option allows the user to specify whether the external cache is enabled of disabled.

q. **Internal Cache Memory**. This option allows users to enable or disabled the internal cache of 80486 microprocessors.

r. **Fast Gate A20 Option**. Enabling the option will optimise the OS/2 environment.

s. **Turbo Switch Function**. This option allows users to enable or disable the turbo switch.

t. **Password Checking Option**. The password feature can be used to prevent from unauthorised system boot up or use of BIOS SETUP PROGRAM. If the 'Always' option is chosen at Setup, each time the system is turned on, the prompt for user password will appear. Default setting is 'Setup'. The password prompt will not appear when the system is turned on but will appear if the user attempts to enter the Setup program. Factory default password is 'AMI'. The program allows three attempts to key in the correct password. After each incorrect attempt, the prompt to enter the current password will appear, followed by an 'X'. After the third incorrect attempt, the system will lock, and it will be necessary to reboot.

u. **Video ROM Shadow C000**, **32K**. Shadow RAM enabled or disabled at each different segment, ReadOnly?

v. **Adaptor ROM Shadow C800 ~ E000**, **32K**. This option enables or disables the Shadow Function of Adaptor's BIOS if there is, such as SCSI Controller.

w. **System ROM Shadow F000**, **64K**: This option enables or disables Shadow Function of SYSTEM BIOS, ReadOnly?

Advanced Chipset Setup

45. This portion of the BIOS SETUP PROGRAM is entirely chipset specific and requires knowledge about the CS8001/ CS8002 chipset in use. This option is used to change the register values for the chipset. These registers control most of the system options. The screen of the Factory Setup Value of 'Advanced Chipset Setup' is shown on the next page. A short description follows for each of the options on the 'Advanced Chipset Setup':

[18] Central Processing Unit (CPU).

a. **AT-BUS Clock Speed**. This option provided the selection of a different Bus Clock which allows users to use the I/O cars with various speeds. Different types and speeds of microprocessors must be set with different AT Bus Clock Speed.

b. **I/O Cmd Recovery Control**. This function will generate long enough I/O command recovery time for slow reacting peripheral cards when 'Enabled'.

c. **Adapt**. **Shadow RAM Cacheable**. This option allows you to select the shadowed address C8000H ~ EFFFFH to be cacheable or not. The option will only affect when Adapter ROM Shadow is Enabled in 'Advanced CMOS Setup'.

d. **Video Shadow RAM Cacheable**. This option allows you to select the shadowed address C0000H ~ C7FFFH to be cacheable or not. The option will only affect when Adapter ROM Shadow is Enabled in 'Advanced CMOS Setup'.

e. **System Shadow RAM Cacheable**. This option allows you to select the shadowed address F0000H ~ FFFFFH to be cacheable or not. The option will only affect when Adapter ROM Shadow is Enabled in 'Advanced CMOS Setup'.

f. **Remapped Memory**. Enabling this option can save up to 256kB usable memory located from 640kB to 1MB (0A000H ~ 0FFFFFH) can be remapped to the top of the on-board memory.

g. **Remapped Memory Cacheable**. 'Yes' option allows saving up to 256kB of unusable memory. The physical memory location can be remapped. If set as 'No', the Shadow function will be disabled automatically.

h. **Block-1 Memory Size**. This option allows the user to select the memory Block-1 Size from 256kB, 512kB, 1MB or 2MB.

i. **Block-1 Memory Base Address**. This option must be a boundary of Block-I Memory Size. Information of options are available when pressing 'F1'.

j. **Block-1 Memory Cacheable**. This option is for Local Memory Access. It must be set as Cacheable ('Yes').

k. **Block-2 Memory Size**. This option allows the user to select the memory Block-1 Size from 256kB, 512kB, 1MB or 2MB.

l. **Block-2 Memory Base Address**. This option must be a boundary of Block-I Memory Size. Information of options are available when pressing 'F1'.

m. **Block-2 Memory Cacheable**. This option is for Local Memory Access. It must be set as Cacheable ('Yes').

n. **Fast Reset Delay**. 2 us or 6 us. The time in microseconds for software reset, between real and protected modes. The lower the figure, the better the performance, but this may affect reliability[19].

o. **Fast Reset & A20 Emulation**. Enabled.

[19] The Bios Companion - Phil Croucher - Google Books

(1) **Gate A20 Emulation**. You have the choice of Keyboard Controller (if disabled) or Chipset, which is faster. This is for programs that use BIOS calls or I/O ports 60/ 64h for A20 operations, where the chipset will intercept those commands and emulate the keyboard controller to allow the generation of the relevant signals. The sequence is to write D1h to port 64h, followed by an I/O write to 60h with 00h. Fast reset is an I/O write to 64h with 1111XXX0b.

(2) Fast means that the A20 gate is controlled by I/O port 92h where programs use BIOS calls. Both means Gate A20 is controlled by the keyboard controller and chipset where programs use I/O port 60/ 64h.

(3) **Fast Reset Emulation**. Enhances the speed of switching in and out of protected mode by delaying certain signals (INIT or CPURST) by a certain time and holding them for 25 CPUCLK. Switching from Protected to Real Mode requires a 'reboot' at chip level and this setting allows the BIOS to reboot your system without having to reinitialise all of the hardware. In fact, a pulse is used to take the microprocessor out of protected mode, which is left set on a fast microprocessor reset, so is detectable by software (in a boot up, a bit is looked for which indicated whether this is a 'boot start' or a return to 8088. If the latter, the contents of the registers are kept). This setting helps solve problems caused by switching in and out of protected mode to fast[20].

p. **1 Clock Delay for Local Bus**. Enabled. Mostly disable this is system running at 33MHz or below, but some VLB devices may need 1 wait state anyway. You may need to enable this (i.e. insert 1 wait state) for 50MHz[21].

q. **386-40mhzPresent en/disable**. Enabled

r. **Cache Scheme**. WR/Back or WR/Thru, there are two concepts of cache handling. The first is the write-back (WR/Back), you work against the cache and when that data is finished it is written back to the primary memory. You should put it as write-back to receive the best performance. The second one is write-through (WR/Thru), that instead of waiting until the work with the data is finished write to primary memory for every change in the cache[22].

s. **486 Cache Mask** (**Size**:**Start**). Disabled. This mask region is used for masking of the microprocessor internal cache memory. Size, the masking size. Start, the starting address to be masked off.

t. **2nd Cache Mask** (**Size**:**Start**). Disabled. This mask region is used for masking off the microprocessors external cache memory. Size, the masking size. Start, the starting address to be masked off.

u. **DRAM Mask Start**. Disabled

v. **START/CMD for ISA DMA**. Disabled.

---

[20] The Bios Companion - Phil Croucher - Google Books
[21] The Bios Companion - Phil Croucher - Google Books
[22] Advanced BIOS Settings (scritub.com)

46. **Note**. The CS8001 has 256kB of shadow RAM, between address range C0000 ~ FFFFF, organised as 4 x32kB and 2 x 64kB[23].

Auto Configuration With BIOS Defaults

47. The Auto Configuration With BIOS feature uses the default system values before the user has changed any CMOS values. If the CMOS is corrupted, the BIOS defaults will automatically be loaded to the 'Advanced CMOS Setup' and 'Advanced Chipset Setup'. These default values will provide the optimum performance for the system.

Auto Configuration With Power-On Defaults

48. This feature uses the default Power-On values. You may wish to use this option as a diagnostic aid if your system is behaving erratically.

Change Password

49. The BIOS SETUP PROGRAM has an optional password feature. The password check function is enabled or disabled in 'Advanced CMOS Setup'. The password check function is enabled by choosing either 'Always' or 'Setup'.

50. The password, which will be stored in the CMOS, cannot exceed six American Standard Code for Information Interchange (ASCII) characters, a default password, to be used if the CMOS is corrupted, is stored in the ROM. The default password is 'AMI'.

51. To change the user password, by using the arrow keys to move the cursor to this selecting and pressing 'ENTER' and follow the request and ask for help by pressing 'F1' when needed.

52. Once Setup is completed and the changed values have been stored in the CMOS, when the system next boots, the user will be prompted for the password if the password function is present and has been enabled.

Write to CMOS And Exit

53. The features selected and configured in the Standard Setup, 'Advanced CMOS Setup', 'Advanced Chipset Setup' and 'Password Setup' will be stored in the CMOS when this option is taken. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the BIOS.

Do Not Write to CMOS And Exit

54. This option passes control back to the BIOS without writing and changes to the CMOS.

---

23 http://webcache.googleusercontent.com/search?q=cache:amLxngtxSakJ:annex.retroarchive.org/cdrom/smsw-vol5/UTILS/TLB_T252/CHIPSET.DOC+&cd=18&hl=en&ct=clnk&gl=uk

Appendix A BIOS Error Beep Codes

55. During the POST routines, which are performed each time the system is powered on, errors may occur.

56. Non-fatal errors are those which, in most cases, allow the system to continue the boot up process. The error messages normally appear on the screen.

57. Fatal errors are those which will not allow the system to continue the boot up procedure. If a fatal error occurs, you should consult with your local dealer for possible repairs.

58. These fatal errors are usually communicated through a series of audible beeps. The number on the fatal error list below corresponds to the number of beeps for the corresponding error. All errors listed, except for number eight, are fatal errors.

# of Beeps	Error Message	Note(s)
1	Refresh Failure. The memory refresh circuitry of the motherboard is faulty.	
2	Parity Error. A parity error was detected in the base memory (the first block of 64kB) of the system.	
3	Base 64kB Memory Failure. A memory failure occurred with the first 64kB of memory.	
4	Timer Not Operational. Timer #1 on the system board has failed to function properly.	
5	Microprocessor Error. The microprocessor on the system board has generated an error.	
6	8042 Gate A20 Failure. The keyboard controller (8042) contains the Gate A20 switch which allows the microprocessor to operate in virtual mode. This error message means that the BIOS in not able to switch the microprocessor into protected mode.	
7	Processor Exception Interrupt Error. The microprocessor on the motherboard has generated an exception interrupt.	
8	Display Memory Read/ Write Error. The system video adapter is either missing or its memory is fault.	Not a fatal error.
9	ROM Checksum Error. The ROM checksum value does not match the value encoded in the BIOS.	
10	CMOS Shutdown Register Read/ Write Error. The shutdown register for the CMOS memory	

	has failed	

Table 17..

Appendix B BIOS Non-Fatal Error Message

59. If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line **2**
Press <F1> to RESUME

60. **Note**. The error message and press the 'F1' to continue with the boot up procedure. Note: If the 'Wait for <F1> If Any Error' option in the 'Advanced CMOS Setup' portion of the BIOS SETUP PROGRAM has been set to 'Disabled', the 'F1' prompt will not appear on the third line.

61. For most of the error messages, there is no 'ERROR Message Line 2'. Generally, for those messages containing a line 2 error message, the text will be 'RUN SETUP UTILITY'. Pressing 'F1' will invoke the BIOS SETUP PROGRAM.

62. A description of the error messages appears below:

a. **CH-2 Timer Error**. Most AT standard system boards include two timers. An error with time one is a fatal error, explained in Appendix A. If an error occurs with timer two, this error message appears.

b. **INTR #1 Error**. The first interrupt channel failed the POST routine.

c. **INTR #2 Error**. The second interrupt channel failed the POST routine.

d. **CMOS Battery State Low**. There is a battery in your system board which is used for storing the CMOS values. This battery appears to below in power and needs to be replaced.

e. **CMOS Checksum Failure**. After the CMOS values are saved, a checksum value is generated to provide for error checking. If the previous value is different from the value currently read, this message appears. To correct this error, you should run the BIOS SETUP PROGRAM.

f. **CMOS System Options Not Set**. The values stored in the CMOS are either corrupt or non-existent. Run the BIOS SETUP PROGRAM to correct this error.

g. **CMOS Display Type Mismatch**. The type of video stored in the CMOS does not match the type detected by the BIOS. Run the BIOS SETUP PROGRAM to correct this error.

h. **Display Switch Not Proper**. Some systems require that a video switch on the motherboard be set to either colour or monochrome, depending upon the type of video you are using. To correct this situation, set the switch properly (remember to shut down the system first).

i. **Keyboard is locked**. The keyboard lock on the system is engaged. The system must be unlocked to continue the boot up procedure.

j. **Keyboard Error**. The BIOS has encountered a timing problem with the keyboard. You may also set the Keyboard option in the BIOS SETUP PROGRAM to 'Not Installed', which will cause the BIOS to skip the keyboard POST routines.

k. **KB/Interface Error**. The BIOS has found an error with the keyboard connector on the system board.

l. **CMOS Memory Size Mismatch**. If the BIOS finds the amount of memory on your system board to be different from the amount stored in CMOS, this error message is generated. Run the BIOS SETUP PROGRAM to correct this error.

m. **FDD Controller Failure**. The BIOS is not able to communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered off.

n. **HDD Controller Failure**. The BIOS is not able to communicate with the hard disk drive controller. Check all appropriate connections after the system is powered off.

o. **C**: **Drive Error**. The BIOS is not receiving any response from hard disk drive C, it may be necessary to run the 'Hard Disk Utility' to correct this problem. Also, check the type of hard disk selected in the 'Standard CMOS Setup' of the BIOS SETUP PROGRAM to see if the correct hard disk drive has been selected.

p. **D**: **Drive Error**. The same error has occurred with hard drive D, follow the procedures in 'D: Drive Error' to correct this situation.

q. **C**: **Drive Failure**. The BIOS cannot get any response form the hard disk drive C. It may be necessary to replace the hard disk.

r. **D**: **Drive Failure**. The same error as 'C: Drive Failure' has occurred with hard drive D.

s. **CMOS Time** & **Date Not Set**. Run the 'Standard CMOS Setup' of the BIOS SETUP PROGRAM to set the time and date of the CMOS.

t. **Cache Memory Bad**, **Do Not Enable Cache**! The BIOS has found the cache memory of the motherboard to be defective. Consult your system manufacturer to repair this problem.

u. **8042 Gate A20 Error**. The Gate A20 portion of the keyboard controller (8042) has failed to operate correctly. The 8042 should be replaced.

v. **Address Line Short**. An error has occurred in the address decoding circuitry of the motherboard.

w. **DMA #2 Error**. An error has occurred with the second DMA channel on the motherboard.

x. **DMA #1 Error**. An error has occurred with the first DMA channel on the motherboard.

y. **DMA Error**. An error has occurred with the DMA controller on the motherboard.

z. **No ROM Basic**. The error occurs when a proper bootable sector cannot be found on either the floppy diskette drive A or the hard disk drive C. The BIOS will try at this point to run ROM BASIC and the error message will be generated when the BIOS does not find it.

aa. **Diskette Boot Failure**. The diskette used to boot up in floppy drive A is corrupt, which means you cannot use it to boot up the system. Use another boot diskette and follow the instructions on screen.

bb. **Invalid Boot Diskette**. The BIOS can read the diskette in floppy drive A, but it cannot boot-up the system with it. Use another boot diskette and follow the instructions on screen.

cc. **On Board Parity Error**. The BIOS has encountered a parity error with some memory installed on the motherboard. The message will appear as follows:

ON BOARD PARITY ERROR
ADDR (**HEX**) = (**XXXX**)

dd. Where XXXX is the address (in hexadecimal) at which the error has occured. 'On Board' means that it is part of the memory attached directly to the motherboard, as opposed to memory installed via an expansion card in a bus slot.

ee. **Off Board Parity Error**. The BIOS has encountered a parity error with some memory installed in a bus slot. The message will appear as follows:

OFF BOARD PARITY ERROR
ADDR (**HEX**) = (**XXXX**)

ff. Where XXXX is the address (in hexadecimal) at which the error has occurred. 'Off Board' means that it is part of the memory installed via and expansion card in a bus slot, as opposed to memory attached directly to the motherboard.

gg. **Parity Error** ???? The BIOS has encountered a parity error with some memory in the system, but it is not able to determine the address of the error.

Appendix C

63. Due to the unique nature of the chipset the following EISA functions are not supported on this motherboard[24]:

a. Non-ISA compatible DMA

b. Non-ISA compatible interrupts

c. Non-ISA compatible timers (i.e., sanity, watchdog timer, etc[25])

d. DMA to physical memory addresses that have bits 28, 29 or 30 turned on. However, this should only mean that the chipset cannot do DMA to physical memory above 256MB.

64. HiNT chose not to implement some of these non-ISA compatible redundant features defined by EISA, for example the sanity timer because it is not an ISA function and its function in EISA applications are not obvious. The sanity timer does nothing but generates periodic interrupts which may slow down system performance. At the BIOS level, the timer is turned off upon system power-up. No applications have been known to use this feature yet.

65. However, some EISA cards may not function correctly, so try to enable the following as a troubleshooting procedure:

a. 32-bit DMA transfer only

b. Level triggered interrupt (EDGE)[26]

66. This can be achieved by editing the .CFG file of the affected EISA card with a text editor, an example being is the file for the AHA-1742A EISA Fast SCSI-2 host adapter[27].

67. Edit the !ADP0002.CFG file and change the following:

a. SHARE = "AHA1740" to SHARE = NO

b. TRIGGER = LEVEL to TRIGGER = EDGE

68. Another limitation of the CS8002 is the DMA controller, as it is an ISA DMA controller, limited to 16-bit data transfers and 24-bits of address (16MB addressing limitation). However, this is unimportant to a bus mastering EISA SCSI controller, such as the Adaptec 1742 EISA Fast SCSI-2 host adapter, as it has an on-board DMA controller, the HiNT chipset does not restrict the full 32-bit DMA capabilities of bus mastering DMA devices attached to the EISA bus[28].

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[24] https://groups.google.com/g/comp.os.ms-windows.programmer.win32/c/uDh7RWrEltc
[25] https://stason.org/TULARC/pc/pc_hardware_faq/2_43_What_disadvantages_are_there_to_the_HiNT_EISA_chip_set.html
[26] https://www.vogons.org/viewtopic.php?f=46&t=69768
[27] Q: Adaptec 1740 Enchanced mode + Hint chipset (google.com)
[28] https://groups.google.com/g/comp.sys.ibm.pc.hardware/c/1FbH7-aizTU/m/PPtwUGwV6H4J

69. Other EISA cards require these features and are therefore unusable on this motherboard. But if you are using bus mastering cards that allow 32-bit DMA and 32-bit addressing they should work.

70. The Altura XL EISA boards are not completely compatible with this motherboard. Do not install EISA-8 or EISA-EX controllers on this motherboard, use the ISA-8 or ISA-EX instead[29].

71. The Racal Interlan ES3210 Network Interface Card is known not to work, failing both DMA and Interrupt testing[30].

[29] https://www.alturaxl.com/docs/ipll_supplement.pdf
[30] https://groups.google.com/g/comp.sys.ibm.pc.hardware/c/1FbH7-aizTU/m/PPtwUGwV6H4J

Appendix D Contents of !HIT0001.cfg[31]

```
;3-16-92, HiNT Corp. U.S.A.
;EISA-486 Demo Board
;This configuration file is only used for HiNT's demo board.
;HiNT will not be responsible for any mistake or any addition change need
;for this demo board.
BOARD
    ID="HIT0001"
    NAME="EISA-486 Demo Board"
    MFR="HINT"
    CATEGORY="SYS"
    SLOT=EMB(0)
    READID=YES
    COMMENTS="This is the Board Identification Block comment field for the
        EISA-486 Main Board"
    HELP="This is the main board configuration help field for EISA-486
        Main Board."

SYSTEM
    NONVOLATILE=8192
    SLOT(1)=EISA
        LENGTH=341
        BUSMASTER=YES
    SLOT(2)=EISA
        LENGTH=341
        BUSMASTER=YES
    SLOT(3)=EISA
        LENGTH=341
        BUSMASTER=YES
    SLOT(4)=EISA
        LENGTH=341
        BUSMASTER=YES
    SLOT(5)=EISA
        LENGTH=341
        BUSMASTER=YES
    SLOT(6)=ISA16
        LENGTH=341
        BUSMASTER=NO
    SLOT(7)=ISA16
        LENGTH=341
        BUSMASTER=NO
    SLOT(8)=ISA16
        LENGTH=341
        BUSMASTER=NO

FUNCTION="Co-processor"
    CHOICE="Installed"
```

[31] http://66.113.161.23/~mR_Slug/EISA/!HIT0001.CFG/1992-03-18/

http://datasheets.chipdb.org/IBM/x86/486/40006.PDF

HINT CS8001/ 8002
Supply Voltage: 5
WB Cache: no
Suspend Mode: no
SMM: NO
Note: PCI bridge in Q3 94

SCSI Board that appears to work
http://www.verycomputer.com/73_16b8aaf8dfa0484d_1.htm
AHA-1510/1520/1522 AIC-6260/6360
Also to use double buffer

The manual refers to the board as a "Super ISA" instead of an EISA.

G486HVL motherboards. We purchased our PCs from Cornell Computer Systems. The board supports the following:
1. 3 EISA slots
2. 5 ISA slots
3. 2 VLB slots
4. 8 16mB simms
5. 64/128/256 kB direct map cache with either write back or write through

Socketed IC's

U40, MB8464A-10L-SK (Plastic Package DIP-28-M04)
CMOS 64K BIT LOW POWER SRAM
https://nfggames.com/X68000/Development/datasheets/MB8464A%20-%20SRAM.pdf
---
U34, PAL16L88CN
https://pdf1.alldatasheet.com/datasheet-pdf/view/108212/NSC/PAL16L8.html
---
U24 and U25, PAL16R4BCN (Possibly)
20-Pin TTL Programmable Array Logic
https://www.electronicsdatasheets.com/manufacturers/rochester-electronics/parts/pal16r4bcn
---
Serial 930309468

https://groups.google.com/g/comp.sys.ibm.pc.hardware/c/1FbH7-aizTU/m/PPtwUGwV6H4J

like the HINT motherboard you are referring to is operating
in the Super-ISA mode, which probably cannot do more than 16-bit
data transfers. I deduce this limitation from part of the description
of the CS8002 chip, which says:

SD0-15 [data bits 0 through 15] is supported through the chip
while SD16-31 is supported through external buffers, with all
the controls provided by the CS8002.

SD0 ~ 15 (System Data Bus), these signals provide data bus bits 0 ~ 15 for the peripheral devices. All 8-bit devices use SD 0 ~ 7 for data transfers. The 16-bit devices use 0 ~ 15. To support 8-dit devices, the data on 8 ~ 15 will be gated to 0 ~ 7 during 8-bit transfers to these devices. The 16-bit microprocessor cycles will be converted to two, 8-bit cycles for 8-bit peripherals automatically.

DIMM-PC 520 manual (kontron.com)