Quiz 9, COE 233, Term 252 B

Student Name: **ID#:**

Q1) A processor supports four types of instructions. The execution of each instruction can be divided into smaller subtasks, as shown below. The numbers indicate the time required (in nanoseconds (ns)) for each stage for every instruction type. If a stage has no value, it means that stage is not required for that particular instruction type.

Instruction Class/Type	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5
A	190	130	80		100
B	190	130	80	250	100
C	190			250	100
D	190				100

Assume that a program with 2 million instruction has the following distribution:
Type-A (40 %), Type-B (30%), Type-C (10 %) , Type-D (20 %)

a) Assume a single cycle CPU is built, what would be the program execution time.

Clock cycle is dictated by the longest instruction (timewise), which is type B and the clock cycle=750 ns

ET= $(2{,}000{,}000) \times 1 \times 750\times10^{-9} = 1500 \times10^{-3} = 1.5$ seconds

b) Assume a multi-cycle CPU is built, what would be the program execution time.

Clock cycle is dictated by the longest stage (timewise), which is stage-4 and the clock cycle=250 ns

CPI= $0.4(4) +0.3(5) +0.1(3) + 0.2(2) = 1.6 + 1.5 + 0.3 + 0.4 = 3.8$

ET= $(2{,}000{,}000) \times 3.8 \times 250 \times10^{-9} = 2 \times \frac{3800}{4} \times 10^{-3} = 1900 \times 10^{-3} = 1.9$ seconds

c) Which one is faster (single or multi cycle) and by how much (what is the speedup)?

Single cycle is faster by = $\frac{1.9}{1.5} = 1.9 \times \frac{2}{3} = \times \frac{3.8}{3} = 1.3$ (approximately without calculate) or 1.2667

Q2) a) A direct mapped cache has 5 offset bits, 13 index bits and 10 tag bits. What is the cache capacity (total cache data size) in KB?

Size= $2^{13} \times 2^5 = 2^{18} = 256$ KB

b) An 8 way set associative cache with same number of offset, index, and tag bits as in (a); What is the cache capacity in MB?

Size= $2^{18} \times 8 = 2^{18} \times 2^3 = 2^{21} = 2$ MB

c) Assume the direct map cache in (a) **already** have the following **valid cache lines** (given as : index(its value) with tag (its value):
index (2) with tag (5) , index (3) with tag (4) , and index (4) with tag (2).
Now the next address generated is: 0x010007E, does that generate: HIT or MISS? Explain your answer.

The address in binary: 0000 0001 0000000000000 0111 1110

The highlighted underlined is the index, it is 3 in decimal.
The tag are the bits to the left of the index, they=4 in this address

In the cache, the block with index 3 has the same tag as the new address (4). That means, it is a HIT

d) Given that a combined HIT rate in Cache is 90%, answer the following 4 questions.

- what is the combined miss rate? 10%

- If The D_cach miss rate is 12% and the load/store instruction are 25% of the code, what is the I_cache miss rate?
  Let the I_cach miss rate is X:

  0.1 = X + (0.12)(0.25)

  X= 0.1 - 0.03 = 0.07 (7%)

- If the miss penalty is 50 clock cycles and the CPI = 2.2 (without miss stall). What is the overall CPI (including the MISS stall).

  Overall CPI = 0.1(50) +2.2 = 7.2

- What is this Cache AMAT (Average Memory Access Time), assuming the HIT time is 1 clock cycles.

$$\text{AMAT} = 1 + \frac{0.1}{1.25}\ 50\ =\ 1\ +\ \ 0.1\ \ \times \frac{4}{5}\ \ \times 50\ = 5$$