



SRI KRISHNA INSTITUTE OF TECHNOLOGY

(Accredited by NAAC, Approved by A.I.C.T.E. New Delhi, Recognised by Govt. of Karnataka & Affiliated to V.T U., Belagavi)
#57, Chimney Hills, Hesaraghatta Main Road, Chikkabanavara Post, Bengaluru- 560090

Department of Electronics Engineering-VLSI D&T

Subject Name: **Digital VLSI Design**
SEM:5TH DIV: VI A

Subject Code : **BVL503**
Issue date : **18.09.2025**

Faculty: **Dr. N C Patil**

Submission date: **20.09.2025**

ASSIGNMENT -I Questions

SL No	Question	CO	Level	Marks
1	Explain the operation of MOS transistor as switches	1	L1	5
2	Explain the working of i) CMOS Inverter ii) 2 input NAND gate with CMOS circuits	1	L2	5
3	Explain the operation of i) 2:1 Mux using TG ii) D Flip Flop	1	L2	5
4	Explain the circuit representation i) Behavioral ii) Structural iii) Physical	1	L1	5
5	Compare the CMOS and nMOS Logic	1	L2	5
6	Sketch a static CMOS gate computing $Y = \overline{(A + B + C)} \cdot D$.	1	L2	5
7	Sketch a static CMOS gate computing $Y = \overline{(A + B)} \cdot \overline{(C+D)}$	1	L2	5

Faculty Signature



SRI KRISHNA INSTITUTE OF TECHNOLOGY

(Accredited by NAAC, Approved by A.I.C.T.E. New Delhi, Recognised by Govt. of Karnataka & Affiliated to V.T U., Belagavi)
#57, Chimney Hills, Hesaraghatta Main Road, Chikkabanavara Post, Bengaluru- 560090

Department of Electronics & Communication Engineering

Subject Name: **Digital VLSI Design**
SEM: DIV: VI A
Faculty: Dr. N C Patil

Subject Code : BVL503
Issue date :
Submission date:

Assignment-I Questions

1	Explain the operation of nMOS enhancement mode transistor with its physical structure	1	L1	5
2	Explain i) Threshold voltage and ii) Body effect	1	L2	5
3	With neat diagram explain V-I characteristics for N and P MOS transistors	2	L2	5
4	Explain CMOS inverter DC Characteristics	2	L2	5
5	Explain the Influence of β_n/β_p ratio on transfer characteristics	2	L2	5
6	Explain the Noise margin	2	L2	5
7	Explain the Pseudo nMOS inverter with its DC characteristics	2	L2	5
8	Explain the Transmission gate DC characteristics	2	L2	5
9	Explain the concept of Latch-up in CMOS	2	L2	5

Faculty Signature