EE319K Lecture Lec08.ppt in class worksheet

Question 1. What is a thread?

Question 2. What is the main thread? What are interrupt threads?

Question 3. What are the five steps that occur automatically (in hardware) as the context switches from the main thread to an interrupt thread?

Question 4. Define the following terms as they relate to interrupts.

Hardware trigger
Interrupt enable bit I in the PRIMASK register
Interrupt enable bit in the NVIC_EN0_R register
Interrupt priority in the NVIC_SYS_PRI3_R or NVIC_PRI1_R register
Interrupt arm bit like bit1 (INTEN) in the NVIC_ST_CTRL_R register
Interrupt vector

Question 5. What is an interrupt acknowledge? How does the SysTick interrupt get acknowledged and how is SysTick acknowledge different from the other interrupts?

Question 6. Notice the similarity of the answers to these two questions.
Part a) According to AAPCS, what must a function do if it wishes to use R4-R11?
Part b) What must an ISR do if it wishes to use R4-R11?

Question 7. Notice the difference between the answers to these two questions.
Part a) According to AAPCS, what must a function do if it wishes to use LR?
Part b) What must an ISR do if it wishes to use LR?

Question 8. Do you understand priority?
Part a) What happens if we are running a priority 2 ISR and a priority 1 is triggered?
Part b) What happens if we are running a priority 2 ISR and a second priority 2 is triggered?
Part c) What happens if we are running a priority 2 ISR and a priority 3 is triggered?

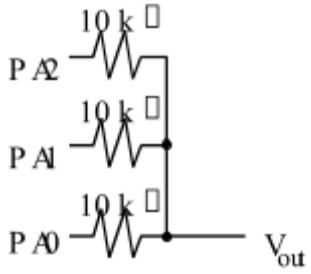
Question 9. Define the following terms:

Latency
Real time
Bandwidth

Question 10. 10 V is applied across the series combination of a 1000Ω and a 2000Ω resistor. What is the voltage across the 2000Ω resistor? What is the current through the 2000Ω resistor?

Question 11. 10 V is applied across the parallel combination of a 1000Ω and a 2000Ω resistor. What is the voltage across the 2000Ω resistor? What is the current through the 2000Ω resistor?

Question 12. What is the output voltage V_{out} when PA2 is high, PA1 is high, and PA0 is low? Assume V_{OH} is 3.3V and V_{OL} = 0V.



Question 13. Define the Nyquist Theorem

Question 14. In terms of a DAC define resolution, range, precision, monotonic.

Question 15. How do you extend the 4-bit binary-weighted DAC to 6-bits?

Question 16. Design a 6-bit R-2R DAC.

Question 17. Write C code that increments a variable, but forces it to a range of 0 to 31 (0,1,2,3, … 29,30,31,0,1,2,…)

Answer 1. A thread is the action cause by executing software, or a thread is executing software.

Answer 2. The main thread is the executing main program. In embedded systems it is executed at reset, runs the initialization once, and then runs an infinite loop forever. An interrupt thread is the execution of an ISR. Each time the interrupt is triggered a new thread is created, executed, and then destroyed.

Answer 3. The five steps that occur automatically (in hardware) as the context switches from the main thread to an interrupt thread are (steps 3-5 can occur in any order, or could occur simultaneously)
1) Finish the current instruction
2) Push 8 registers on the stack (PSW,PC,LR,R12,R3,R2,R1,R0, with R0 on top)
3) Set LR to 0xFFFFFFF9
4) Set IPSR to the interrupt number
5) Set PC to the vector

Answer 4. Define the following terms as they relate to interrupts.
Trigger is a flag in a hardware device register that is set by the hardware event, causing or triggering the interrupt. E.g., Count flag in SysTick is set when the counter goes 1 to 0.

I in the PRIMASK register is the global enable. I=0 is allow, I=1 postpone all interrupts.

Enable bit in the NVIC_EN0_R register allows a particular flag to interrupt.

Interrupt priority sets the relative importance between interrupts. 0 is highest, 7 is lowest

Arm bit allows the trigger flag to interrupt. There are hundreds of trigger flags on the TM4C123, but on any one system we will at most use only a few of them. Most trigger flags have two arm bits, one in the device registers and a second arm in the NVIC_ENx_R register. However, SysTick just has one arm, bit 1 (INTEN) in the NVIC_ST_CTRL_R register.

Interrupt vector specifies the address of the ISR, see step 5 in answer 3.

Answer 5. Normally we acknowledge by clearing the trigger flag that caused that interrupt. Typically this is software that is executed in the ISR. However, SysTick interrupts are automatically acknowledged by hardware when the SysTick ISR is invoked. SysTick ISRs do not have software that clears the trigger, while other ISRs have explicit software to clear the corresponding trigger flag.

Answer 6. Notice the similarity of the answers to these two questions.
Part a) According to AAPCS, if a function wishes to use R4-R11, a function must save (push on stack), use R4-R11, and then restore R4-R11 (pop off stack).
Part b) Since R4-R11 were not pushed on the stack during the interrupt context switch (see answer 3 part 2), if an ISR wishes to use R4-R11, the ISR must save (push on stack), use R4-R11, and then restore R4-R11 (pop off stack).
**** this means all is good as long as the ISR follows AAPCS rules******

Answer 7. Notice the difference between the answers to these two questions.
Part a) According to AAPCS, if a first function calls a second function, the first function must save LR (push on stack), call the second function, and then restore LR (pop off stack).
Part b) Since LR is set to 0xFFFFFFF9 and must still be 0xFFFFFFF9 at the end of the ISR, if the ISR calls another function, the ISR must save LR (push on stack), call the other function, and then restore LR (pop off stack).
**** this means all is good as long as the ISR follows AAPCS rules******

Answer 8. Do you understand priority?
Part a) If we are running a priority 2 ISR and a priority 1 is triggered, the priority 2 ISR is suspended and the priority 1 ISR is run. When the priority 1 ISR finished, control is returned back to the priority 2 ISR.
Part b) If we are running a priority 2 ISR and a second priority 2 is triggered, the second priority 2 ISR is postponed until the first priority 2 ISR completes, at which time the second priority 2 ISR is run.
Part c) If we are running a priority 2 ISR and a priority 3 is triggered, the priority 4 ISR is postponed until the priority 2 ISR completes, at which time the priority 3 ISR is run.

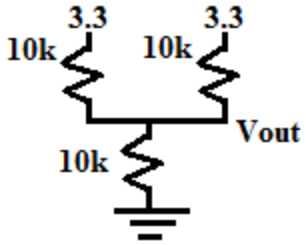
Answer 9. Define the following terms:
Latency is the time between a request for service and the completion of that service.
Real time is when the latency is short and bounded. Service is guaranteed.
Bandwidth is the amount of data transmitted (processes) per second. It could be maximum, or peak bandwidth or it could be the average bandwidth.

Answer 10. 10 V is applied across the series combination of a 1000Ω and a 2000Ω resistor. What is the voltage across the 2000Ω resistor?
Voltage divider V = 10*2000/(1000+2000) = 6.67V
What is the current through the 2000Ω resistor?
I = 6.67V/2000 = 3.33mA
or I = 10V/(1000+2000) = 3.33mA

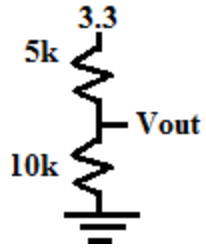
Answer 11. 10 V is applied across the parallel combination of a 1000Ω and a 2000Ω resistor. What is the voltage across the 2000Ω resistor?
The entire 10V is across the resistor (what it means to be parallel combination)
What is the current through the 2000Ω resistor?
I = 10V/2000 = 5 mA

Answer 12. PA2 is high, PA1 is high, and PA0 is low

Step 1) draw an equivalent circuit



Step 2) simplify 10k in parallel with 10k is 5k



Step 3) resistor divider
Vout = 3.3V*10k/15k = 2.2V

Answer 13. Define the Nyquist Theorem
If data is sampled in digital form at a rate of f_s, then the data can faithfully represent signals from 0 to ½ f_s frequencies.

Answer 14. In terms of a DAC define resolution, range, precision, monotonic.
Resolution is the change in output voltage that occurs when the digital input is changed by 1.

Range is the smallest output voltage to the largest output voltage.

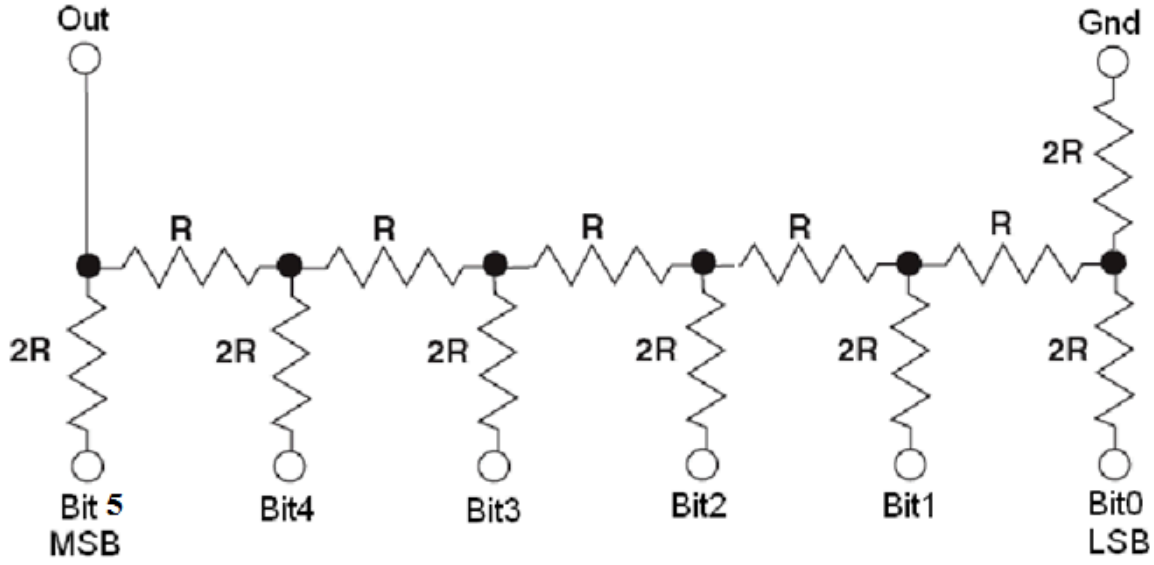
Precision is the number of distinct possible output voltages.

Monotonic means if the digital input is increased then the analog output increases.

Answer 15. How do you extend the 4-bit binary-weighted DAC to 6-bits?
For a 4-bit DAC we have R,2R,4R and 8R.

To make 6-bit DAC we can add two more least significant bits at 16R and 32R. You could try and make two additional most significant bits with ½R and ¼R, but the current may be too large (over 8 mA) for the digital output to manage.

Answer 16. Design a 6-bit R-2R DAC.



Answer 17. Write C code that increments a variable, but forces it to a range of 0 to 31 (0,1,2,3, … 29,30,31,0,1,2,…)

```
Data = (Data+1)&0x1F;
```

or

```
Data = (Data+1)%32;
```

or

```
if(Data==31){
  Data = 0;
}else{
  Data = Data+1;
}
```