Date: 01/24/20
Attendees: Ali, Reza, Bill, Carrie, Kevin, Alex, Christian, Lei, Jinshui, Rita, DJ, Jawad, Tawfik, Manoj

Agenda:

Opens:

1. Generate a list of registrants
2. Panel on workflow for chiplets
    a. Leverage and learn from HBM workflow
    b. Bill can help with the Xilinx contact
    c. Bapi to introduce Bill/Manish/
    d. Confirmed - EDA - Si/Pi tools, Intel - packaging
    e. Packaging conference in Arizona
    f. Revisit plan for the panel by 1/31/20
    g. **Kaby Lake G**
    h. Open Silicon/eSilicon
    i. Jinshui - TSMC flow at Hotchips
3. Updates:
    a. PIPE - need reviewing help from PCIe controller designers
    b. BoW - selected a Vdd, currently focused on Bump map discussions
    c. Link Layer - NXP did a Diport discussion. Diport is an AXI bridge protocol
    d. Open HBI - starting soon
    e. CDX - Picking up steam on power modeling, looking to assemble a chiplet wiki
    f. Biz - Sam traveling
    g. PoC HW - Baseboard design in flight, NXP PChiplet in flight, need an FPGA Pchiplet
    h. PoC SW - looking at MSFT Project Catapult as a template for applications
4. Open HBI also informally referred to as a bunch of wires.
    a. Do we need naming clarity/conventions.
    b. Need clarity on electricals on BoW vs HBI
    c. Is it ok if they end up two separate things
    d. Could end up being disjoint hardware efforts
    e. Manoj - BoW is an umbrella term, HBI is an enhanced HBM compatible interface, leverage bump maps and other attributes
5. Bill
    a. Roadmap symposium going strong - 2/20 (Samsung), 2/21 (Semi)
    b. Moved to Samsung auditorium -
    c. Bill to email reg link
    d. Speakers from Intel, Google
6. Future agenda
    a. Group updates